NANO-THERMISTOR: PRECISE TEMPERATURE MEASUREMENT AT NANOSCALE

Cross-Reference to Related Application

[0001] This application claims the benefit of priority of Singapore Patent Application No. 10202250632Q, filed 29 July 2022, the content of it being hereby incorporated by reference in its entirety for all purposes.

Technical Field

[0002] The present disclosure relates to a temperature sensor. The present disclosure also relates to a method of forming the temperature sensor.

Background

[0003] Precise control of temperature beyond microscale may have become an emerging topic in many scientific and engineering activities, especially for advanced technologies such as extreme ultraviolet (EUV) lithography, biochemical processes, micro/nano-electronics and microfluidics. In the applications that require high temperature precisions, take EUV lithography for instance, slight temperature variation may have great impact on the patterning precision. Since the EUV light tends to be strongly absorbed by most materials, heating of the projection components, such as the reticle, mirrors and motors becomes inevitable. With the semiconductor industry's need for higher resolution, ultra-precise thermal control may have become increasingly important. On the other hand, ultra-high spatial resolution may be required in many fields like biomedicine, where real-time microscale temperature monitoring provides precious diagnostic information for cancer cell screening and the thermal treatment of malignant tumours. In micro/nano-electronics, temperature monitoring with lateral resolution below one micron and accuracy in the order of milliKelvin tends to be demanded to search hot spots during operation. However, the currently used silicon sensors tends to hardly achieve accuracy beyond 1 K and footprint below 200 um^2 due to low sensitivities and large areas required by the complex circuitries (see FIG. 1A).

[0004] Among various temperature sensors, negative temperature coefficient resistance (NTCR) thermistors may possess desirable sensitivities with exponential dependence

of resistance. Challenges with traditional NTCR thermistors lie in achieving high spatial and temperature resolution at the same time. Also, traditional thermistors based on transition metal oxides usually possess large band gaps, but low processibilities pose difficulties in device miniaturization. Early attempts have been implemented to fabricate NTCR thin film using electron-beam evaporation, radio frequency (RF) sputtering, and screen printing, etc. Unfortunately, unsatisfactory performances of those deposited thin films hinder the progress towards practical application. Further improvements also tend to be limited due to the complexity raised from non-stoichiometry, porosity, and inhomogeneity even after annealing. For example, NTCR thin film have been prepared by various deposition and printing techniques, but their predictability and performances were highly limited by non-stoichiometry and phase separation even after annealing.

[0005] Recent reported developments of low dimensional materials may bring new opportunities for device miniaturization. Thermistors based on carbon nanotubes composites, graphene, and ZnS nano wires have recently been demonstrated by several groups. Despite the potentials of microscale temperature measurement, their sensitivities tend to be highly constrained by the nature of small band gap and their reliabilities remain to be improved (see FIG. 1B).

[0006] There is thus a need to provide for a solution that addresses one or more of the limitations mentioned above.

Summary

[0007] In a first aspect, there is provided for a temperature sensor comprising:

two electrodes;

a metal phosphorus chalcogenide configured between and in contact with the two electrodes, wherein the metal phosphorus chalcogenide is represented by a formula of:

$$AMP_2X_6$$

wherein:

A is a metal,

M is a metal,

P is phosphorus, and

X is a chalcogen.

[0008] In another aspect, there is provided for a method of forming the temperature sensor described in various embodiments of the first aspect, the method comprising:

providing the two electrodes;

forming the metal phosphorus chalcogenide; and

configuring the metal phosphorus chalcogenide between and in contact with the two electrodes.

Brief Description of the Drawings

[0009] The drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the present disclosure. In the following description, various embodiments of the present disclosure are described with reference to the following drawings, in which:

[0010] FIG. 1A is a table listing reported developments of temperature sensors embedded on chip.

[0011] FIG. 1B is a table listing reported developments of thermistors based on low dimensional materials.

[0012] FIG. 2A shows the crystal structure of $CuVP_2S_6$: a 2 x 2-unit cell, especially the structure defined by ABC-stacked sulfur framework.

[0013] FIG. 2B shows unit cells of $CuVP_2S_6$ looking down from the "a" axis.

[0014] FIG. 2C shows disordered octahedra cages filled with Cu, P-P and V atoms. The crystal structure of $CuVP_2S_6$ has the lattice parameter a = 5.955 Å, b = 10.321 Å, c = 6.699 Å and $\beta = 107.46^{\circ}$. Every six sulfur atoms form the disordered octahedra, in which V, Cu and P dimers fill the voids in sequence to form a repeating unit.

[0015] FIG. 2D is a planar view looking from the perpendicular direction. The repeating units mentioned for FIG. 2C are stacked alternatively along the perpendicular direction, yielding a hexagonal pattern.

[0016] FIG. 2E shows optical image of CVT-synthesized $CuVP_2S_6$ crystals.

[0017] FIG. 2F shows the Raman spectrum of $CuVP_2S_6$ acquired at room temperature, showing characteristic P-P stretch mode and Cu cation related vibrational mode (top) and XRD spectrum (bottom). "a.u." denotes arbitrary unit.

[0018] FIG. 2G is transmission electron microscopy (TEM) image looking from (001) direction, matching with theoretic model and FFT pattern (top right), showing good crystallinity.

[0019] FIG. 2H shows EDS element mapping of $CuVP_2S_6$, indicating uniform distribution.

[0020] FIG. 3A shows crystal structure of $AgVP_2S_6$ viewed from [0 1 0] direction. The lattice parameter of $AgVP_2S_6$ is: a = 5.921 Å, b = 10.684 Å, c = 6.755 Å and β = 106.62°.

[0021] FIG. 3B shows crystal structure of $AgVP_2S_6$ viewed from [1 0 0] direction. The lattice parameter of $AgVP_2S_6$ is: a = 5.921 Å, b = 10.684 Å, c = 6.755 Å and β = 106.62°.

[0022] FIG. 3C shows crystal structure of $AgVP_2S_6$ viewed from [40 1 10] direction. The lattice parameter of $AgVP_2S_6$ is: a = 5.921 Å, b = 10.684 Å, c = 6.755 Å and β = 106.62°.

[0023] FIG. 3D shows crystal structure of $AgVP_2S_6$ viewed from [1 0 3] direction. The lattice parameter of $AgVP_2S_6$ is: a = 5.921 Å, b = 10.684 Å, c = 6.755 Å and β = 106.62°.

[0024] FIG. 3E shows crystal structure of VPS_3 viewed from [0 1 0] direction. The lattice parameter of VPS_3 is: a = 5.85 Å, b = 10.13 Å, c = 6.66 Å and β = 107.1°.

[0025] FIG. 3F shows crystal structure of VPS_3 viewed from [1 0 0] direction. The lattice parameter of VPS_3 is: a = 5.85 Å, b = 10.13 Å, c = 6.66 Å and β = 107.1°.

[0026] FIG. 3G shows crystal structure of VPS_3 viewed from [40 1 10] direction. The lattice parameter of VPS_3 is: a = 5.85 Å, b = 10.13 Å, c = 6.66 Å and β = 107.1°.

[0027] FIG. 3H shows crystal structure of VPS_3 viewed from [1 0 3] direction. The lattice parameter of VPS_3 is: a = 5.85 Å, b = 10.13 Å, c = 6.66 Å and β = 107.1°.

[0028] FIG. 3I shows Raman spectrum of $AgVP_2S_6$. Peaks are labelled with possible vibrational modes calculated by DFT.

[0029] FIG. 3J shows Raman spectrum of VPS_3. Peaks are labelled with possible vibrational modes calculated by DFT.

[0030] FIG. 3K shows a scanning transmission electron microscope (STEM) image of $AgVP_2S_6$.

[0031] FIG. 3L shows a scanning transmission electron microscope (STEM) image of VPS_3.

[0032] FIG. 4A shows the optical and atomic force microscopy (AFM) images of exfoliated $CuVP_2S_6$ thin flakes with different thicknesses. Scale bar denotes 4 μm.

[0033] FIG. 4B shows the optical and atomic force microscopy (AFM) images of exfoliated $CuVP_2S_6$ thin flakes with different thicknesses. Scale bar denotes 4 μm.

[0034] FIG. 4C shows the optical and atomic force microscopy (AFM) images of exfoliated $CuVP_2S_6$ thin flakes with different thicknesses. Scale bar denotes 4 μm.

[0035] FIG. 4D shows a $CuVP_2S_6$ device fabricated for characterization with 4-wire method. Scale bar denotes 10 μm.

[0036] FIG. 4E is a summarized plot of thickness-dependent resistivity. The conductivity firstly increases with increasing thickness until reaching a peak at around 22 nm and gradually decays afterwards.

[0037] FIG. 4F shows a box chart of resistances measured at different temperatures. All the boxes collapse into single lines in the overall plot, indicating a consistent electronic behavior together with precise measurements at a coefficient of variation below 0.15% (see FIG. 5). The zoomed-in box chart at 20°C is inserted at the left bottom corner.

[0038] FIG. 4G shows the deviations from ideal polaron transport model beyond working temperature range. $CuVP_2S_6$ has the best predictability from -40°C to 110°C.

[0039] FIG. 4H shows the deviations from ideal polaron transport model beyond working temperature range. $CuVP_2S_6$ has the best predictability from -40°C to 110°C.

[0040] FIG. 4I shows a 4-wire $CuVP_2Se_6$ device. Comparing to $CuVP_2S_6$, octahedral scaffold formed by less ionic selenide atoms may be favorable for a stabler cation position, so that the temperature dependency may be much weaker and hence rendering a device suitable for applications that may require such property. Electric measurements indicate that $CuVP_2Se_6$ is non-conductive. Scale bar denotes 10 μm.

[0041] FIG. 4J is a comparison plot of the temperature-dependent conduction behavior for $CuVP_2S_6$, $AgVP_2S_6$, and VPS_3. $CuVP_2S_6$ is fitted with -10 ~ 100 °C, $AgVP_2S_6$ is fitted with -50 ~ 110 °C and VPS_3 is fitted with -30 ~ 130 °C.

[0042] FIG. 4K is a plot of the real-time resistance changes of a $CuVP_2S_6$ device upon temperature change, showing a step-like feature. The zoomed-in plot for the heating step from 0 ~ 10 °C is inserted at top left corner.

[0043] FIG. 4L is a summary plot of the temperature uncertainties caused by material's deviation from ideal equation, environment temperature, measurement error, contact resistance and self-heating, and the statistically combined total uncertainties.

[0044] FIG. 4M is a plot for stability evaluation by the changes of the determinate parameters A and B during heating and cooling cycles.

[0045] FIG. 5 is a table listing the statistics of the $CuVP_2S_6$ nano-thermistor. In FIG. 5 and in the context of the present disclosure, the notation, for example "1.51E-03" (see first row under column header "Coefficient of Variation"), represents a number written in scientific notation. That is to say, the "E" denotes an exponent and indicates the power of 10 by which the number is to be multiplied. This means that for "1.51E-03" the decimal point is moved three places to the left, as indicated by the negative exponent (-03), being equivalent to a value of 0.00151.

[0046] FIG. 6A shows real-time resistance changes upon the heating from 0 °C to 10 °C.

[0047] FIG. 6B is a calibration curve with four terms, where $In(RT) = 14.55 + 3729.03\left(\frac{1000}{T}\right) - 46.94 * 10^4\left(\frac{1000}{T}\right)^2 + 5.05 * 10^7\left(\frac{1000}{T}\right)^3$ and the adjusted R-square equals to 0.99998.

[0048] FIG. 6C is a box plot summarizing the resistances measured by 4-wire method and 2-wire method. Contact resistance is estimated by half of the mean differences.

[0049] FIG. 6D is a plot of the dissipation factor determination at constant currents. The self-heating effect is characterized by the dissipation factor $\delta = \frac{P}{T_f - T_i} = \frac{|S|VI}{\Delta R/R_i}$. $\delta_{3nA} = 0.628\ \mathrm{nW/K}$ and $\delta_{6nA} = 0.154\ \mathrm{nW/K}$, where δ increases with decreasing supply currents, depending on the thermal conductance of the microenvironment.

[0050] FIG. 7A shows the fitting curves of 15 thermistors, outlining in a relatively narrow band. Reasonably small device to device variation can be achieved.

[0051] FIG. 7B is a plot of the parameters of the fitting curves $R = R_0 * \frac{1}{T} * \exp(\beta/T)$.

[0052] FIG. 7C is a plot of adjusted R-square values of the fitting curves and sensitivities of the 15 thermistors, demonstrating almost perfect correlation between the theoretical model and experimental results.

[0053] FIG. 7D is a plot of the temperature uncertainties, estimated by the measurement errors and environment temperature fluctuation (the uncertainties caused by self-heating and contact resistance are insignificant).

[0054] FIG. 8A is a plot of the cycling profile of a $CuVP_2S_6$ device. Temperature cycles between 5 to 80 °C with a 25 °C interval. A detailed characterization is performed from 0 to 80 °C with a 10 °C interval after every 20 half cycles.

[0055] FIG. 8B is a plot of two terms calibration curves for every 20^{th} half cycle.

[0056] FIG. 9A is a SEM image of the selected single-walled carbon nanotube (SWCNT, or CNT for brevity). Scale bar denotes 1 μm.

[0057] FIG. 9B shows the Raman results for the CNT, demonstrating the high quality of the single CNT.

[0058] FIG. 9C depicts an AFM image, a zoomed-in image and the lane scanning profile of the selected single CNT. The height of the CNT is 2 nm.

[0059] FIG. 9D is a SEM image of the single CNT after electrode fabrication. Scale bar denotes 10 μm. Inset is the optical image, scale bar denotes 100 nm.

[0060] FIG. 9E is a plot of CNT resistance changes with respect to voltages.

[0061] FIG. 9F is a plot of the resistance profiles of the CNT under different heating voltages.

[0062] FIG. 10 is a plot of the resistance of the top $CuVP_2S_6$ sensor with respect to time under different voltages.

[0063] FIG. 11 is a table listing the statistical details of the fitting equations for CVPS, AVPS, and VPS.

[0064] FIG. 12A is a plot showing the temperature dependent Raman study of thin layer $AgVP_2S_6$ under vacuum condition. Referring to Raman results on $CuInP_2S_6$ and $Sn_2P_2S_6$, the peak 1 around 79 cm^{-1} is likely to arise from cation transition while peaks 2-4 are likely to rise from S-P-S deformations.

[0065] FIG. 12B is a plot showing temperature dependent powder XRD study of $CuVP_2S_6$. The left (001) peak remains unchanged while the right (33-1) peak shifts to the right with increasing temperature, indicating a temperature-dependent lattice change along a, b directions.

[0066] FIG. 12C is a plot showing temperature dependence of the Raman peak shift. Raman peak shift shows two sharp transitions around 270-290 K and 350 K, which are consistent with the temperature dependent cation transition for $CuInP_2S_6$.

[0067] FIG. 12D shows simulated vibrational mode for the four peaks at 266.39 cm^{-1}, 206.27 cm^{-1}, 172.10 cm^{-1} and 78.95 cm^{-1}, respectively from top to bottom.

[0068] FIG. 13A shows models of micrometric conductor configured with three branches and nanometric carbon nanotube (CNT). The top shows the structure of the micrometric conductor with three branches. The carbon nanotube is a single-walled CNT (SWCNT) – bottom image.

[0069] FIG. 13B is an optical image of the fabricated CVPS device, marked with three positions.

[0070] FIG. 13C is a plot of temperature profiles under different source voltages.

[0071] FIG. 13D is a schematic of the present sensor device configured for SWCNT heating detection.

[0072] FIG. 13E is a plot of the detected temperature changes and CNT heating powers with respect to supply voltage. Inset shows optical image of the device. Sensitivity of -3.06 %/K is used for calculation.

[0073] FIG. 14A is an illustration of current crowding at conductor junctions.

[0074] FIG. 14B is an optical image of the device marked with 5 positions.

[0075] FIG. 14C is a plot of temperature profiles under different source currents.

[0076] FIG. 14D is an illustration of Peltier effect at PN heterojunction.

[0077] FIG. 14E is an optical image of the device. The profile of temperature changes along the marked positions under different sourcing currents.

[0078] FIG. 14F is a plot of the temperature changes and current-voltage (IV) curve of the PN heterojunction.

[0079] FIG. 15A is a three-dimensional (3D) comparison plot of power consumption, footprint and temperature uncertainty (left image). The right image is a temperature range comparison. The nano-thermistors of the present disclosure have the best accuracy of 0.1 K in the range from -40 ~ 110 °C, while it holds accuracy of 0.4 K from -100 ~ 150 °C (also see FIG. 15B).

[0080] FIG. 15B is a table comparison of commercial thermistors, reported IC sensors, commercial IC sensors and the $CuVP_2S_6$ nano-thermistor. "*" denotes that the footprint of cylindrical devices is estimated by the products of diameter and length; footprint of cuboidal devices is estimated by the products of length and width. "**" denotes that the temperature uncertainty is converted into absolute Kelvin using the sensitivity at 300 K, when tolerance is specified in terms of percentage.

Detailed Description

[0081] The following detailed description refers to the accompanying drawings that show, by way of illustration, specific details and embodiments in which the present disclosure may be practiced.

[0082] Features that are described in the context of an embodiment may correspondingly be applicable to the same or similar features in the other embodiments. Features that are described in the context of an embodiment may correspondingly be applicable to the other embodiments, even if not explicitly described in these other embodiments. Furthermore, additions and/or combinations and/or alternatives as described for a feature in the context of an embodiment may correspondingly be applicable to the same or similar feature in the other embodiments.

[0083] The present disclosure describes for a temperature sensor and a method for forming the temperature sensor. The temperature sensor of the present disclosure can be a thermistor. In various embodiments, the temperature sensor is operable as a negative temperature coefficient resistance (NTCR) thermistor.

[0084] NCTR thermistors are thermistors that exhibit a exponential decrease in resistance with an increase in temperature. Such a behavior may arise due to the changes in the energy band structure of a material with temperature. As the temperature rises, more charge carriers (electrons or holes) may become available, leading to increased conductivity and reduced resistance. The material, in the context of the present disclosure, comprises a metal phosphorus chalcognide.

[0085] Advantageously, temperature sensors of the present disclosure satisfies one or more of the following characteristics: a large band gap for good sensitivity; easy processibility for device downscaling; and good crystallinity and stability for repeatable measurements. For instance, temperature sensors of the present disclosure have a considerably improved precision of 0.1 K accuracy and nanometric lateral resolution from -40 to 110 °C. Real-time precise temperature detections are demonstrated from microscale to nanoscale at material interfaces from homojunction to heterojunction in the examples section further below.

[0086] Details of various embodiments of the present temperature sensor, and the method of forming the temperature sensor, and advantages associated with the various embodiments are now described below. Where the embodiments and advantages are

already described in the examples section further hereinbelow, they shall not be iterated for brevity.

[0087] The present disclosure relates to a temperature sensor. The temperature sensor comprises two electrodes, a metal phosphorus chalcogenide configured between and in contact with the two electrodes, wherein the metal phosphorus chalcogenide may be represented by a formula of:

$$AMP_2X_6$$

[0088] wherein A is a metal, M is a metal, P is phosphorus, and X is a chalcogen.

[0089] In various embodiments, A and M may comprise the same metal or A and M may comprise different metals.

[0090] In embodiments where A and M comprise the same metal, A and M may comprise vanadium or tin.

[0091] In embodiments where A and M comprise different metals, A may comprise silver or copper. In such non-limiting embodiments, M may comprise chromium, indium, vanadium, iron, cobalt, nickel, or manganese.

[0092] In various non-limiting embodiments, the metal phosphorus chalcogenide may be represented by a formula of:

$$A^{I}M^{III}P_2X_6$$

[0093] wherein A^{I} is a metal and the metal has a valency of one, M^{III} is a metal and the metal has a valency of three, P is phosphorus, and X is a chalcogen. In such non-limiting embodiments, A^{I} may be silver or copper and M^{III} may be chromium, indium, vanadium, iron, cobalt, or manganese.

[0094] In various embodiments, the chalcogen may comprise sulfur, selenium, or tellurium.

[0095] In various embodiments, the metal phosphorus chalcogenide may comprise $CuVP_2S_6$, $AgVP_2S_6$, $V_2P_2S_6$, $CuInP_2S_6$, or $Sn_2P_2S_6$.

[0096] In various embodiments, the temperature sensor may be a negative temperature coefficient resistance thermistor.

[0097] In various embodiments, the metal phosphorus chalcogenide may have a thickness of 5 nm to 40 nm, 10 nm to 40 nm, 15 nm to 40 nm, 20 nm to 40 nm, 25 nm to 40 nm, 35 nm to 40 nm, etc. In various non-limiting embodiments, the metal phosphorus chalcogenide may have a thickness of 15 nm to 30 nm, 22 nm, etc. These

thicknesses demonstrate for the possibility of the metal phosphorus chalcogenide being ultra-thin and hence the temperature sensor can be an ultra-thin device of a few nanometers. That said, such thicknesses are non-limiting and thicker metal phosphorus chalcogenide can be formed to result in thicker temperature sensor. Advantageously, the present metal phosphorus chalcogenide is versatile in that it does not limit the temperature sensor to certain thicknesses and yet still able to attain the improved measurement precision and spatial resolution.

[0098] In various embodiments, the temperature sensor may further comprise a carbon nanotube configured below the metal phosphorus chalcogenide. The carbon nanotube may be electrically coupled to two electrodes, i.e. one at each end of the carbon nanotube. These two electrodes may be named "two bottom electrodes" as they are configured below the metal phosphorus chalcogenide. In various non-limiting embodiments, the two bottom electrodes may be configured orthogonal (e.g. in a different plane) to the two electrodes which the metal phosphorus chalcogenide is in contact with, as shown in FIG. 13D. In various non-limiting embodiments, the two bottom electrodes may be configured in any orientation with respect to the two electrode that are in contact with the metal phosphorus chalcogenide. In various embodiments, the carbon nanotube may be a single-walled carbon nanotube (SWCNT). The CNT (e.g. SWCNT) may be operated as a nanoscale heat source (e.g. 2 nm diameter). Advantageously, as can be seen through the demonstration of CNT (e.g. SWCNT) in the examples section, the present temperature sensor is capable of real-time temperature monitoring even for ultra-small heat sources/features down to 2 nm dimension.

[0099] In various embodiments, the temperature sensor may further comprise an insulating layer configured between the metal phosphorus chalcogenide and the carbon nanotube. In various embodiments, the insulating layer may comprise hexagonal boron nitride (h-BN), silicon dioxide (SiO_2), hafnium dioxide (HfO_2), aluminum oxide (Al_2O_3), or gallium oxide (Ga_2O_3). Such insulating layers, advantageously, can prevent electrical shorting and at the same time have high thermal conductivity and hence does not interfere with temperature measurement. Any other insulating layers that confer such advantages may be suitable.

[00100] The present disclosure also relates to a method of forming the temperature sensor described in various embodiments of the first aspect. Embodiments and advantages described for the temperature sensor of the first aspect can be analogously valid for the present method described herein, and vice versa. Where the various embodiments and advantages have already been described above and in the examples section further hereinbelow, they shall not be iterated for brevity.

[00101] The method of forming the temperature sensor may comprise providing the two electrodes, forming the metal phosphorus chalcogenide, and configuring the metal phosphorus chalcogenide between and in contact with the two electrodes.

[00102] In various embodiments, forming the metal phosphorus chalcogenide may be carried out via chemical vapor transport. Steps for such a chemical vapor transport may comprise loading a powder mixture into one end of a sealable enclosure, arranging the sealable enclosure, which may be sealed (e.g. prior to placing in a furnace), in a furnace with the one end of the sealable enclosure containing the powder mixture positioned (i) proximal to a reaction zone of the furnace and (ii) distal from a growth zone of the furnace, and heating the furnace to render the reaction zone to have a lower temperature than the growth zone for a period, then heating the furnace to render the reaction zone to have a higher temperature than the growth zone so as to obtain a crystal form of the metal phosphorus chalcogenide. In various embodiments, the method may further comprise maintaining the reaction zone at the higher temperature for a duration shorter than the period.

[00103] In various embodiments, the powder mixture may comprise one or more metals, phosphorus (or phosphorus-containing compound), and the chalcogen. The one or more metals may correspond to the one or more metals in one or more of the formulae described above. For example, the one or more metals may comprise vanadium, tin, silver, copper, chromium, indium, iron, cobalt, nickel, manganese, etc.

[00104] In various embodiments, heating the furnace to render the reaction zone a lower temperature than the growth zone may comprise heating the reaction zone to a temperature of 700 to 900 °C (e.g. 750 to 900 °C, 800 to 900 °C, 850 to 900 °C) and the growth zone to 800 to 1000 °C (e.g. 850 to 1000 °C, 900 to 1000 °C, 950 to 1000 °C) for about or within about 30 hours (e.g. 20 hours, 25 hours). Following this, the furnace may then be heated to to render the reaction zone a higher temperature of 900

to 1050 °C (e.g. 950 to 1050 °C, 1000 to 1050 °C) than the growth zone for about or within about 10 hours (e.g. 5 hours).

[00105] In various embodiments, the method may further comprise providing two bottom electrodes, forming a carbon nanotube which may be electrically coupled to the two bottom electrodes, and configuring the carbon nanotube between and in contact with the two bottom electrodes. As this (e.g. the carbon nanotube, bottom electrodes, and their configuration) has been described in one or more embodiments of the first aspect and also in the examples section, these embodiments shall not be reiterated for brevity.

[00106] In various embodiments, the method may further comprise configuring an insulating layer on the carbon nanotube. The insulating layer may comprise hexagonal boron nitride as described one or more embodiments of the first aspect. For brevity, other examples of the insulating layer are already described in various embodiments of the first aspect and hence shall not be reiterated. In various embodiments, the metal phosphorus chalcogenide may be configured on (e.g. over) the insulating layer.

[00107] The word “substantially” does not exclude “completely” e.g. a composition which is “substantially free” from Y may be completely free from Y. Where necessary, the word “substantially” may be omitted from the definition of the present disclosure.

[00108] In the context of various embodiments, the articles “a”, “an” and “the” as used with regard to a feature or element include a reference to one or more of the features or elements.

[00109] In the context of various embodiments, the term “about” or “approximately” as applied to a numeric value encompasses the exact value and a reasonable variance.

[00110] As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items.

[00111] Unless specified otherwise, the terms "comprising" and "comprise", and grammatical variants thereof, are intended to represent "open" or "inclusive" language such that they include recited elements but also permit inclusion of additional, unrecited elements.

Examples

[00112] The present disclosure relates to a temperature sensor and method of forming the temperature sensor. The temperature sensors of the present disclosure are opreable as thermistors. The thermistors are negative temperature coefficient resistance (NTCR) thermistor. As the thermistors of the present disclosure have a size in the nanoscale (nanoscale resolution), i.e. dimensions are of nanometers, the temperature sensors are exchangeably termed herein "NTCR nano-thermistors", "nano-thermistors", and for brevity "thermistors". Advantageously, even with such considerable small size, the thermistors of the present disclosure are still able to maintain a 0.1 K temperature accuracy (or even higher accuracy).

[00113] The temperature sensors of the present disclosure, i.e. the thermistors, include a metal phosphorous chalcogenide. Non-limiting examples of such metal phosphorus chalcogenide include $CuVP_2S_6$, $AgVP_2S_6$ and $V_2P_2S_6$ (denoted in the present disclosure as VPS_3). Since these three materials share similar properties, $CuVP_2S_6$ was used as a non-limiting example for demonstrating the thermistors of the present disclosure, highlighting the considerably enhanced sensitivity of the present thermistors as compared to traditional temperature sensors. Metal phosphorus chalcogenide of the present disclosure can be represented by the formula AMP_2X_6, wherein A and M are metals, P denotes phosphorus and X is a chalcogen. In certain non-limiting instances, A may be a metal having a valency of one and/or B may be a metal having a valency of three. In such non-limiting instances, the metal phosphorus chalcogenide may be represented by the formula $A^IM^{III}P_2X_6$, wherein A^I and M^{III} denote the metals having valency of one and valency of three, respectively.

[00114] The advantages of thermistors of the present disclosure, such as $CuVP_2S_6$ nano-thermistor, include high temperature precision and ultra-small size. $CuVP_2S_6$ nano-thermistor is operably functional as an electric temperature sensor that reaches 0.1 K temperature precision with nanometric lateral precision. In addition, due to the ultra-high sensitivity and high resistance of the present thermistors, the power required for improved accuracy in temperature sensing is significantly lower than other sensors. Commercial thermistors tend to require current at a level beyond milliamperes and voltage at a level beyond few volts, leading to power consumption higher than milliwatts. Commercial integrated circuit (IC) sensors require input power from tens of

microwatts to milliwatts. In contrast, thermistors of the present disclosure, such as $CuVP_2S_6$ sensors, are operable even at millivolts with a current of around nanoampere, which means power consumption of picowatts, six order of magnitudes smaller than various traditional and commercial sensors. Performance comparison of commercial thermistors, CMOS sensors and the present thermistors (illustrating $CuVP_2S_6$ nano-thermistor as a non-limiting example) is depicted in FIG. 15A and FIG. 15B.

[00115] For a better understanding, the present temperature sensor and method of forming thereof, are described in details, by way of non-limiting examples, as set forth below.

[00116] **Example 1: Introductory discussion**

[00117] In the following examples, NTCR nano-thermistors with nanoscale resolution, while keeping 0.1 K temperature accuracy using the metal phosphorous trichalcogenides $CuVP_2S_6$, $AgVP_2S_6$ and $V_2P_2S_6$ (denoted herein as VPS_3), were demonstrated. Without any intention to limit the examples but for the sole purpose of demonstrating the NTCR nano-thermistors of the present disclosure so as to provide a better understanding thereof, $CuVP_2S_6$ was chosen as the focus as it affords a sensitivity which is desirable for demonstration purpose. Nevertheless, the three nano-thermistors formed based on $CuVP_2S_6$, $AgVP_2S_6$ and VPS_3 share similar properties.

[00118] The metal phosphorous chalcogenide compound $CuVP_2S_6$ is a semiconductor that possesses scaling capabilities and high temperature sensitivities, which are desirable for achieving precise temperature measurement at nanometric scale.

[00119] Bulk $CuVP_2S_6$ crystals, as shown in FIG. 2E, were synthesized by chemical vapour transport (CVT) (see example 2). $CuVP_2S_6$ crystalizes in the monoclinic symmetry, space group C2 with the lattice parameter a = 5.955 Å, b = 10.321 Å, c = 6.699 Å and $\beta = 107.46^{\circ}$. $CuVP_2S_6$ comprises vertically stacked polyhedral layers linked by weak Van der Waals (vdW) interactions. Similar to other, $A^{I}M^{III}P_2X_6$ compounds (A^{I}=Ag or Cu; M^{III}=Cr, In or V and X=S or Se), the structure of $CuVP_2S_6$ is defined by ABC-stacked sulfur framework as shown in FIG. 2A and FIG. 2B. Every six sulfur atoms form a disordered octahedra, in which V, Cu and P dimers fill the voids in sequence to form a repeating unit as illustrated in FIG. 2C. To fully describe the structure, the octahedra chains formed by those repeating units are stacked alternatively along the perpendicular direction, yielding a hexagonal pattern as displayed in FIG. 2D

(see FIG. 3A to 3D for the structure of $AgVP_2S_6$ and FIG. 3E to 3H for the structure of VPS_3). Due to the vdW interactions, thermistors of the present disclosure are also referred to as vdW nano-thermistors.

[00120] Raman spectroscopy with 532 nm excitation shows a distinct peak around 380 cm^{-1} as illustrated in FIG. 2F (see FIG. 3I and 3J for $AgVP_2S_6$ and VPS_3, respectively) which aligns well with the P-P stretching modes for $[P_2S_6]^{4-}$ unit in $CuInP_2S_6$ and $Sn_2P_2S_6$.

[00121] X-ray diffraction (XRD) analysis of $CuVP_2S_6$ shows crystalline diffraction peaks at 2θ values of 13.74°, 27.93°, 30.48°, 35.61° and 53.54°, aligning well with the planes (001), (002), (1-30), (131), and (33-1), respectively (see FIG. 2F).

[00122] Exfoliated $CuVP_2S_6$ nanoflakes were characterized by STEM. The image along [001] direction clearly displays a periodic stripe structure (FIG. 2G), and the fast Fourier transform (FFT) pattern indicates a high crystallinity as shown in the inset of FIG. 2G. Energy Dispersive Spectroscopy (EDS) mapping of the nanoflake confirms the uniform distribution of Cu, V, P and S elements (see FIG. 2H). The corresponding elements ratio was determined to be 0.82: 1.03: 2.02: 6.13. Refer to FIG. 3I to 3L for Raman spectrum and STEM information of $AgVP_2S_6$ and VPS_3.

[00123] **Example 2: Method - Material Systhesis**

[00124] Bulk crystals of $CuVP_2S_6$, $AgVP_2S_6$, and VPS_3 were synthesized via CVT method with a little iodine as the transport agent. A total of 0.5 g powder with the stoichiometric ratio of Cu:V:P:S = 1:1:2:6 was loaded in a silica tube, which was sealed under a high vacuum condition ($<10^{-2}$ Pa). Then, the sealed tube was loaded into a two-zone furnace, whose reaction end was heated to 750 °C within 30 hours, and the growth end was heated to 850 °C. Next, the reaction end was set up to 950 °C within 10 hours, and the furnace was held at the condition for 200 hours. Finally, the furnace was cooled down to room temperature at a rate of 2 °C/hour and bulk $CuVP_2S_6$ crystals were collected at the growth end. The synthesis of $AgVP_2S_6$ and VPS_3 crystals followed the same procedure as that of $CuVP_2S_6$, except the temperature of the two ends was different: 800°C for the growth end and 850°C for the reaction end.

[00125] **Example 3A: Characterization – Scanning Transmission Electron Microscopy (STEM)**

[00126] The STEM samples were prepared by a polypropylene carbonate (PPC) transfer method. $CuVP_2S_6$, $AgVP_2S_6$ and VPS_3 thin flakes were firstly exfoliated onto a wafer spin coated PPC using the typical Stoch tape. PPC film was then peeled and transferred onto a TEM grid (Quantifoil Au grid). Acetone was subsequently used to dissolve the PPC film and clean the residuals. The TEM grid was annealed at 100 °C in vacuum for 4 hours to remove the residuals thoroughly. TEM imaging analysis was performed on a JEOL ARM200CF with a cold field-emission gun and an aberration corrector operating at 80 kV. The inner and outer collection angles for the STEM image were 68 mrad and 280 mrad, respectively, with a convergence semi-angle of 28 mrad. The beam current was about 15 pA for the annular dark-field imaging.

[00127] **Example 3B: Characterization – Atomic Force Microscopy (AFM)**

[00128] A Park NX10 atomic force microscope coupled with the SmartScan™ and XEI software was used for thickness determination. Tapping mode was used with a sufficiently small scanning rate (e.g. 0.4 Hz) for high quality image.

[00129] **Example 3C: Characterization – X-ray Diffraction (XRD)**

[00130] CVT synthesized crystals were grinded into powder for analysis. A Shimadzu XRD-6000 X-ray diffraction system was used to obtain powder X-ray diffraction patterns. Cu Kα radiation (wavelength λ = 1.5406 A) was produced using an operation voltage of 40 kV and a current of 30 mA. Temperature dependent XRD study of $CuVP_2S_6$ was carried out by heating measurements from 20 ˚C to 120 ˚C and cooling measurements from 20 ˚C to -120 ˚C with a 20 ˚C interval. The same was carried out for the other $AgVP_2S_6$ and VPS_3 crystals.

[00131] **Example 3D: Characterization – Scanning Electron Microscopy (SEM)**

[00132] A field emission scanning electron microscope (FESEM) JEOL JSM-7600F attached with a EDX (Oxford INCA) and a E-beam lithography (EBL) system was used to image the microstructure. Elemental composition of $CuVP_2S_6$ bulk single crystals as well as the other bulk single crystals (e.g. $AgVP_2S_6$ and VPS_3) were determined by the attached EDX system. E-beam lithography was conducted at a voltage of 20 KeV and a probe current of 1 nA.

[00133] **Example 3E: Characterization – Raman**

[00134] CVT-synthesized crystals were exfoliated onto silicon wafer using scotch tape method for Raman analysis. A WITec Alpha300 was used to measure the Raman

spectra using a typical 532 nm laser with 2400g/mm gating. Integration time was 60 s and numbers of accumulation was twice. Laser power was kept below 1 mW to avoid laser damage. Temperature dependent Raman study of was conducted using a THMS350V temperature control stage purchased from Linkam company from 410 K to 190 K under vacuum.

[00135] **Example 3F: Characterization – Vibrational Mode Simulation**

[00136] The calculations of unit cell structure optimization and vibrational mode analysis are performed with VASP software package with PBE functional and an energy cutoff of 400 eV. The crystal structure of $CuVP_2S_6$ and AVPS are optimized, and the lattice parameters are a = 6.010 Å, b = 10.443 Å, c = 6.488 Å, α = 90.000 degree, β = 72.006 degree, and γ = 90.000 degree; and a = 6.508 Å, b = 10.760 Å, c = 5.673 Å, α = 90.000 degree, β = 105.721 degree, and γ = 90.000 degree, respectively. The vibrational modes are extracted from eigenvectors and incorporated on atomic coordinates, then visualized via VESTA tool.

[00137] **Example 3G: Thickness Dependent Study**

[00138] Thickness-dependent studies were carried out to investigate how conductivity varies with thickness prior to performance characterization. CVT-synthesized single crystals were mechanically exfoliated onto silicon wafers with 280 nm oxide film using scotch tape method. As-exfoliated nanoflakes with estimated thickness varying from 5 nm to 40 nm were firstly screened using optical microscope (Olympus) and then carefully measured using AFM (FIG. 4A to 4C). Afterwards, Ti/Au (5/50 nm) contact electrodes were fabricated for four probe measurements (FIG. 4D) to eliminate the impact of contact resistance. Electric measurements were conducted in a probe station with connection to an Agilent B1500A semiconductor device parameter analyser. Resistivity was calculated using the formula:

$$\rho = \frac{RL}{A} = \frac{RL}{tW}$$

[00139] where A is the cross-section area, L is the channel length, W is the sample width and t is the sample thickness (FIG. 4E). Thereafter, thermistors were fabricated with a desired thickness and their performances were characterized including working temperature range, temperature precision, time constant and stability.

[00140] **Example 3H: Temperature Dependent Study**

[00141] Tested samples were manually wire bonded onto chips using silver paste and gold wires. The chips were firmly attached onto a THMS350V temperature control stage (Linkam) with connection to the Agilent B1500A semiconductor device parameter analyser. Environmental temperature fluctuation can be controlled at 0.1 K level. At each temperature, a range of currents was applied throughout the sample and the voltage drop across two inner electrodes was recorded. Thereafter, box charts were plotted in data analysis to describe the sample stability as well as the measurement precision as shown in FIG. 4F. Mean values of the resistances were used for fitting in the temperature range from around 230 K to 370 K (FIG. 4J), defining the working temperature range. Mean values of the resistances were used for fitting as demonstrated in FIG. 4J. Standard deviation and coefficient of variation were used for uncertainty analysis (FIG. 4M). The declining trend of resistances with increasing temperature looks similar to the conduction behaviour in the intrinsic region of a semiconductor, in which the resistivity is governed by:

$$R(T) = R_0 exp\,(\frac{E_g}{2kT})$$

[00142] where k is the Boltzmann constant, R_0 is a constant and E_g is the band gap of the semiconductor. Based on this band conduction model, the sensitivity ($\frac{E_g}{2k}$) of a small band gap semiconductor that can be thermally activated at room temperature (0.025 eV) would be too low for real applications. Otherwise, for large band gap semiconductors like silicon, the energy barrier may be sufficiently high to prevent conduction around room temperature. Therefore, band conduction theory may not work for NTCR thermistors in either case. Instead, the conductivity was formulated as the equation below:

$$\sigma = \sigma_0 \frac{1}{T} \exp\left(-\frac{E_a}{kT}\right)$$

[00143] where σ_0 is a constant and E_a is the activation energy of the hopping process. The sensitivity, S, is then derived as:

$$S = \frac{1}{R}\frac{dR}{dT} = -\frac{\beta + T}{T^2}$$

[00144] $AgVP_2S_6$ shows a gentler gradient while VPS_3 (without Cu or Ag cations) demonstrates a lower sensitivity for applications that have such needs.

[00145] **Example 3I: Characterization – Time Constant Analysis**

[00146] The response time of a thermistor was determined by continuous measuring the resistance upon heating and cooling, yielding overall step-like resistance profile. For each step, the resistance changed linearly first, then varied in an exponential manner until it researched a stable state. The time constant is defined by the equation:

$$T = (T_2 - T_1)(1 - e^{(-t/\tau)})$$

[00147] where, τ is the time constant. Time constant is estimated to be 15 s (FIG. 6A) by taking one seventh of the total relaxation time. Notably, time constant is usually determined with sudden temperature change. With the limitation of instrumentation (Linkam temperature control stage), heating process which take a large portion of the total relaxation time, thus time constant estimated by this work was overstated.

[00148] **Example 3J: Characterization – Uncertainty Analysis**

[00149] Temperature accuracy was analysed using the calibration equation:

$$In(RT) = A + B\left(\frac{1000}{T}\right) + \mathrm{C}\left(\frac{1000}{\mathrm{T}}\right)^2 + \mathrm{D}\left(\frac{1000}{\mathrm{T}}\right)^3 + \cdots$$

[00150] where A, B, C and D are determinate parameters. Four terms were adopted for calibration (FIG. 6B). Applying a source current, the uncertainty of the voltage measurement was termed as u_V, and the equivalent temperature uncertainty, u_T, was be determined by the following equation:

$$u_T = \frac{u_V}{|S|} = T^2\frac{V_{cov}}{\beta + T} = T^2\frac{R_{cov}}{\beta + T}$$

[00151] where V_{cov} and R_{cov} are the coefficients of variation for voltage and resistance, respectively. Standard deviation and coefficient of variation were used for uncertainty analysis (FIG. 5). The temperature uncertainty caused by contact resistance u_R was termed as:

$$u_R = \frac{R_c}{R_{thermistor}}\frac{1}{|S|} = \frac{R_c T^2}{(\beta + T)R_{thermistor}}$$

[00152] where R_c is the contact resistance and $R_{thermistor}$ is the thermistor resistance. Contact resistance was estimated by subtracting the 2-wire measurement resistance with the 4-wire measurement resistance (FIG. 6C). Temperature impact on R_c was neglected as this variation was insignificant to the overall u_R. The error caused by the self-heating, $u_{self-heating}$, was proportional to the product of dissipated power and

dissipation factor, which characterized the amount of energy required to elevate temperature by a unit:

$$u_{self-heating} = \delta I^2 R = \frac{\delta V^2}{R}$$

[00153] where δ is the dissipation factor, which varies with the measurement currents (FIG. 6D). Notably, the uncertainty caused by self-heating diminished at sufficiently low measuring currents as the generated heat could be immediately conducted away. Therefore, the self-heating uncertainty demonstrated in FIG. 4L was overstated as the calculation refers to the dissipation factor obtained at 3 nA. Said differently, the true uncertainty caused by self-heating should be even smaller than that displayed in FIG. 4L. In practice, the measurement currents of $CuVP_2S_6$ were timely adjusted with temperature and always kept at the order of picoampere to avert self-heating effect. Environmental temperature fluctuation was controlled at 0.1 K level as the Linkam stage can only reach such precision. Statistics of 15 thermistors were displayed in FIG. 7A to 7D, illustrating slight device to device variation, thus in turn the robustness of $CuVP_2S_6$. The mean sensitivity, -3.06 %/K, would be used for further calculation.

[00154] **Example 3K: Characterization – Cyclability Study**

[00155] The stability was tested through continuous heating and cooling using a cycling profile self-programmed by LabVIEW. Temperature cycled between 5 to 80 ˚C with a 25 ˚C interval and a detailed characterization is performed from 0 to 80 ˚C with a 10 ˚C interval after every 20 half cycles (FIG. 8A to 8B). During heating half cycles, temperature was held at set points for 3 mins to for material relaxation and measurements were conducted only within the last 60 s. The holding time was set as 5 mins for cooling half cycles. Over 200 half cycles were recorded for cyclability analysis in more than 72 hours continuous cycling. The resistance changes of $CuVP_2S_6$ were recorded and the performance was analysed using two term calibration of the equation below for simplification.

$$In(RT) = A + B\left(\frac{1000}{T}\right) + \mathrm{C}\left(\frac{1000}{\mathrm{T}}\right)^2 + \mathrm{D}\left(\frac{1000}{\mathrm{T}}\right)^3 + \cdots$$

[00156] **Example 3L: Device Fabrication – Proof of Concept Application**

[00157] For joule heating detection devices, heat sources were pre-patterned Cr/Au (5/15 nm) bottom electrodes and single SWCNT. Bottom electrodes were patterned by

e-beam lithography (EBL) and e-beam evaporation (EBE). The single-walled carbon nanotubes (SWNTs) were synthesized by the floating catalytic chemical vapor deposition (CVD) method. Ferrocene/sulfur powder was placed upstream as catalyst under 60 °C and growth temperature for the main quartz tube was set as 1100 °C. 1000 sccm argon mixed with 10 sccm methane was used as the carrier gas and carbon source, respectively. A silicon wafer was placed downstream of the quartz tube to deposit the isolated SWNTs directly. Single SWCNT was firstly screened using SEM. Then the thickness was measured using AFM and the quality was confirmed by Raman. Conducting electrodes were then patterned at the two sides (FIG. 9A to 9F). A thin flake of hexagonal boron nitride (h-BN) was then transferred onto the structure as an insulating layer. The as-transferred structure was annealed at 300 ˚C for 10 hours to remove polymer residuals. Afterwards, functional material $CuVP_2S_6$ with suitable size was carefully transferred onwards, aligning well with the bottom electrodes. Top Ti/Au (5/60 nm) electrodes were finally fabricated using EBL and EBE. Electric measurements were conducted in an aluminium foil shielded probe station under high vacuum condition to minimize thermal radiation and convection. For the detection of current crowding at gold homojunction, Cr/Au (5/15 nm) bottom electrodes were pre-patterned with two sharp geometry changes. A series of constant currents were applied to generate current crowding effect (FIG. 14A), while measuring the resistance change of the top $CuVP_2S_6$. For joule heating detection, constant voltages were applied for as demonstrated in FIG. 13C. Change of resistances at different heating scenarios were obtained using the above methodology. For the detection of Peltier effect, a PN junction was pre-constructed using a N-type semiconductor MoS_2 and a P-type semiconductor WSe_2. A thin flake of h-BN served as an insulating layer and a $CuVP_2S_6$ thermistor was built on the top, directly aligning with the heterojunction. The change of temperature was finally calculated using the mean sensitivity of the 15 thermistors.

[00158] **Example 4: Discussion of Performance**

[00159] $CuVP_2S_6$, $AgVP_2S_6$ and VPS_3 (denoted in the present disclosure as CVPS, AVPS, VPS, respectively) demonstrated thermistor behaviours as shown in FIG. 4J with exponential fittings and their coefficient of determination are as high as 0.999 (FIG. 11). Such temperature-dependent conduction behavior was attributed to the unique cation instability in the $A^{I}M^{III}P_2X_6$ compounds (e.g. A=Ag or Cu; M^{III}=Cr, In

or V and X=S or Se) and the corresponding small polaron hopping process: cations favor a tetrahedral coordination instead of sitting at the center of the octahedron, which is driven by the second-order Jahn–Teller coupling between the filled 3d manifold and the empty 4s orbital. The possibility and degree of ion instability depend on the polarizability of the active cations and the ionicity of the scaffold atoms of the octahedra. In the case of $CuVP_2S_6$, competition between coulombic attraction and the specific coordination stability shifts copper cations among three crystallographic sites inside and outside the octahedra (FIG. 12A to 12D). Meanwhile, excess charge carriers firmly trapped in a strong potential well by localized distortions could produce an in-gap state localized below the conduction band bottom. As a result, the thermally activated hopping conduction leads to an Arrhenius-type temperature dependence. Referring to the thermistor guidelines provided by the International Bureau of Weights and Measures (BIPM), the bijective function between resistance and temperature is reformulated as (see example 3H):

$$R = R_0 \frac{1}{T} \exp\left(\frac{\beta}{T}\right)$$

[00160] where R_0 is a reference resistance, and β is an experimentally obtained parameter. The curve slopes shown in FIG. 4J reflect temperature dependency, where $CuVP_2S_6$ shows a better sensitivity (see example 3G and FIG. 4G to 4H) for thickness-dependent study and working temperature determination).

[00161] The response time of $CuVP_2S_6$ upon temperature change is determined from the step-like resistance profile as shown in FIG. 4K (see example 3H and FIG. 6A for time constant characterization). Temperature accuracy is rigorously analysed with the most significant limiting factors (see examples 3H to 3J and FIG. 6B to 6D) as summarized in FIG. 4L. Firstly, measurement uncertainty fluctuates in the range from 0.01 K to 0.05 K, which is closely related to the quality of electric circuitry and noise isolation. Secondly, contact resistance is considered especially at high temperature when the thermistor resistance is low. The corresponding uncertainty gradually raises with temperature from 0.1 mK to 10 mK. Thirdly, measuring current itself may cause joule heating, which can be a serious problem when measurements are taken cross a wide temperature range. For constant current measurements, the power dissipation (I^2R) increases exponentially with thermistor resistance at low temperature; while for

constant voltage measurements, the power dissipation (V^2/R) increases rapidly with decreasing thermistor resistance at high temperature. In practice, the measurement currents are timely adjusted, ensuring self-heating uncertainty below 0.03 K. Lastly, thermal fluctuation associated with calibration environment is estimated to be around 0.1 K as specified by the calibration equipment. As demonstrated in the plot, the combined uncertainty of 0.1 K can be achieved throughout the working temperature range, in which calibration instrumentation becomes the most significant limiting factor. Further developments could be done to enhance the accuracy limit of the present nano-thermistors up to 10 mK via integrating $CuVP_2S_6$ into specially configured measurement circuitry with ultra-high precision and configuring the instrumentation such as minimizing the thermal noise of environment (FIG. 7A to 7D) for the statistics of 15 thermistors). Stability is characterized using two terms calibration (see examples 3J and 3K). FIG. 4M demonstrates the changes over 200 half cycles, where the parameter A slightly oscillates within ± 0.4 %, while the parameter B has a drift below 4 %, indicating nice stability (FIG. 8A and 8B).

[00162] To demonstrate the potentials of precise temperature detections with ultra-high spatial resolution, proof-of-concept devices have been fabricated with heat sources from microscale to nanoscale. FIG. 13A illustrates heat sources developed based on joule heating. The top one is designed with three branches at micrometre scale, in which the heat dissipation is inversely proportional to the resistance (V^2/R). Optical image of the fabricated device is shown in FIG. 13B. The measured results (FIG. 13C) display localized temperature elevation, matching with the branch widths, which in turn imply a successful proof of concept. Moreover, the slight temperature differences among those three positions are clearly presented, reflecting excellent sensitivity. Furthermore, a series of heating voltages from 0.5 V to 3.5 V yield temperature profiles with a consistent trend, suggesting the reliability and robustness of the vdW nano-thermistor.

[00163] As precise temperature measurement at micrometre is still a tough task, pushing the spatial limit down to few nanometric scale becomes increasingly challenging. Taking single-walled carbon nanotube (SWCNT) as an example, despite tremendous research interests attracted, temperature related investigations of such a small feature could only be indirectly conducted using either thermal-related parameters as indicators or complex models with many assumptions. Remarkably,

direct temperature detection with nanometric spatial resolution via a 2-nm-diametered SWCNT heat source (FIG. 9A to 9F) was demonstrated. FIG. 13D shows the schematic of the device. The sensed temperature change exhibits a nearly perfect correlation with heating power (FIG. 13E), proving itself as the most precise thermistor for nanometric thermal detection.

[00164] Aside the robustness of the nano-thermistor, its applications at device level was explored. In micro/nano-electronics, for example, the homojunction and heterojunction interfaces dominate device performances and heat dissipation at such interfaces traditionally tend to be a major bottleneck that constrains integrated circuit (IC) designs. Firstly, thermal monitoring at conductor homojunction may be becoming increasingly important. Interconnect power dissipation may have reached over 50% of the total power in a microprocessor since 2004, and this number appears to keep rising as complementary metal-oxide semiconductor (CMOS) technology scales down to nanometric regime. By this means, it is herein illustrated precise temperature sensing at a conductor homojunctions using gold. FIG. 14A models the localized temperature change based on current crowding and FIG. 14B. shows the optical image of the fabricated device, in which five different positions are marked based on the geometry. FIG. 14C displays the detected temperature profiles with two distinct peaks, aligning well with the design. Meanwhile, the slight temperature differences are well presented at these five positions and temperature profiles remain the same under different currents, which again confirms the excellent sensitivity and robustness of the vdW nano-thermistor.

[00165] As guided by the International Technology Roadmap for Semiconductors (ITRS) and the scaling roadmaps revealed by leading companies in semiconductor industry (such as ASML and Taiwan Semiconductor Manufacturing Company), transition from fin field-effect transistor (FinFET) to nanosheet architecture and even to two-dimensional (2D) atomic channel structure may be an emerging area of exploration for future transistors. Although, high-performance monolayer transistors based on 2D semiconductors may have been reported, temperature effects at such nanoscale atomic interfaces were not explored and not investigated. Herein, real-time detections of the current induced temperature change, so called Peltier effects (FIG. 14D) at a 2D heterojunction are investigated. In this case, MoS_2 and WSe_2 are stacked

to form a PN junction as imaged in FIG. 14E. This 2D PN hetrojunction exhibits a typical diode behaviour with an almost zero reverse current and an exponential forward current as shown in FIG. 14F. The top $CuVP_2S_6$ vdW nano-thermistor simultaneously quantifies the corresponding reverse heating and forward cooling phenomenon. Importantly, reverse current can heat up the junction by over 0.5 K and a forward current of 50 nA causes temperature decreasing by ~2 K. Since reported monolayer MoS_2 transitors can work with a drain current of micronAmperes, the side temperature effects should be rigorously considered during device configuration and operation. These results unveil the potentials of the present nano-thermistor that can facilitate temperature-related studies at atomic interfaces and help establish the foundation for future transistors based on atomically thin materials.

[00166] Besides the breakthroughs in temperature precision and spatial resolution, ultra-low power consumption is another advantage of the present nano-thermistors, as the energy input is significantly lower than other sensors. Specifically, commercial thermistors usually work with currents over milliamperes and a few volts, leading to power consumptions above milliwatts, while IC sensors require power from tens of microwatts to milliwatts. In contrast, the ultra-high sensitivity and high resistance of the present nano-thermistors enable operability at millivolts and nanoamperes, resulting in significantly lesser power consumption of picowatts, six orders of magnitudes smaller than traditional sensors. Performance comparisons of commercial thermistors, IC sensors and this vdW nano-thermistor are summarized in FIG. 15A to 15B.

[00167] **Example 5: Summary**

[00168] In conclusion, the present disclosure has demonstrated metal phosphorous chalcogenide compounds $CuVP_2S_6$ ($AgVP_2S_6$ and VPS_3) as functional nano-thermistors that advantageously attain an accuracy of 0.1 K temperature precision. The precision limit towards about 10 mK can be developed by integrating the materials into specially configured measurement circuitry with ultra-high precision (i.e. improving circuitry and instrumentation) and configuring the calibration conditions such as minimizing the thermal noise of environment.

[00169] Furthermore, as illustrated in the proof-of-concept applications, current crowding, joule heating and PN junction temperature effect are sensed with excellent reliability and single CNT heating joule heating detection is achieved even with

nanometric lateral resolution. The excellent sensitivity and robustness demonstrated above render $CuVP_2S_6$ (and the other metal phosphorus chalcogenides) the potentials to not only facilitate thermal-related study at nanoscale and pave the way to next generation temperature monitoring technology systems. Remarkably, the nano-thermistors are highly sensitive, robust and can achieve ultra-high spatial resolution from microscale to nanoscale. More importantly, real-time temperature monitoring at atomic interfaces from conductor homojunctions to 2D PN heterojunctions were demonstrated. The nano-thermistors can provide a platform for temperature studies of future nanoelectronics. The present disclosure not only facilitates thermal-related research at micro/nanoscale, but also paves the way for next-generation temperature monitoring system for industries.

[00170] The above examples demonstrated that thermistors of the present disclosure have the potential for future applications in precise temperature measurement at nanometric scale. The thermistors, which include metal phosphorus chalcogenide, such as but not limited to, $CuVP_2S_6$, $AgVP_2S_6$ and VP_2S_6, are readily feasible for small scale specialized applications in the perspective of material performance. A straightforward application may be the demand of sensing localized temperature change in various research fields regarding two dimensional materials. $CuVP_2S_6$ thermistors can be capsulated by a thin passivation polymer layer such as polymethyl methacrylate (PMMA) to achieve measurement in liquid environment, so that another window opens for precise microenvironment temperature control in chemical reaction systems and biology/medical systems.

[00171] While the present disclosure has been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the present disclosure as defined by the appended claims. The scope of the present disclosure is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

CLAIMS

1. A temperature sensor comprising:

two electrodes;

a metal phosphorus chalcogenide configured between and in contact with the two electrodes, wherein the metal phosphorus chalcogenide is represented by a formula of:

$$AMP_2X_6$$

wherein:

A is a metal,

M is a metal,

P is phosphorus, and

X is a chalcogen.

2. The temperature sensor of claim 1, wherein A and M comprise the same metal.

3. The temperature sensor of claim 2, wherein A and M comprise vanadium or tin.

4. The temperature sensor of claim 1, wherein A and M comprise different metals.

5. The temperature sensor of claim 4, wherein A comprises silver or copper.

6. The temperature sensor of claim 4 or 5, wherein M comprises chromium, indium, vanadium, iron, cobalt, nickel, or manganese.

7. The temperature sensor of claim 1, the metal phosphorus chalcogenide is represented by a formula of:

$$A^{I}M^{III}P_2X_6$$

wherein:

A^{I} is a metal, and the metal has a valency of one,

M^{III} is a metal, and the metal has a valency of three,

P is phosphorus, and

X is a chalcogen.

8. The temperature sensor of any one of claims 1 to 7, wherein the chalcogen comprises sulfur, selenium, or tellurium.

9. The temperature sensor of claim 1, wherein the metal phosphorus chalcogenide comprises $CuVP_2S_6$, $AgVP_2S_6$, $V_2P_2S_6$, $CuInP_2S_6$, or $Sn_2P_2S_6$.

10. The temperature sensor of any one of claims 1 to 9, wherein the temperature sensor is a negative temperature coefficient resistance thermistor.

11. The temperature sensor of any one of claims 1 to 10, further comprises a carbon nanotube configured below the metal phosphorus chalcogenide, wherein the carbon nanotube is electrically coupled to two bottom electrodes.

12. The temperature sensor of claim 11, further comprises an insulating layer configured between the metal phosphorus chalcogenide and the carbon nanotube.

13. The temperature sensor of claim 12, wherein the insulating layer comprises hexagonal boron nitride, silicon dioxide, hafnium dioxide, aluminum oxide, or gallium oxide.

14. A method of forming the temperature sensor of any one of claims 1 to 13, the method comprising:

providing the two electrodes;

forming the metal phosphorus chalcogenide; and

configuring the metal phosphorus chalcogenide between and in contact with the two electrodes.

15. The method of claim 14, wherein forming the metal phosphorus chalcogenide is carried out via chemical vapor transport, which comprises:

loading a powder mixture into one end of a sealable enclosure, wherein the powder mixture comprises one or more metals, phosphorus, and the chalcogen;

arranging the sealable enclosure, which is sealed, in a furnace with the one end of the sealable enclosure containing the powder mixture positioned (i) proximal to a reaction zone of the furnace and (ii) distal from a growth zone of the furnace; and

heating the furnace to render the reaction zone to have a lower temperature than the growth zone for a period, then heating the furnace to render the reaction zone to have a higher temperature than the growth zone so as to obtain a crystal form of the metal phosphorus chalcogenide.

16. The method of claim 15, further comprising maintaining the reaction zone at the higher temperature for a duration shorter than the period.

17. The method of claim 15 or 16, further comprising:

providing two bottom electrodes;

forming a carbon nanotube which is electrically coupled to the two bottom electrodes; and

configuring the carbon nanotube between and in contact with the two bottom electrodes.

18. The method of claim 17, further comprising configuring an insulating layer on the carbon nanotube.

19. The method of claim 18, wherein the insulating layer comprises hexagonal boron nitride, silicon dioxide, hafnium dioxide, aluminum oxide, or gallium oxide.

20. The method of claim 18 or 19, wherein the metal phosphorus chalcogenide is configured on the insulating layer.