A LEVEL SHIFTER AND A METHOD OF SHIFTING AN INPUT LOGIC SIGNAL FROM A FIRST SUPPLY DOMAIN TO A SECOND SUPPLY DOMAIN

TECHNICAL FIELD

The present disclosure relates broadly to a level shifter and a method of shifting an input logic signal from a first supply domain to a second supply domain.

BACKGROUND

Level shifters are used in electronic circuits for changing the voltage of a signal from a first supply domain e.g., first voltage level/domain to a second supply domain e.g., second voltage level/domain. Level shifters may be used in applications such as integrated circuits where input logic voltage level signals are translated to output signals at higher or lower voltage levels.

In general, there is a need for a level shifter that can reliably translate a logic level from a first supply domain to a shifting second supply domain while handling glitches that could occur during operation of the level shifter, and depending on how fast the second supply domain shifts. That is, the second supply domain may be expected to shift during operation of the level shifter, and hence glitches which result from the shift will have to be resolved for proper operation of the level shifter.

Typically, the output of level shifters is in the form of a latch in the second output supply domain. During operation, glitches may occur such that the output latch is corrupted. In one example, when there is an inadvertent/undesired shift in the voltage levels of the second supply domain, an inaccurate logic state is propagated through to the input of the output latch, resulting in an inaccurate output logic signal. In another example, the shift in the voltage levels of the second supply domain can be expected and yet unavoidable as part of the operation of an overall system, resulting in an inaccurate logic state being propagated through to the input of the output latch, which in turn results in an inaccurate output logic signal.

In order to combat glitches from occurring, different circuit designs have been proposed. However, such designs are often complicated and are not as effective. They may also consume relatively large amounts of power, due to their specific design requirements.

Thus, there is a need for a level shifter and a method of shifting an input logic signal from a first supply domain to a second supply domain that seek to address or alleviate at least one of the above problems.

SUMMARY

In accordance with a first aspect of the present disclosure, there is provided a level shifter for shifting an input logic signal from a first supply domain to a second supply domain, the level shifter comprising, a set-level circuit configured to provide a pulse in a raw set signal in the second supply domain when a rising edge is detected in the input logic signal in the first supply domain; a reset-level circuit configured to provide a pulse in a raw reset signal in the second supply domain when a falling edge is detected in the input logic signal in the first supply domain; a slew filter coupled to the set-level and reset-level circuits, the slew filter configured to filter the raw set signal and raw reset signal, to provide a filtered set signal and a filtered reset signal, such that pulses which are simultaneously provided in the raw set signal and raw reset signal are filtered away; and an output latch configured to set an output voltage when a pulse is detected in the filtered set signal and to reset the output voltage when a pulse is detected in the filtered reset signal.

The slew filter may be a set-reset latch in the second supply domain.

The output latch may be an other set-reset latch in the second supply domain.

The set-level circuit may comprise a first inverter in the second supply domain, the first inverter comprising, a first inverter output terminal coupled to a first slew filter input terminal; and a first inverter input terminal coupled to a first pull-up circuit at a first node, said first pull-up circuit configured to pull up the first node and maintain the first node in a pulled-up state; and a first pull-down circuit at the first node, said first pull-down circuit configured to pull down the first node momentarily, when the rising edge is detected in the input logic signal, such that the first inverter output terminal is configured to output the pulse in the raw set signal to the first slew filter input terminal when the first node is pulled down.

The reset-level circuit may comprise a second inverter in the second supply domain, the second inverter comprising, a second inverter output terminal coupled to a second slew filter input terminal; and a second inverter input terminal coupled to a second pull-up circuit at a second node, said second pull-up circuit is configured to pull up the second node and maintain the second node in a pulled-up state; and a second pull-down circuit at the second node, said second pull-down circuit configured to pull down the second node momentarily, when the falling edge is detected in the input logic signal, such that the second inverter output terminal is configured to output the pulse in the raw reset signal to the second slew filter input terminal when the second node is pulled down.

The first pull-down circuit may comprise, a first pulse generator in the first supply domain, said first pulse generator configured to generate a first pulse in response to rising edges in the input logic signal; a first pull-down component configured to pull down the first node; and a first switch configured to switch on momentarily by the first pulse, thereby providing a first electrical path between the first pull-down component and the first node, said first electrical path allowing the first node to be pulled down.

The second pull-down circuit may comprise, a second pulse generator in the first supply domain, said second pulse generator configured to generate a second pulse in response to falling edges in the input logic signal; a second pull-down component configured to pull down the second node; and a second switch configured to switch on momentarily by the second pulse, thereby providing a second electrical path between the second pull-down component and the second node, said second electrical path allowing the second node to be pulled down.

The slew filter may be configured to utilize the presence of pulses simultaneously provided in the raw set signal and raw reset signal to the slew filter as the condition to filter out common-mode glitches in the raw set and reset signals generated on the set-level and reset-level circuits.

The level shifter may further comprise a reference-level circuit configured to generate a reference signal for the slew filter, the reference-level circuit configured to replicate the configuration of the set- and reset-level circuits, such that common-mode glitches at the first and second nodes of the set- and reset-level circuits are also captured at the reference-level circuit.

The reference-level circuit may comprise a third inverter comprising, a third inverter output terminal coupled to a third slew filter input terminal; and a third inverter input terminal coupled to a third pull-up circuit at a third node, said third pull-up circuit is configured to pull up the third node and maintain the third node in a pulled-up state; and a third pull-down circuit at the third node, said third pull-down circuit configured to pull down the third node when a third switch is activated, said activation of the third switch providing a third electrical path between the third pull-down circuit and the third node.

The slew filter may be configured to utilize the reference signal as the condition to filter out common-mode glitches in the raw set and reset signals generated on the set-level and reset-level circuits.

The level shifter may further comprise a refresh block configured to detect an occurrence of slew of the second supply domain and to adapt the input logic signal in the first supply domain accordingly, based on the detection such that the input logic signal that occurs during the slew is not lost and is able to propagate to the output latch.

The first pull-down circuit may comprise a first capacitive circuit, the first capacitive circuit comprising, a first pulse generator in the first supply domain, said first pulse generator configured to generate a first pulse in response to rising edges in the input logic signal; and a first capacitor configured to pull down the first node momentarily by the first pulse.

The second pull-down circuit may comprise a second capacitive circuit, the second capacitive circuit comprising, a second pulse generator in the first supply domain, said second pulse generator configured to generate a second pulse in response to falling edges in the input logic signal; and a second capacitor configured to pull down the second node momentarily by the second pulse.

The set-level circuit may comprise a first buffer in the second supply domain, the first buffer comprising, a first buffer output terminal coupled to a first slew filter input terminal; and a first buffer input terminal coupled to a first pull-up circuit at the first node, said first pull-up circuit configured to pull up the first node momentarily, when the rising edge is detected in the input logic signal, such that the first buffer output terminal is configured to output the pulse in the raw set signal to the first slew filter input terminal when the first node is pulled up; and a first pull-down circuit at the first node, said first pull-down circuit configured to pull down the first node and maintain the first node in a pulled-down state; wherein the first pull-up circuit

comprises a first capacitive circuit, the first capacitive circuit comprising, a first pulse generator in the first supply domain, said first pulse generator configured to generate a first pulse in response to rising edges in the input logic signal; and a first capacitor configured to pull up the first node momentarily by the first pulse.

The reset-level circuit may comprise a second buffer in the second supply domain, the second buffer comprising, a second buffer output terminal coupled to a second slew filter input terminal; and a second buffer input terminal coupled to a second pull-up circuit at a second node, said second pull-up circuit configured to pull up the second node momentarily, when the falling edge is detected in the input logic signal, such that the second buffer output terminal is configured to output the pulse in the raw reset signal to the second slew filter input terminal when the second node is pulled up; a second pull-down circuit at the second node, said second pull-down circuit configured to pull down the second node and maintain the second node in a pulled-down state; and wherein the second pull-up circuit comprises a second capacitive circuit, the second capacitive circuit comprising, a second pulse generator in the first supply domain, said second pulse generator configured to generate a second pulse in response to falling edges in the input logic signal; and a second capacitor configured to pull up the second node momentarily by the second pulse.

In accordance with a second aspect of the present disclosure, there is provided a method of shifting an input logic signal from a first supply domain to a second supply domain, the method comprising, receiving the input logic signal; providing a pulse in a raw set signal in the second supply domain using a set-level circuit, when a rising edge is detected in the input logic signal in the first supply domain; providing a pulse in a raw reset signal in the second supply domain using a reset-level circuit, when a falling edge is detected in the input logic signal in the first supply domain; filtering the raw set signal and raw reset signal to provide a filtered set signal and a filtered reset signal using a slew filter, such that pulses which are simultaneously provided in the raw set signal and raw reset signal are filtered away; and setting an output voltage from a latch output when a pulse is detected in the filtered set signal and resetting the output voltage from the latch output when a pulse is detected in the filtered reset signal.

The method may further comprise, pulling up a first node of the set-level circuit and maintaining the first node in a pulled-up state using a first pull-up circuit; and pulling up a second node of the reset-level circuit and maintaining the second node in a pulled-up state using a second pull-up circuit.

The method may further comprise, generating a first pulse from a first pulse generator in response to rising edges in the input logic signal; pulling down the first node of the set-level circuit momentarily by the first pulse; and outputting the pulse in the raw set signal when the first node is pulled down.

The method may further comprise, generating a second pulse from a second pulse generator in response to falling edges in the input logic signal; pulling down the second node of the reset-level circuit momentarily by the second pulse; and outputting the pulse in the raw reset signal when the second node is pulled down.

The method may further comprise, pulling down a first node of the set-level circuit and maintaining the first node in a pulled-down state using a first pull-down circuit; and pulling down a second node of the reset-level circuit and maintaining the second node in a pulled-down state using a second pull-down circuit.

The method may further comprise, generating a first pulse from a first pulse generator in response to rising edges in the input logic signal; pulling up the first node of the set-level circuit momentarily by the first pulse; and outputting the pulse in the raw set signal when the first node is pulled up.

The method may further comprise, generating a second pulse from a second pulse generator in response to falling edges in the input logic signal; pulling up the second node of the reset-level circuit momentarily by the second pulse; and outputting the pulse in the raw reset signal when the second node is pulled up.

The method may further comprise utilizing the presence of pulses simultaneously provided in the raw set signal and raw reset signal to the slew filter as the condition to filter out common-mode glitches in the raw set and reset signals generated on the set-level and reset-level circuits.

The method may further comprise, generating a reference signal for the slew filter using a reference-level circuit, the reference-level circuit configured to replicate the configuration of the set- and reset-level circuits, such that common-mode glitches at the set- and reset-level circuits are also captured at the reference-level circuit; and utilizing the

reference signal as the condition to filter out common-mode glitches in the raw set and reset signals generated on the set- and reset-level circuits.

The method may further comprise, detecting an occurrence of slew of the second supply domain using a refresh block; and generating an additional refresh input to the first supply domain after the occurrence of slew such that the input logic signal that occurs during the slew is not lost and is able to propagate to the output latch.

BRIEF DESCRIPTION OF THE DRAWINGS

Exemplary embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

FIG. 1 is a schematic block diagram of a level shifter for shifting an input logic signal from a first supply domain to a second supply domain in an example embodiment.

FIG. 2 is a circuit diagram of a level shifter for shifting an input logic signal (e.g., input logic signal ***In***) from a first supply/voltage domain (e.g., input VDD-GND supply domain) to a second supply/voltage domain (e.g., floating VB-VS supply domain) in an example embodiment.

FIG. 3A is a circuit diagram of a level shifter for shifting an input logic signal (e.g., input logic signal ***In***) from a first supply/voltage domain (e.g., input VDD-GND supply domain) to a second supply/voltage domain (e.g., floating VB-VS supply domain) in another example embodiment.

FIG. 3B is a circuit diagram of a gated set-reset latch (gated SR latch) in an example embodiment.

FIG. 3C is a circuit diagram of a (non-SR latch) circuit for slew filtering based on the reference signal, in an example embodiment.

FIG. 3D is a circuit diagram of a (non-SR latch) circuit for slew filtering based on pulses which are simultaneously provided in the raw set and reset signals in an example embodiment.

FIG. 3E is a circuit diagram of a (non-SR latch) circuit for slew filtering based on both the reference signal and the pulses which are simultaneously provided in the raw set and reset signals in an example embodiment.

FIG. 4 is a circuit diagram of a level shifter for shifting an input logic signal (e.g., input logic signal ***In***) from a first supply/voltage domain (e.g., input VDD-GND supply domain) to a second supply/voltage domain (e.g., floating VB-VS supply domain) in yet another example embodiment.

FIG. 5 is a circuit diagram of a level shifter for shifting an input logic signal (e.g., input logic signal ***In***) from a first supply/voltage domain (e.g., input VDD-GND supply domain) to a second supply/voltage domain (e.g., floating VB-VS supply domain) in an alternative example embodiment.

FIG. 6 is a schematic flow chart for illustrating a method of shifting an input logic signal from a first supply domain to a second supply domain in an example embodiment.

DETAILED DESCRIPTION

Example, non-limiting embodiments may provide a level shifter and a method of shifting a logic signal from a first supply/voltage domain to a second supply/voltage domain.

FIG. 1 is a schematic block diagram of a level shifter 100 for shifting an input logic signal from a first supply domain to a second supply domain in an example embodiment. An input logic signal 102 in the first supply domain is level shifted to an output logic signal 104a in the second supply domain.

The level shifter 100 comprises a set-level circuit 106 configured to provide a pulse in a raw set signal 108 in the second supply domain when a rising edge, e.g., rising pulse edge is detected in the input logic signal 102 in the first supply domain. The level shifter 100 further comprises a reset-level circuit 110 configured to provide a pulse in a raw reset signal 112 in the second supply domain when a falling edge, e.g., falling pulse edge is detected in the input logic signal 102 in the first supply domain.

The level shifter 100 further comprises a slew filter 114 coupled to the set level circuit 106 and reset-level circuit 110. The slew filter 114 functions to filter out common-mode glitches

that are simultaneously provided at the raw set signal and raw reset signal. In the example embodiment, the slew filter 114 is configured to filter the raw set signal 108 and raw reset signal 112 and to provide a filtered set signal 116 and a filtered reset signal 118, such that pulses which are simultaneously provided in the raw set signal 108 and raw reset signal 112 are filtered away. During operation, raw set and raw reset glitches (i.e., simultaneous pulse signals provided in the raw set signal 108 and raw reset signal 112) happen due to the slew / change / shift in the second supply domain. In other words, it is the slew of the second supply domain that causes the glitches to occur. These glitches can occur without any change in the input signal 102. The glitches can occur due to charge injection into interfacing nodes when the second supply domain slews. Interfacing nodes are the circuit junctions that interface between the first and second supply domain. At the interfacing nodes, charge injection occurs as there are inherent or parasitic resistive and capacitive coupling components (i.e., RC components).

In the example embodiment, the slew filter 114 may be configured to perform its slew filtering function based on one or more predetermined filter/filtering conditions.

In one example, the filter condition may be the presence of pulses simultaneously provided in the raw set signal 108 and raw reset signal 112 to the slew filter 114. In other words, the slew filter 114 may be configured to utilize the presence of pulses simultaneously provided in the raw set signal 108 and raw reset signal 112 to the slew filter 114 as the condition to filter out common-mode glitches in the raw set signal 108 and raw reset signal 112 generated on the set-level circuit 106 and reset-level circuit 110.

In another example, the filter condition may be a reference signal (not shown) generated by a replica/reference-level circuit (not shown). The reference-level circuit may be a circuit that replicates the configuration of the set-level circuit 106 and reset-level circuit 110, such that common-mode glitches at the set-level circuit 106 and reset-level circuit 110 are also captured at the reference-level circuit. In other words, the slew filter 114 may be configured to utilize the reference signal as the condition to filter out common-mode glitches in the raw set signal 108 and raw reset signal 112 generated on the set-level circuit 106 and reset-level circuit 110. It will be appreciated that in this case, common-mode glitches are still simultaneously provided at the raw set signal 108 and raw reset signal 112, but their simultaneous presence is not the condition for filtering by the slew filter 114. In this case, the primary filter condition is the use of (or presence of) the reference signal. In this case, the

filtering condition based on the simultaneous presence of both set and reset pulses may be secondary or optional.

The level shifter 100 further comprises an output latch 120 coupled to the slew filter 114. The output latch 120 is configured to provide the output logic signal, e.g., output voltage 104a in the second supply domain. That is, the output latch 120 is configured to set an output voltage in the second supply domain when a pulse is detected in the filtered set signal 116 and to reset the output voltage in the second supply domain when a pulse is detected in the filtered reset signal 118. During operation, the filtered set signal 116 is configured to change (or set) the output voltage 104a from logic low to logic high. The filtered reset signal 118 is configured to change (or reset) the output voltage 104a from logic high to logic low. The output latch 120 may be configured to provide another dependent output voltage 104b which is complementary to the output voltage 104a, i.e., Out_fl and Outb_fl as described in the subsequent figures, where Outb_fl is complementary of Out_fl.

In the example embodiment, the output latch 120 may be a latch, e.g., a set-reset latch and the slew filter 114 may be an other latch, e.g., set-reset latch, specially configured to perform slew filtering function. The level shifter 100 employs the slew filter 114 to block both set and reset glitches from propagating to the output latch 120 when there is a slew or change in the second supply domain, thereby advantageously preventing corruption of the output latch 120. In other words, the slew filter 114 uses digital logic circuitry to block both pulses from propagating to the latch output 120 based on the one or more predetermined filter conditions. In addition, the level shifter 100 may advantageously provide reduced power consumption due to its pulsed nature. For example, where the slew filter 114 is a set-reset latch (e.g., a set-reset latch built by cross-coupled NOR gates), the set-reset latch is able to function as the slew filter due to its “not allowed state”, of S = 1 and R = 1, making both its output = 0, thereby making it suitable for performing the slew filtering function. It will be appreciated that the slew filter 114 is not limited to a set-reset latch, the slew filter 114 may be constructed using other logic gates, e.g., multiple AND gates connected appropriately, to achieve the same or similar technical effects of blocking both set and reset glitches from propagating to the output latch 120 when there is a slew or change in the second supply domain. It will also be appreciated that the output latch 120 is not limited to a set-reset latch, the output latch 120 may be constructed using other types of latches to achieve the same or similar technical effects of changing the output voltage. For example, the output latch may be constructed from cross-coupled back-to-back inverters, with input NMOS pulldowns that can flip the latch. For

example, the output latch may also be implemented using D-flip flops, with appropriate adjustments to the control logic.

In the example embodiment, the level shifter 100 is implemented when either one or the supply domains is floating. The two supply domains (i.e., the first and second supply domains) can have the same or different voltage differences. The architecture of the level shifter 100 may be used to implement a shift up level shifter or a shift down level shifter. For example, in a shift up level shifter, the first supply domain may have a voltage difference of 5V – 0V (GND) (VDD – GND). The second supply domain may be floating and can go from 4V – -1V, to 17V – 12V (VB – VS). For example, in a shift down level shifter, the first supply domain may be floating and can go from 4V – -1V, to 17V – 12V (VB – VS). The second supply domain may have a voltage difference of 5V – 0V (GND) (VDD – GND).

FIG. 2 is a circuit diagram of a level shifter 200 for shifting an input logic signal (e.g., input logic signal ***In***) from a first supply/voltage domain (e.g., input VDD-GND supply domain) to a second supply/voltage domain (e.g., floating VB-VS supply domain) in an example embodiment.

The level shifter 200 comprises a set-level circuit 202 configured to provide a pulse in a raw set signal in the second supply domain when a rising edge, e.g., rising pulse edge is detected in the input logic signal ***In*** in the first supply domain and a reset-level circuit 204 configured to provide a pulse in a raw reset signal in the second supply domain when a falling edge, e.g., falling pulse edge is detected in the input logic signal ***In*** in the first supply domain. The set-level circuit 202 and reset-level circuit 204 are comprised in an input stage 206 and an interfacing stage 208 as shown in FIG. 2. It will be appreciated that the components of the input stage 206 are in the first supply domain and the components of the interfacing stage 208 are in the second supply domain.

The set-level circuit 202 comprises a first inverter INV0, e.g., high threshold voltage inverter $V_{th,inv}$, in the second supply domain coupled to a first pull-up circuit and a first pull-down circuit. The first inverter INV0 comprises a first inverter output terminal coupled to a first slew filter input terminal S_{raw}. The first inverter INV0 further comprises a first inverter input terminal coupled to the first pull-up circuit and the first pull-down circuit at a first node n0.

The first pull-up circuit is configured to pull up the potential/voltage of the first node n0 and maintain the first node n0 in a pulled-up state, when the first pull-down circuit is not in

operation. In the example embodiment, the first pull-up circuit comprises a first resistor R0 coupled between the first node n0 and the floating supply VB.

The first pull-down circuit is configured to pull down the potential/voltage of the first node n0 momentarily, when a rising edge is detected in the input logic signal ***In***, such that the first inverter output terminal is configured to output the pulse in the raw set signal to the first slew filter input terminal S_{raw} when the first node n0 is pulled down.

The first pull-down circuit comprises a first pulse generator 210 e.g., a positive edge pulse generator in the first supply domain and which is configured to generate a first pulse in response to rising edges in the input logic signal ***In***. The first pulse generator 210 comprises a first pulse generator input for receiving the input logic signal ***In*** and a first pulse generator output for outputting the first pulse.

The first pull-down circuit further comprises a first switch e.g., high voltage switch HVSW0 disposed between the first node n0 and the ground GND in the first supply domain, and a first current source I0 for providing a current disposed between the first switch HVSW0 and the ground GND in the first supply domain. The first switch HVSW0 and the first current source I0 are connected in series between the first node n0 to the ground GND. The first switch HVSW0 is configured to switch on momentarily by the first pulse, thereby providing a first electrical path between the first current source I0 and the first node n0. The first electrical path allows the potential at the first node n0 to be pulled down to GND. It will be appreciated that in practice, the potential at the first node n0 may not be pulled down completely to the ground GND. When the first switch HVSW0 is switched on, the current e.g., a fixed current from the first current source I0 is allowed to flow through the first electrical path created. The voltage drop across the first resistor R0 is determined to be the product of the current from the first current source I0 and the resistance of the first resistor R0 (i.e., Voltage drop = I0 x R0). In other words, the amount of potential being pulled down at the first node n0 is controlled by the first current source I0, where the amount of potential being pulled down is the product of I0 and R0. It will be appreciated that the first current source I0 serves as a pull-down component for pulling the first node n0 down to GND. Other examples of a pull-down component may include a simple short or a resistor. Accordingly, the first current source I0 may be replaced by other examples of a pull-down component, such that when the first switch is turned on, the first node n0 will be pulled directly to GND (in the case of a short acting as the pull-down component) or pulled to GND through the resistor (in the case of a resistor acting as the pull-down component).

The set-level circuit 202 further comprises a first diode D0 and a second diode D1 connected in reverse biased between the floating supply VB-VS, with the first node n0 coupled between the diodes D0 and D1. That is, the positive terminals of the first diode D0 and the second diode D1 are connected to the first node n0 and VS, respectively. The negative terminals of the first diode D0 and the second diode D1 are connected to VB and the first node n0, respectively. The diodes D0 and D1 neither pull the first node n0 up to VB nor pull the first node n0 down to GND. Instead, these two diodes D0 and D1 serve as protection clamps, such that the first node n0 can only swing up to one diode voltage above or below VB or VS, respectively.

The reset-level circuit 204 comprises a second inverter INV1, e.g., high threshold voltage inverter $V_{th,inv}$, in the second supply domain coupled to a second pull-up circuit and a second pull-down circuit. The second inverter INV1 comprises a second inverter output terminal coupled to a second slew filter input terminal R_{raw}. The second inverter INV1 further comprises a second inverter input terminal coupled to the second pull-up circuit and the second pull-down circuit at a second node n1.

The second pull-up circuit is configured to pull up the potential/voltage of the second node n1 and maintain the second node n1 in a pulled-up state when the second pull-down circuit is not in operation. In the example embodiment, the second pull-up circuit comprises a second resistor R1 coupled between the second node n1 and the floating supply VB.

The second pull-down circuit is configured to pull down the potential/voltage of the second node n1 momentarily, when a falling edge is detected in the input logic signal ***In***, such that the second inverter output terminal is configured to output the pulse in the raw reset signal to the second slew filter input terminal R_{raw} when the second node n1 is pulled down.

The second pull-down circuit comprises a second pulse generator 212 e.g., a negative edge pulse generator in the first supply domain and configured to generate a second pulse in response to falling edges in the input logic signal ***In***. The second pulse generator 212 comprises a second pulse generator input for receiving the input logic signal ***In*** and a second pulse generator output for outputting the second pulse.

The second pull-down circuit further comprises a second switch e.g., high voltage switch HVSW1 disposed between the second node n1 and the ground GND in the first supply

domain, and a second current source I1 for providing a current disposed between the second switch HVSW1 and the ground GND in the first supply domain. The second switch HVSW1 and the second current source I1 are connected in series between the second node n1 to the ground GND. The second switch HVSW1 is configured to switch on momentarily by the second pulse, thereby providing a second electrical path between the second current source I1 and the second node n1. The second electrical path allows the potential at the second node n1 to be pulled down to GND. It will be appreciated that in practice, the potential at the second node n1 may not be pulled down completely to the ground GND. When the second switch HVSW1 is switched on, a current e.g., a fixed current from the second current source I1 is allowed to flow through the second electrical path created. The voltage drop across the second resistor R1 is determined to be the product of the current from the second current source I1 and the resistance of the second resistor R1 (i.e., Voltage drop = I1 x R1). In other words, the amount of potential being pulled down at the second node n1 is controlled by the second current source I1, such that the amount of potential being pulled down is the product of I1 and R1. It will be appreciated that the second current source I1 serves as a pull-down component for pulling the second node n1 down to GND. Other examples of a pull-down component may include a simple short or a resistor. Accordingly, the second current source I1 may be replaced by other examples of a pull-down component, such that when the second switch is turned on, the second node n1 will be pulled directly to GND (in the case of a short acting as the pull-down component) or pulled to GND through the resistor (in the case of a resistor acting as the pull-down component).

The reset-level circuit 204 further comprises a third diode D2 and a fourth diode D3 connected in reverse biased between the floating supply VB-VS, with the second node n1 coupled between the diodes D2 and D3. That is, the positive terminals of the third diode D2 and the fourth diode D3 are connected to the second node n1 and VS, respectively. The negative terminals of the third diode D2 and the fourth diode D3 are connected to VB and the second node n1, respectively. The diodes D2 and D3 neither pull the second node n1 up to VB nor pull the second node n1 down to GND. Instead, these two diodes D2 and D3 serve as protection clamps, such that the second node n1 can only swing up to one diode voltage above or below VB or VS, respectively.

The level shifter 200 further comprises a slew filter 214 coupled to the set level circuit 202 and reset-level circuit 204 in the interfacing stage 208. The slew filter 214 is configured to filter the raw set signal and raw reset signal and to provide a filtered set signal and a filtered reset signal, such that pulses which are simultaneously provided in the raw set signal and raw

reset signal are filtered away. The level shifter 200 further comprises an output latch 216, e.g., Set-Reset latch, coupled to the slew filter 214. The output latch 216 is configured to provide an output logic signal e.g., output voltage in the second supply domain, e.g., to set the output voltage when a pulse is detected in the filtered set signal and to reset the output voltage when a pulse is detected in the filtered reset signal.

The slew filter 214 comprises the first slew filter input terminal S_{raw} coupled to the set-level circuit 202 and configured to receive the raw set signal from the set-level circuit 202; and the second slew filter input terminal R_{raw} coupled to the reset-level circuit 204 and configured to receive the raw reset signal from the reset-level circuit 204. The slew filter 214 further comprises a first slew filter output terminal configured to provide the filtered set signal and a second slew filter output terminal configured to provide the filtered reset signal to the output latch 216.

The output latch 216 comprises a first latch input terminal S coupled to the first slew filter output terminal and configured to receive the filtered set signal from the first slew filter output terminal; and a second latch input terminal R coupled to the second slew filter output terminal and configured to receive the filtered reset signal from the second slew filter output terminal. The output latch 216 further comprises a first latch output terminal Q configured to provide an output Out_fl. The filtered set signal is configured to change (or set) the output Out_fl from logic low to logic high. The filtered reset signal is configured to change (or reset) the output Out_fl from logic high to logic low. The output latch 216 further comprises a second latch output terminal Qb configured to provide an output Outb_fl, which is dependent on and complementary to the output Out_fl. For example, Out_fl may be VS voltage level, and Outb_fl may be VB voltage level.

In the example embodiment, the level shifter 200 functions to shift the input logic signal ***In*** from the input VDD-GND supply domain to the floating VB-VS supply domain. The floating supply may swing up with VS >> VDD, and down with VB > GND > VS. In other words, VS may go negative with respect to GND. In addition, the floating supply may swing with a slew rate of up to 500ps, resulting in common-mode glitches generated on both the first node n0 and the second node n1 due to their RC (resistive and capacitive) components. In the example embodiment, the slew filter 214 is able to filter out both common-mode glitches generated on the first node n0 and the second node n1, thereby preventing the output latch from being erroneously corrupted when the floating supply slews.

During operation of the level shifter 200, it is assumed that initially, the input logic signal ***In*** is low, such that the output Out_fl is also latched to low. The level shifter 200 is idle, as both the first switch HVSW0 and second switch HVSW1 are switched off, and both the first node n0 and the second node n1 are pulled to VB by the first resistor R0 of the first pull-up circuit and the second resistor R1 of the second pull-up circuit, respectively. The output latch e.g., SR latch 216 receives logic low for both its inputs at the first latch input terminal S and second latch input terminal R.

When the input logic signal ***In*** changes from low to high, the positive edge pulse generator 210 detects the rising edge in the input logic signal ***In*** and generates a pulse to switch on the first switch HVSW0 momentarily. Accordingly, the first node n0 is pulled down and trips the first inverter INV0. While the first node n0 is being pulled down, the first inverter INV0 will output logic high, and remains high. After the first switch HVSW0 switches off at the end of the period for which it is configured to be switched on (i.e., the pulse width of the pulse generated by the edge pulse generator), the first electrical path (i.e., pull-down electrical path) is disconnected, and the first resistor R0 of the first pull-up circuit pulls the first node n0 back to VB and the first inverter INV0 will output logic low, thereby completing a set pulse. The set pulse (i.e., a pulse in the raw set signal) generated by the first inverter INV0 will be buffered by the slew filter 214 and thereafter sets the output latch 216, completing the level shifter operation. It will be appreciated that the pulse generated by the positive edge pulse generator 210 to switch on the first switch HVSW0 momentarily, is configured such that the period for which the first switch HVSW0 is activated (or switched on), is sufficient to effectively pull-down the first node n0 such that a desired output logic state (of e.g., VB voltage level) is obtained or output at Out_fl, and a complementary output logic state (of e.g., VS voltage level) is obtained or output at Outb_fl.

When the input logic signal ***In*** changes from high to low, the same occur for the corresponding path of the negative edge pulse generator 212, the second switch HVSW1, the second node n1, the second resistor R1, the second inverter INV1, the slew filter 214 and the output latch 216. That is, when the input logic signal ***In*** changes from high to low, the negative edge pulse generator 212 detects the falling edge in the input logic signal ***In*** and generates a pulse to switch on the second switch HVSW1 momentarily. Accordingly, the second node n1 is pulled down and trips the second inverter INV1. While the second node n1 is being pulled down, the second inverter INV1 will output logic high, and remains high. After the second switch HVSW1 switches off at the end of the period for which it is configured to be switched on (i.e., the pulse width of the pulse generated by the edge pulse generator), the second

electrical path (i.e., pull-down electrical path) is disconnected, and the second resistor R1 of the second pull-up circuit pulls the second node n1 back to VB and the second inverter INV1 will output logic low, thereby completing a reset pulse. The reset pulse (i.e., a pulse in the raw reset signal) generated by the second inverter INV1 will be buffered by the slew filter 214 and thereafter resets the output latch 216, completing the level shifter operation. It will be appreciated that the pulse generated by the negative edge pulse generator 212 to switch on the second switch HVSW1 momentarily, is configured such that the period for which the second switch is activated (or switched on), is sufficient to effectively pull-down the second node n1 such that a desired output logic state (of e.g., VS voltage level) is obtained or output at Out_fl, and a complementary output logic state (of e.g., VB voltage level) is obtained or output at Outb_fl.

In the example embodiment, the pulsed nature of the level shifter 200 advantageously allows it to reduce its power consumption.

When VB-VS floating supply slews up, common-mode glitch pulses will be generated on both the first node n0 and the second node n1 due to their RC components. Hence, both the first inverter INV0 and the second inverter INV1 will generate and feed pulses to the slew filter 214. The slew filter 214 uses the presence of both set and reset pulses to block both pulses from propagating to the output latch 216 using digital logics, thereby preventing the corruption of the output latch 216.

When VB-VS floating supply slews down, both the first node n0 and the second node n1 go above VB and get clamped by the first diode D0 of the set level circuit 202 and the third diode D2 of the reset level circuit 204, respectively. When VB-VS floating supply slews down, the first inverter INV0 and the second inverter INV1 do not trip, and no glitch pulses are generated.

It will be appreciated that architecture and operations of pulse generators and set-reset latches are known to a person skilled in the art and are therefore not described in further detail for brevity. It will also be appreciated that the pulse generators (e.g., 210, 212), slew filter (e.g., 214) and output latch (e.g., 216) may be implemented with different combinations of logic gates, which collectively provide the desired output logic state whilst achieving the slew filtering function described herein. For example, the circuit (326) as shown in FIG. 3D may be implemented for the slew filter (214) of the level shifter (200). Alternatively, a set-reset latch may be implemented for the slew filter (214) of the level shifter (200).

FIG. 3A is a circuit diagram of a level shifter 300 for shifting an input logic signal (e.g., input logic signal ***In***) from a first supply/voltage domain (e.g., VDD-GND supply domain) to a second supply/voltage domain (e.g., floating VB-VS supply domain) in another example embodiment.

The level shifter 300 comprises a set-level circuit 302 configured to provide a pulse in a raw set signal in the second supply domain when a rising edge, e.g., rising pulse edge is detected in the input logic signal ***In*** in the first supply domain and a reset-level circuit 304 configured to provide a pulse in a raw reset signal in the second supply domain when a falling edge, e.g., falling pulse edge is detected in the input logic signal ***In*** in the first supply domain. The set-level circuit 302 and reset-level circuit 304 are comprised in an input stage 306 and an interfacing stage 308 as shown in FIG. 3A. It will be appreciated that the components of the input stage 306 are in the first supply domain and the components of the interfacing stage 308 are in the second supply domain. It will further be appreciated that the set-level circuit 302 and the reset-level circuit 304 of FIG. 3A function substantially similarly to the set-level circuit 202 and the reset-level circuit 204 of FIG. 2.

The level shifter 300 of FIG. 3A differs from the level shifter 200 of FIG. 2 by further comprising a replica/ reference-level circuit 318. The reference-level circuit 318 is configured to generate a reference signal for a slew filter. The reference-level circuit is configured to replicate the configuration of the set- and reset-level circuits 302, 304, such that common-mode glitches occurring at a first node n0 and a second node n1 of the set and reset-level circuits 302, 304 are also captured at the reference-level circuit 318.

As shown in FIG. 3A, the reference-level circuit 318 comprises components in the input stage 306 and the interfacing stage 308. The reference-level circuit 318 comprises a third inverter INV2 coupled to a third pull-up circuit and a third pull-down circuit. The third inverter INV2 comprises a third inverter output terminal coupled to a third slew filter input terminal Ref; and a third inverter input terminal coupled to the third pull-up circuit and the third pull down circuit at a third node n2.

The third pull-up circuit is configured to pull up the potential of the third node n2 and maintain the third node n2 in a pulled-up state when the third pull-down circuit is not in operation. In the example embodiment, the third pull-up circuit comprises a third resistor R2 coupled between the third node n2 and the floating supply VB.

The third pull-down circuit comprises a third switch e.g., high voltage switch HVSW2 disposed between the third node n2 and the ground GND in the first supply domain, and a third current source I2 disposed between the third switch HVSW2 and the ground GND in the first supply domain. The third switch HVSW2 and the third current source I2 are connected in series between the third node n2 to the ground GND. The third pull-down circuit is configured to pull down the third node n2 when the third switch HVSW2 is activated, said activation of the third switch providing a third electrical path between the third current source I2 and the third node n2. The third electrical path allows the potential at the third node n2 to be pulled down. The third switch HVSW2 is configured to be perpetually off/inactivated by default.

It will be appreciated that the third current source I2 serves as a pull-down component for pulling the third node n2 down to GND. Other examples of a pull-down component may include a simple short or a resistor. Accordingly, the third current source I2 may be replaced by other examples of a pull-down component, such that the third node n2 will be pulled directly to GND (in the case of a short acting as the pull-down component) or pulled to GND through the resistor (in the case of a resistor acting as the pull-down component).

The reference-level circuit 318 further comprises a fifth diode D4 and a sixth diode D5 connected in reverse biased between the floating supply VB-VS, with the third node n2 coupled between the diodes D4 and D5. That is, the positive terminals of the fifth diode D4 and the sixth diode D5 are connected to the third node n2 and VS, respectively. The negative terminals of the fifth diode D4 and the sixth diode D5 are connected to VB and the third node n2, respectively. The diodes D4 and D5 neither pull the third node n2 up to VB nor pull the third node n2 down to GND. Instead, these two diodes D4 and D5 serve as protection clamps, such that the third node n2 can only swing up to one diode voltage above or below VB or VS, respectively.

In the example embodiment, the circuit components in the reference-level circuit are configured to match the circuit components of the set-level circuit 302 and reset-level circuit 304, such that there is matching between the nodes n0, n1, and n2. Hence, the same circuit components are connected to the third node n2 when compared to the first node n0 and the second node n1. It will be appreciated that matching is needed such that all the nodes n0, n1, and n2 will behave in the same manner when the floating VB-VS supply slews. Since the reference-level circuit does not participate in the normal operation of the logic level shifting

(i.e., normal operation of level shifting is through the set-level circuit 302 and the reset-level circuit 304), the third switch HVSW2 does not need to be turned on.

The level shifter 300 further comprises a slew filter 314 coupled to the set level circuit 302, reset-level circuit 304, and reference-level circuit 318 in the interfacing stage 308, and an output latch 316, e.g., SR latch, coupled to the slew filter 314.

The slew filter 314 is configured to filter the raw set signal and raw reset signal and to provide a filtered set signal and a filtered reset signal, such that pulses which are simultaneously provided in the raw set signal and raw reset signal are filtered away. The slew filter 314 comprises a first slew filter input terminal S_{raw} coupled to the set-level circuit 302 and configured to receive the raw set signal from the set-level circuit 302; and a second slew filter input terminal R_{raw} coupled to the reset-level circuit 304 and configured to receive the raw reset signal from the reset-level circuit 304. The slew filter 314 further comprises a first slew filter output terminal configured to provide the filtered set signal and a second slew filter output terminal configured to provide the filtered reset signal to the output latch 316.

The slew filter 314 differs from the slew filter 214 of FIG. 2 by further comprising the third slew filter input terminal Ref configured to receive the reference signal from the reference-level circuit 318. The slew filter 314 is configured to utilize the reference signal to filter out common-mode glitches in the raw set and reset signals generated on the set-level and reset-level circuits. That is, the slew filter 314 is configured to utilize the presence of the reference signal in place of the presence of pulses simultaneously provided in the raw set signal and raw reset signal as the condition to filter out common-mode glitches in the raw set and reset signals generated on the set-level and reset-level circuits. In other words, instead of using the main signal paths provided by the set- and reset-level circuits as the condition for filtering the glitches, the reference-level circuit 318 is used to generate a reference signal for the slew filter 314. The slew filter 314 may be constructed using simple digital logic gates to utilise the reference signal to block the raw set and reset signals. For example, the slew filter 314 may be constructed using AND gates whereby the reference signal is the qualifying signal. Since the reference signal path is only used for filtering glitches, and not for the main level shifting operation, the third switch HVSW2 is never switched on to pull down the third node n2.

The output latch 316 is configured to set an output voltage when a pulse is detected in the filtered set signal and to reset the output voltage when a pulse is detected in the filtered reset signal.

During operation, the level shifter 300 performs its level shifting operation in substantially the same manner as the level shifter 200 of FIG. 2. That is, when the input logic signal ***In*** changes from low to high and from high to low, the set-level circuit 302 and reset-level circuit 304 provides the level shifting operation in substantially the same manner as the level shifter 200 of FIG. 2.

During operation, when the floating supply VB-VS slews, glitches, e.g., common-mode glitches will be generated on the first node n0 and the second node n1 due to their RC components. Hence, both the first inverter INV0 and the second inverter INV1 will generate and feed pulses to the slew filter 314. In addition to the common-mode glitches on the first node n0 and the second node n1, the third node n2 in the replica circuit 318 will also generate the same glitch when the floating supply VB-VS slews, since the same circuit components are used to build the third node n2. Accordingly, the third inverter INV2 also generates and feeds a pulse to the slew filter 314 due to the glitch at the third node n2. Therefore, instead of using the presence of glitches on the main signal paths of the first node n0 and the second node n1, the slew filter 314 uses the presence of the glitch in the reference signal to filter/block both the raw set and reset signals. In other words, the filtering condition for the slew filter 314 is not based on the presence of both raw set and raw reset signals. Rather, the primary filtering condition for the slew filter 314 is based on the presence of the reference signal. It will be appreciated that in the example embodiment, common-mode glitches are still simultaneously provided at the raw set and reset signals, but their simultaneous presence is not the primary filtering condition for filtering by the slew filter 314. In the example embodiment, the filtering condition based on the simultaneous presence of glitches in the raw set and reset signals is secondary and optional.

One advantage of using the reference signal path is that it ensures both the set and reset signal paths are filtered with matching characteristics. Another advantage of using the reference signal path instead of the main signal paths, is that the RC components of the reference signal path at the third node n2 can be designed to glitch more readily as compared to the main signal paths at the first node n0 and the second node n1. Therefore, this may ensure that glitches on the first node n0 and the second node n1 are guaranteed to be filtered and reduces the importance of matching between the first node n0 and the second node n1. In other words, although it is mentioned above that the third node n2 should be matched with the first node n0 and the second node n1, a designed mismatch can be included into the third node n2 such that the third node n2 glitches more readily.

FIG. 3B to FIG. 3E show examples of circuit configurations that are suitable for implementing the slew filter 314. FIG. 3B is a circuit diagram of a gated set-reset latch (gated SR latch) 322 in an example embodiment. The gated SR latch 322 is configured to perform filtering based on both the reference signal and the pulses which are simultaneously provided in the raw set and reset signals. FIG. 3C is a circuit diagram of a (non-SR latch) circuit 324 for slew filtering based on the reference signal in an example embodiment. The circuit 324 is configured to perform filtering based on the reference signal only. FIG. 3D is a circuit diagram of a (non-SR latch) circuit 326 for slew filtering based on pulses which are simultaneously provided in the raw set and reset signals in an example embodiment. That is, the primary filtering condition in FIG. 3D is the presence of pulses which are simultaneously provided in the raw set and reset signals. FIG. 3E is a circuit diagram of a (non-SR latch) circuit 328 for slew filtering based on both the reference signal and the pulses which are simultaneously provided in the raw set and reset signals in an example embodiment.

FIG. 4 is a circuit diagram of a level shifter 400 for shifting an input logic signal (e.g., input logic signal ***In***) from a first supply/voltage domain (e.g., input VDD-GND supply domain) to a second supply/voltage domain (e.g., floating VB-VS supply domain) in yet another example embodiment.

The level shifter 400 comprises a set-level circuit 402 configured to provide a pulse in a raw set signal in the second supply domain when a rising edge, e.g., rising pulse edge is detected in the input logic signal ***In*** in the first supply domain and a reset-level circuit 404 configured to provide a pulse in a raw reset signal in the second supply domain when a falling edge, e.g., falling pulse edge is detected in the input logic signal ***In*** in the first supply domain. The level shifter 400 further comprises a reference-level circuit 418 configured to replicate the configuration of the set- and reset-level circuits 402, 404. The set-level circuit 402, reset-level circuit 404 and reference-level circuit 418 are comprised in an input stage 406 and an interfacing stage 408 as shown in FIG. 4. The level shifter 400 further comprises a slew filter 414 coupled to the set level circuit 402, reset-level circuit 404, reference-level circuit 418 and an output latch 416, e.g., SR (Set-Reset) latch, coupled to the slew filter 414. The set-level circuit 402, reset-level circuit 404, reference-level circuit 418, slew filter 414, and output latch 416 function substantially similarly to the set-level circuit 302, reset-level circuit 304, reference-level circuit 318, slew filter 314, and output latch 316 of FIG. 3A.

The level shifter 400 of FIG. 4 differs from the level shifter 300 of FIG. 3A by further comprising a refresh block 420 configured to detect an occurrence of slew in the second supply domain and to adapt the input logic signal ***In*** in the first supply domain accordingly, based on the detection such that the input logic signal ***In*** that occurs during the slew is not lost and is able to propagate to the output latch 416. Accordingly, the refresh block 420 may be configured to generate an additional refresh input logic signal to the set-level circuit 402 and reset-level circuit 404 in the first supply domain when the occurrence of slew is detected. In the example embodiment, the refresh block 420 is coupled to an input terminal of a first pulse generator 410, e.g., a positive edge pulse generator (compare 210 of FIG. 2), and an input terminal of a second pulse generator 412, e.g., a negative edge pulse generator (compare 212 of FIG. 2), such that the input logic signal ***In*** passes through the refresh block 420 prior to entering the first pulse generator 410 and the second pulse generator 412. The refresh block 420 further comprises a sense terminal coupled to the floating supply VB-VS to detect the occurrence of slew in the floating supply.

During slew filtering, both the set and reset signals are blocked to prevent them from erroneously corrupting the output latch 416. This period where both set and reset signals are blocked is a dead window for the level shifter 400 as the input logic signal ***In*** is unable to propagate through. Here, the refresh block 420 is added to detect the occurrence of VS (floating supply) slew and generate an additional refresh input logic signal after the VS slew. Specifically, the refresh block 420 buffers the input logic signal ***In*** to the level shifter 400 (where the first pulse generator 410 and second pulse generator 412 as part of the set-level circuit 402 and reset-level circuit 404 receives it) in normal operation and the floating supply is not slewing. The refresh block 420 generates an additional refresh input logic signal to the level shifter 400 if it detects a slew in the floating supply, such that input logic signal ***In*** that occurs during this dead window is not lost and is able to propagate to the output latch. Advantageously, this ensures that the input logic signal ***In*** is not lost if it changes during the dead window.

It would be appreciated that the refresh block 420 may also be implemented in the level shifter 200 of FIG. 2, i.e., without the reference-level circuit.

FIG. 5 is a circuit diagram of a level shifter 500 for shifting an input logic signal (e.g., input logic signal ***In***) from a first supply/voltage domain (e.g., input VDD-GND supply domain) to a second supply/voltage domain (e.g., floating VB-VS supply domain) in an alternative example embodiment.

The level shifter 500 comprises a set-level circuit 502 configured to provide a pulse in a raw set signal in the second supply domain when a rising edge, e.g., rising pulse edge is detected in the input logic signal ***In*** in the first supply domain and a reset-level circuit 504 configured to provide a pulse in a raw reset signal in the second supply domain when a falling edge, e.g., falling pulse edge is detected in the input logic signal ***In*** in the first supply domain. The set-level circuit 502 and reset-level circuit 504 are comprised in an input stage 506 and an interfacing stage 508 as shown in FIG. 5. It will be appreciated that the components of the input stage 506 are in the first supply domain and the components of the interfacing stage 508 are in the second supply domain.

The set-level circuit 502 comprises a first inverter INV0, e.g., high threshold voltage inverter $V_{th,inv}$, in the second supply domain coupled to a first pull-up circuit and a first pull-down circuit. The first inverter INV0 comprises a first inverter output terminal coupled to a first slew filter input terminal S_{raw}. The first inverter INV0 further comprises a first inverter input terminal coupled to a first pull-up circuit and a first pull-down circuit at a first node n0.

The first pull-up circuit is configured to pull up the first node n0 and maintain the first node n0 in a pulled-up state, when the first pull-down circuit is not in operation. In the example embodiment, the first pull-up circuit comprises a first resistor R0 coupled between the first node n0 and the floating supply VB.

The first pull-down circuit is configured to pull down the potential of the first node n0 momentarily, when a rising edge is detected in the input logic signal ***In***, such that the first inverter output terminal is configured to output the pulse in the raw set signal to the first slew filter input terminal S_{raw} when the first node n0 is pulled down. The first pull-down circuit comprises a first capacitive circuit comprising a first pulse generator 510 and a first capacitor C0 coupled to the first pulse generator 510 in the first supply domain. The first pulse generator 510 e.g., a positive edge pulse generator in the first supply domain is configured to generate a first pulse in response to rising edges in the input logic signal ***In***. The first pulse generator 510 comprises a first pulse generator input for receiving the input logic signal ***In*** and a first pulse generator output for outputting the first pulse. The first capacitor C0 is configured to pull down the first node n0 momentarily by the first pulse. The first capacitor C0 comprises a bottom plate coupled to the first pulse generator output and a top plate coupled to the first node n0.

The set-level circuit 502 further comprises a first diode D0 and a second diode D1 connected in reverse biased between the floating supply VB-VS, with the first node n0 coupled between the diodes D0 and D1. That is, the positive terminals of the first diode D0 and the second diode D1 are connected to the first node n0 and VS, respectively. The negative terminals of the first diode D0 and the second diode D1 are connected to VB and the first node n0, respectively. The diodes D0 and D1 neither pull the first node n0 up to VB nor pull the first node n0 down to GND. Instead, these two diodes D0 and D1 serve as protection clamps, such that the first node n0 can only swing up to one diode voltage above or below VB or VS, respectively.

The reset-level circuit 504 comprises a second inverter INV1, e.g., high threshold voltage inverter $V_{th,inv}$, in the second voltage domain coupled to a second pull-up circuit and a second pull-down circuit. The second inverter INV1 comprises a second inverter output terminal coupled to a second slew filter input terminal R_{raw}. The second inverter INV1 further comprises a second inverter input terminal coupled to the second pull-up circuit and the second pull-down circuit at a second node n1.

The second pull-up circuit is configured to pull up the potential of the second node n1 and maintain the second node n1 in a pulled-up state when the second pull-down circuit is not in operation. In the example embodiment, the second pull-up circuit comprises a second resistor R1 coupled between the second node n1 and the floating supply VB.

The second pull-down circuit is configured to pull down the potential of the second node n1 momentarily, when the falling edge is detected in the input logic signal ***In***, such that the second inverter output terminal is configured to output the pulse in the raw reset signal to the second slew filter input terminal R_{raw} when the second node n1 is pulled down. The second pull-down circuit comprises a second capacitive circuit comprising a second pulse generator 512 and a second capacitor C1 coupled to the second pulse generator 512 in the first supply domain. The second pulse generator 512 e.g., a negative edge pulse generator in the first supply domain is configured to generate a second pulse in response to falling edges in the input logic signal ***In***. The second pulse generator 512 comprises a second pulse generator input for receiving the input logic signal ***In*** and a second pulse generator output for outputting the second pulse. The second capacitor C1 is configured to pull down the second node n1 momentarily by the second pulse. The second capacitor C1 comprises a bottom plate coupled to the second pulse generator output and a top plate coupled to the second node n1.

The reset-level circuit 504 further comprises a third diode D2 and a fourth diode D3 connected in reverse biased between the floating supply VB-VS, with the second node n1 coupled between the diodes D2 and D3. That is, the positive terminals of the third diode D2 and the fourth diode D3 are connected to the second node n1 and VS, respectively. The negative terminals of the third diode D2 and the fourth diode D3 are connected to VB and the second node n1, respectively. The diodes D2 and D3 neither pull the second node n1 up to VB nor pull the second node n1 down to GND. Instead, these two diodes D2 and D3 serve as protection clamps, such that the second node n1 can only swing up to one diode voltage above or below VB or VS, respectively.

The level shifter 500 further comprises a slew filter 514 coupled to the set level circuit 502 and reset-level circuit 504 in the interfacing stage 508. The slew filter 514 is configured to filter the raw set signal and raw reset signal and to provide a filtered set signal and a filtered reset signal, such that pulses which are simultaneously provided in the raw set signal and raw reset signal are filtered away. The level shifter 500 further comprises an output latch 516, e.g., SR (Set-Reset) latch, coupled to the slew filter 514. The output latch 516 is configured to provide an output logic signal e.g., output voltage in the second supply domain, e.g., to set the output voltage when a pulse is detected in the filtered set signal and to reset the output voltage when a pulse is detected in the filtered reset signal.

The slew filter 514 comprises the first slew filter input terminal S_{raw} coupled to the set-level circuit 502 and configured to receive the raw set signal from the set-level circuit 502; and the second slew filter input terminal R_{raw} coupled to the reset-level circuit 504 and configured to receive the raw reset signal from the reset-level circuit 504. The slew filter 514 further comprises a first slew filter output terminal configured to provide the filtered set signal and a second slew filter output terminal configured to provide the filtered reset signal to the output latch 516.

The output latch 516 comprises a first latch input terminal S coupled to the first slew filter output terminal and configured to receive the filtered set signal from the first slew filter output terminal; and a second latch input terminal R coupled to the second slew filter output terminal and configured to receive the filtered reset signal from the second slew filter output terminal. The output latch 516 further comprises a first latch output terminal Q configured to provide an output Out_fl. The filtered set signal is configured to change (or set) the output Out_fl from logic low to logic high. The filtered reset signal is configured to change (or reset) the output Out_fl from logic high to logic low. The output latch 516 further comprises a second

latch output terminal Qb configured to provide an output Outb_fl, which is dependent on and complementary to the output Out_fl. For example, Out_fl may be VS voltage level, and Outb_fl may be VB voltage level.

The level shifter 500 of FIG. 5 is a capacitive version of a level shifter and differs from the level shifters of FIGS. 2 to 4 in that high voltage capacitors C0 and C1 are used to replace the high voltage switches and their current sources, namely the pairs of HVSW0 and I0 and HVSW1 and I1, respectively.

During operation of the level shifter 500, it is assumed that initially, the input logic signal ***In*** is low, such that the output Out_fl is also latched to low. The level shifter is idle, as both the first node n0 and the second node n1 are pulled to VB by the first resistor R0 of the first pull-up circuit and the second resistor R1 of the second pull-up circuit, respectively, and the bottom plates of the first capacitor C0 and the second capacitor C1 are pulled to VDD by their respective pulse generators. The output SR latch 516 receives logic low for both its inputs at the first latch input terminal S and second latch input terminal R.

When the input logic signal ***In*** changes from low to high, the positive edge pulse generator 510 detects the rising edge in the input logic signal ***In*** and generates a pulse to pull down the bottom plate of the first capacitor C0 momentarily. The first capacitor C0 maintains the voltage difference across itself, therefore pulling down the first node n0 to trip the first inverter INV0. The first inverter INV0 thus generates a set pulse (i.e., a pulse in the set signal) that will be buffered by the slew filter 514 and thereafter sets the output latch 516, completing the level shifter operation. After the pulse, the first resistor R0 pulls the first node n0 back to VB, and the positive edge pulse generator 510 pulls the bottom plate of the first capacitor C0 back to VDD.

When the input logic signal ***In*** changes from high to low, the same occur for the corresponding path of negative edge pulse generator 512, the second capacitor C1, the second node n1, the second resistor R1, the second inverter INV1, slew filter 514 and the output latch 516. That is, when the input logic signal ***In*** changes from high to low, the negative edge pulse generator 512 detects the falling edge in the input logic signal ***In*** and generates a pulse to pull down the bottom plate of the second capacitor C1 momentarily. The second capacitor C1 maintains the voltage difference across itself, therefore pulling down the second node n1 to trip the second inverter INV1. The second inverter INV1 thus generates a reset pulse (i.e., a pulse in the reset signal) that will be buffered by the slew filter 514 and thereafter

resets the output latch 516, completing the level shifter operation. After the pulse, the second resistor R1 pulls the second node n1 back to VB, and the negative edge pulse generator 512 pulls the bottom plate of the second capacitor C1 back to VDD.

In the example embodiment, the capacitive and pulsed nature of the level shifter 500 allow it to reduce its power consumption.

The slew filter 514 in the level shifter 500 of FIG. 5 works the same way as the level shifter 200 of FIG. 2. When VB-VS floating supply slews up, the slew filter 514 uses the presence of both set and reset common-mode glitch pulses to block these glitches from propagating to the output latch 516. Digital logic circuitry in the form of e.g., simple logic gates such as AND gates or SR latch may be employed to implement the filtering, thereby preventing the output latch 516 from being corrupted.

When VB-VS floating supply slews down, both the first node n0 and the second node n1 go above VB and get clamped by the first diode D0 of the set level circuit 502 and the third diode D2 of the reset level circuit 504, respectively. The first inverter INV0 and second inverter INV1 do not trip, and no glitch pulses are generated.

It will be appreciated that the reference level circuit 318 of the embodiment illustrated in FIG. 3A and the refresh block 420 of the embodiment illustrated in FIG. 4 may also be implemented in the embodiment of FIG. 5.

It will be appreciated that architecture and operations of pulse generators and set-reset latches are known to a person skilled in the art and are therefore not described in further detail for brevity. It will also be appreciated that the pulse generators (e.g., 510, 512), slew filter (e.g., 514) and output latch (e.g., 516) may be implemented with different combinations of logic gates, which collectively provide the desired output logic state whilst achieving the slew filtering and output latch function described herein. For example, the circuit 326 as shown in FIG. 3D may be implemented for the slew filter 514 of the level shifter 500. Alternatively, a set-reset latch may be implemented for the slew filter 514 of the level shifter 500.

It will be appreciated that variations of the embodiments described herein may be used to implement a shift up level shifter. For example, in a variant of the level shifter 500 as a shift up level shifter, at the first node n0 and second node n1, the first resistor R0 and second resistor R1 can be connected to VS instead of VB. All other logics can be reconfigured in a

complementary manner in the variant shift up level shifter 500. That is, the resistors R0 and R1 may be reconfigured as the pull-down circuitries to VS, while the capacitors C0 and C1 and the pulse generators may be reconfigured as the pull up circuitries. During operation of the shift up level shifter, the pulses generated will momentarily pull the first node n0 and the second node n1 up to VB. It will be appreciated that the first inverter INV0 and second inverter INV1 also need to be complementary, i.e., instead of being inverters, buffers are used to buffer the positive pulse generated by the action of momentarily pulling up the first node n0 / the second node n1 up to VB.

It will further be appreciated that the embodiments described herein may be reconfigured to implement a shift down level shifter. For variants regarding shift down level shifter, all circuit components as described in FIG. 2 to FIG. 5 can be connected appropriately with the same concept, such that a shift down level shifter is achieved. Using the level shifter 500 of FIG. 5 as an example, the input stage 506 will be connected to the floating VB-VS supply, while the interfacing stage 508, slew filter 514, and output latch 516 will be connected to the VDD-GND supply. When the level shifter 500 is in an idle state, the top plate of the first capacitor C0 / second capacitor C1 will be pulled to VB by their respective pulse generators, while the first node n0 / second node n1 will be pulled to VDD by the first resistor R0 / second resistor R1.

FIG. 6 is a schematic flow chart 600 for illustrating a method of shifting an input logic signal from a first supply domain to a second supply domain in an example embodiment. At step 602, the input logic signal is received. At step 604a, a pulse is provided in a raw set signal in the second supply domain using a set-level circuit, when a rising edge is detected in the input logic signal in the first supply domain. At step 604b, a pulse is provided in a raw reset signal in the second supply domain using a reset-level circuit, when a falling edge is detected in the input logic signal in the first supply domain. At step 606, the raw set signal and raw reset signal are filtered to provide a filtered set signal and a filtered reset signal using a slew filter, such that pulses which are simultaneously provided in the raw set signal and raw reset signal are filtered away. At step 608, an output voltage is set from a latch output when a pulse is detected in the filtered set signal and the output voltage is reset from the latch output when a pulse is detected in the filtered reset signal.

In the example embodiment, the method may further comprise pulling up a first node of the set-level circuit and maintaining the first node in a pulled-up state using a first pull-up circuit; and pulling up a second node of the reset-level circuit and maintaining the second node

in a pulled-up state using a second pull-up circuit. In the example embodiment, the method may further comprise generating a first pulse from a first pulse generator in response to rising edges in the input logic signal; pulling down the first node of the set-level circuit momentarily by the first pulse; and outputting the pulse in the raw set signal when the first node is pulled down. In the example embodiment, the method may further comprise generating a second pulse from a second pulse generator in response to falling edges in the input logic signal; pulling down the second node of the reset-level circuit momentarily by the second pulse; and outputting the pulse in the raw reset signal when the second node is pulled down.

In the example embodiment, the method may alternatively further comprise pulling down a first node of the set-level circuit and maintaining the first node in a pulled-down state using a first pull-down circuit; and pulling down a second node of the reset-level circuit and maintaining the second node in a pulled-down state using a second pull-down circuit. In the example embodiment, the method may alternatively further comprise generating a first pulse from a first pulse generator in response to rising edges in the input logic signal; pulling up the first node of the set-level circuit momentarily by the first pulse; and outputting the pulse in the raw set signal when the first node is pulled up. In the example embodiment, the method may alternatively further comprise generating a second pulse from a second pulse generator in response to falling edges in the input logic signal; pulling up the second node of the reset-level circuit momentarily by the second pulse; and outputting the pulse in the raw reset signal when the second node is pulled up.

In the example embodiment, the method may further comprise utilizing the presence of pulses simultaneously provided in the raw set signal and raw reset signal to the slew filter as the condition to filter out common-mode glitches in the raw set and reset signals generated on the set-level and reset-level circuits. In the example embodiment, the method may further comprise, generating a reference signal for the slew filter using a reference-level circuit, the reference-level circuit configured to replicate the configuration of the set- and reset-level circuits, such that common-mode glitches at the set and reset-level circuits are also captured at the reference-level circuit; and utilizing the reference signal as the condition to filter out common-mode glitches in the raw set and reset signals generated on the set- and reset-level circuits. In the example embodiment, the method may further comprise detecting an occurrence of slew of the second supply domain using a refresh block; and generating an additional refresh input to the first supply domain after the occurrence of slew such that the input logic signal that occurs during the slew is not lost and is able to propagate to the output latch.

In the described example embodiments, the level shifter and method thereof employ a slew filter to block both the set and reset glitches from propagating to the latch when the floating supply slews, thereby, preventing corruption of the latch. Two variations of a high voltage level shifter are described, namely, a switch plus current mirror and a capacitive version. In the described example embodiments, the level shifter and method thereof may advantageously provide reduced power consumption due to its pulsed nature.

The terms "coupled" or "connected" as used in this description are intended to cover both directly connected or connected through one or more intermediate means, unless otherwise stated. Coupling may be used to describe, for example, of two or more objects, devices, and/or components that are communicatively coupled, mechanically coupled, and/or electrically coupled. The term “communicatively coupled” generally refers to any type or configuration of coupling that places two or more objects, devices, components, or portions, elements, or combinations thereof in communication. Mechanical and electrical communications are examples of such communications. The term “mechanically coupled” generally refers to any physical binding, adherence, attachment, and/or other form of physical contact between two or more objects, devices, components, or portions, elements, or combinations thereof. The term “electrically coupled” indicates that one or more objects, devices, components, or portions, elements, or combinations thereof, are in electrical contact such that an electrical signal, pulse, or current (e.g., electrical energy) is capable of passing between the one or more objects, enabling the objects to electrically communicate with one another.

The terms “simultaneous”, “simultaneously”, “at the same time” and the like as used in the description are intended to not be limited to conditions (e.g., an action, an operation, or an event) that start and/or end at the (exact) same time, but also conditions that may not start and/or end at the exact same time, but which takes place during the same time frame.

The description herein may be, in certain portions, explicitly or implicitly described as algorithms and/or functional operations that operate on data within a computer memory or an electronic circuit. These algorithmic descriptions and/or functional operations are usually used by those skilled in the information/data processing arts for efficient description. An algorithm is generally relating to a self-consistent sequence of steps leading to a desired result. The algorithmic steps can include physical manipulations of physical quantities, such as electrical,

magnetic or optical signals capable of being stored, transmitted, transferred, combined, compared, and otherwise manipulated.

Further, unless specifically stated otherwise, and would ordinarily be apparent from the following, a person skilled in the art will appreciate that throughout the present specification, discussions utilizing terms such as “scanning”, “calculating”, “determining”, “replacing”, “generating”, “initializing”, “outputting”, and the like, refer to action and processes of an instructing processor/computer system, or similar electronic circuit/device/component, that manipulates/processes and transforms data represented as physical quantities within the described system into other data similarly represented as physical quantities within the system or other information storage, transmission or display devices etc.

The description also discloses relevant device/apparatus for performing the steps of the described methods. Such apparatus may be specifically constructed for the purposes of the methods.

The example embodiments may also be implemented as hardware modules. A module is a functional hardware unit designed for use with other components or modules. For example, a module may be implemented using digital or discrete electronic components, or it can form a portion of an entire electronic circuit such as an Application Specific Integrated Circuit (ASIC). A person skilled in the art will understand that the example embodiments can also be implemented as a combination of hardware and software modules.

Additionally, when describing some embodiments, the disclosure may have disclosed a method and/or process as a particular sequence of steps. However, unless otherwise required, it will be appreciated the method or process should not be limited to the particular sequence of steps disclosed. Other sequences of steps may be possible. The particular order of the steps disclosed herein should not be construed as undue limitations. Unless otherwise required, a method and/or process disclosed herein should not be limited to the steps being carried out in the order written. The sequence of steps may be varied and still remain within the scope of the disclosure.

Further, in the description herein, the word “substantially” whenever used is understood to include, but not restricted to, "entirely" or “completely” and the like. In addition, terms such as "comprising", "comprise", and the like whenever used, are intended to be non-restricting descriptive language in that they broadly include elements/components recited after

such terms, in addition to other components not explicitly recited. For an example, when “comprising” is used, reference to a “one” feature is also intended to be a reference to “at least one” of that feature. Terms such as “consisting”, “consist”, and the like, may, in the appropriate context, be considered as a subset of terms such as "comprising", "comprise", and the like. Therefore, in embodiments disclosed herein using the terms such as "comprising", "comprise", and the like, it will be appreciated that these embodiments provide teaching for corresponding embodiments using terms such as “consisting”, “consist”, and the like. Further, terms such as "about", "approximately" and the like whenever used, typically means a reasonable variation, for example a variation of +/- 5% of the disclosed value, or a variance of 4% of the disclosed value, or a variance of 3% of the disclosed value, a variance of 2% of the disclosed value or a variance of 1% of the disclosed value.

Furthermore, in the description herein, certain values may be disclosed in a range. The values showing the end points of a range are intended to illustrate a preferred range. Whenever a range has been described, it is intended that the range covers and teaches all possible sub-ranges as well as individual numerical values within that range. That is, the end points of a range should not be interpreted as inflexible limitations. For example, a description of a range of 1% to 5% is intended to have specifically disclosed sub-ranges 1% to 2%, 1% to 3%, 1% to 4%, 2% to 3% etc., as well as individually, values within that range such as 1%, 2%, 3%, 4% and 5%. The intention of the above specific disclosure is applicable to any depth/breadth of a range.

It will be appreciated by a person skilled in the art that other variations and/or modifications may be made to the specific embodiments without departing from the scope of the invention as broadly described. For example, in the description herein, features of different exemplary embodiments may be mixed, combined, interchanged, incorporated, adopted, modified, included etc. or the like across different exemplary embodiments. The present embodiments are, therefore, to be considered in all respects to be illustrative and not restrictive.

CLAIMS

1. A level shifter for shifting an input logic signal from a first supply domain to a second supply domain, the level shifter comprising,

a set-level circuit configured to provide a pulse in a raw set signal in the second supply domain when a rising edge is detected in the input logic signal in the first supply domain;

a reset-level circuit configured to provide a pulse in a raw reset signal in the second supply domain when a falling edge is detected in the input logic signal in the first supply domain;

a slew filter coupled to the set-level and reset-level circuits, the slew filter configured to filter the raw set signal and raw reset signal, to provide a filtered set signal and a filtered reset signal, such that pulses which are simultaneously provided in the raw set signal and raw reset signal are filtered away; and

an output latch configured to set an output voltage when a pulse is detected in the filtered set signal and to reset the output voltage when a pulse is detected in the filtered reset signal.

2. The level shifter according to claim 1, wherein the slew filter is a set-reset latch in the second supply domain.

3. The level shifter according to claim 1 or 2, wherein the output latch is an other set-reset latch in the second supply domain.

4. The level shifter according to any one of claims 1 to 3, wherein the set-level circuit comprises a first inverter in the second supply domain, the first inverter comprising,

a first inverter output terminal coupled to a first slew filter input terminal; and

a first inverter input terminal coupled to

a first pull-up circuit at a first node, said first pull-up circuit configured to pull up the first node and maintain the first node in a pulled-up state; and

a first pull-down circuit at the first node, said first pull-down circuit configured to pull down the first node momentarily, when the rising edge is detected in the input logic signal, such that the first inverter output terminal is configured to output the pulse in the raw set signal to the first slew filter input terminal when the first node is pulled down.

5. The level shifter according to any one of claims 1 to 4, wherein the reset-level circuit comprises a second inverter in the second supply domain, the second inverter comprising,

a second inverter output terminal coupled to a second slew filter input terminal; and

a second inverter input terminal coupled to

a second pull-up circuit at a second node, said second pull-up circuit is configured to pull up the second node and maintain the second node in a pulled-up state; and

a second pull-down circuit at the second node, said second pull-down circuit configured to pull down the second node momentarily, when the falling edge is detected in the input logic signal, such that the second inverter output terminal is configured to output the pulse in the raw reset signal to the second slew filter input terminal when the second node is pulled down.

6. The level shifter according to claim 4, wherein the first pull-down circuit comprises,

a first pulse generator in the first supply domain, said first pulse generator configured to generate a first pulse in response to rising edges in the input logic signal;

a first pull-down component configured to pull down the first node; and

a first switch configured to switch on momentarily by the first pulse, thereby providing a first electrical path between the first pull-down component and the first node, said first electrical path allowing the first node to be pulled down.

7. The level shifter according to claim 5, wherein the second pull-down circuit comprises,

a second pulse generator in the first supply domain, said second pulse generator configured to generate a second pulse in response to falling edges in the input logic signal;

a second pull-down component configured to pull down the second node; and

a second switch configured to switch on momentarily by the second pulse, thereby providing a second electrical path between the second pull-down component and the second node, said second electrical path allowing the second node to be pulled down.

8. The level shifter according to any one of claims 1 to 7, wherein the slew filter is configured to utilize the presence of pulses simultaneously provided in the raw set signal and raw reset signal to the slew filter as the condition to filter out common-mode glitches in the raw set and reset signals generated on the set-level and reset-level circuits.

9. The level shifter according to any one of claims 1 to 7, further comprising a reference-level circuit configured to generate a reference signal for the slew filter, the reference-level circuit configured to replicate the configuration of the set- and reset-level circuits, such that common-mode glitches at the first and second nodes of the set- and reset-level circuits are also captured at the reference-level circuit.

10. The level shifter according to claim 9, wherein the reference-level circuit comprises a third inverter comprising,

a third inverter output terminal coupled to a third slew filter input terminal; and

a third inverter input terminal coupled to

a third pull-up circuit at a third node, said third pull-up circuit is configured to pull up the third node and maintain the third node in a pulled-up state; and

a third pull-down circuit at the third node, said third pull-down circuit configured to pull down the third node when a third switch is activated, said activation of the third switch providing a third electrical path between the third pull-down circuit and the third node.

11. The level shifter according to claim 9 or 10, wherein the slew filter is configured to utilize the reference signal as the condition to filter out common-mode glitches in the raw set and reset signals generated on the set-level and reset-level circuits.

12. The level shifter according to any one of claims 1 to 11, further comprising a refresh block configured to detect an occurrence of slew of the second supply domain and to adapt the input logic signal in the first supply domain accordingly, based on the detection such that the input logic signal that occurs during the slew is not lost and is able to propagate to the output latch.

13. The level shifter according to claim 4, wherein the first pull-down circuit comprises a first capacitive circuit, the first capacitive circuit comprising,

a first pulse generator in the first supply domain, said first pulse generator configured to generate a first pulse in response to rising edges in the input logic signal; and

a first capacitor configured to pull down the first node momentarily by the first pulse.

14. The level shifter according to claim 5, wherein the second pull-down circuit comprises a second capacitive circuit, the second capacitive circuit comprising,

a second pulse generator in the first supply domain, said second pulse generator configured to generate a second pulse in response to falling edges in the input logic signal; and

a second capacitor configured to pull down the second node momentarily by the second pulse.

15. The level shifter according to any one of claims 1 to 3, wherein the set-level circuit comprises a first buffer in the second supply domain, the first buffer comprising,

a first buffer output terminal coupled to a first slew filter input terminal; and

a first buffer input terminal coupled to

a first pull-up circuit at the first node, said first pull-up circuit configured to pull up the first node momentarily, when the rising edge is detected in the input logic signal, such that the first buffer output terminal is configured to output the pulse in the raw set signal to the first slew filter input terminal when the first node is pulled up; and

a first pull-down circuit at the first node, said first pull-down circuit configured to pull down the first node and maintain the first node in a pulled-down state;

wherein the first pull-up circuit comprises a first capacitive circuit, the first capacitive circuit comprising,

a first pulse generator in the first supply domain, said first pulse generator configured to generate a first pulse in response to rising edges in the input logic signal; and

a first capacitor configured to pull up the first node momentarily by the first pulse.

16. The level shifter according to claims 1 to 3 and 15, wherein the reset-level circuit comprises a second buffer in the second supply domain, the second buffer comprising,

a second buffer output terminal coupled to a second slew filter input terminal; and

a second buffer input terminal coupled to

a second pull-up circuit at a second node, said second pull-up circuit configured to pull up the second node momentarily, when the falling edge is detected in the input logic signal, such that the second buffer output terminal is configured to output the pulse in the raw reset signal to the second slew filter input terminal when the second node is pulled up;

a second pull-down circuit at the second node, said second pull-down circuit configured to pull down the second node and maintain the second node in a pulled-down state; and

wherein the second pull-up circuit comprises a second capacitive circuit, the second capacitive circuit comprising,

a second pulse generator in the first supply domain, said second pulse generator configured to generate a second pulse in response to falling edges in the input logic signal; and

a second capacitor configured to pull up the second node momentarily by the second pulse.

17. A method of shifting an input logic signal from a first supply domain to a second supply domain, the method comprising,

receiving the input logic signal;

providing a pulse in a raw set signal in the second supply domain using a set-level circuit, when a rising edge is detected in the input logic signal in the first supply domain;

providing a pulse in a raw reset signal in the second supply domain using a reset-level circuit, when a falling edge is detected in the input logic signal in the first supply domain;

filtering the raw set signal and raw reset signal to provide a filtered set signal and a filtered reset signal using a slew filter, such that pulses which are simultaneously provided in the raw set signal and raw reset signal are filtered away; and

setting an output voltage from a latch output when a pulse is detected in the filtered set signal and resetting the output voltage from the latch output when a pulse is detected in the filtered reset signal.

18. The method according to claim 17, further comprising,

pulling up a first node of the set-level circuit and maintaining the first node in a pulled-up state using a first pull-up circuit; and

pulling up a second node of the reset-level circuit and maintaining the second node in a pulled-up state using a second pull-up circuit.

19. The method according to claim 18, further comprising,

generating a first pulse from a first pulse generator in response to rising edges in the input logic signal;

pulling down the first node of the set-level circuit momentarily by the first pulse; and

outputting the pulse in the raw set signal when the first node is pulled down.

20. The method according to claim 18, further comprising,

generating a second pulse from a second pulse generator in response to falling edges in the input logic signal;

pulling down the second node of the reset-level circuit momentarily by the second pulse; and

outputting the pulse in the raw reset signal when the second node is pulled down.

21. The method according to claim 17, further comprising,

pulling down a first node of the set-level circuit and maintaining the first node in a pulled-down state using a first pull-down circuit; and

pulling down a second node of the reset-level circuit and maintaining the second node in a pulled-down state using a second pull-down circuit.

22. The method according to claim 21, further comprising,

generating a first pulse from a first pulse generator in response to rising edges in the input logic signal;

pulling up the first node of the set-level circuit momentarily by the first pulse; and

outputting the pulse in the raw set signal when the first node is pulled up.

23. The method according to claim 21, further comprising,

generating a second pulse from a second pulse generator in response to falling edges in the input logic signal;

pulling up the second node of the reset-level circuit momentarily by the second pulse; and

outputting the pulse in the raw reset signal when the second node is pulled up.

24. The method according to any one of claims 17 to 23, further comprising utilizing the presence of pulses simultaneously provided in the raw set signal and raw reset signal to the slew filter as the condition to filter out common-mode glitches in the raw set and reset signals generated on the set-level and reset-level circuits.

25. The method according to any one of claims 17 to 23, further comprising,

generating a reference signal for the slew filter using a reference-level circuit, the reference-level circuit configured to replicate the configuration of the set- and reset-level circuits, such that common-mode glitches at the set- and reset-level circuits are also captured at the reference-level circuit; and

utilizing the reference signal as the condition to filter out common-mode glitches in the raw set and reset signals generated on the set- and reset-level circuits.

26. The method according to any one of claims 17 to 25, further comprising,

detecting an occurrence of slew of the second supply domain using a refresh block; and

generating an additional refresh input to the first supply domain after the occurrence of slew such that the input logic signal that occurs during the slew is not lost and is able to propagate to the output latch.