SIT111 - Task 3.3D

This objective was to use a Hardware Description Language (HDL) to design an Arithmetic Logic Unit (ALU). It receives two input values (x and y), decides the operation using control signals, and outputs an output with flags.

I used the ALU.hdl file that was supplied, which included the ALU design specification and pseudocode, for this implementation. It described how control signals would be used to manipulate the inputs and which operation would be chosen.

My method involved breaking the ALU into smaller parts that matched the procedures mentioned in the pseudo code. In order to zero or negate x and y, I used multiplexers (Mux) to conditionally pass inputs based on control signals. For bitwise AND operation, AND gates were applied, and adders (Add16) were used for addition of integers. Another multiplexer selected the right addition/AND output. At last, I put the logic for output negation into practice and set the flags for zero and negative.

I have used these types for chips for its relevant uses,

- Mux16 for conditional selection
- Add16 for 16-bit addition
- And16 for bitwise AND
- Not16 for negation
- Or8Way/Or to set flag

I tried few inputs to test the functionality and it performed the operation correctly. The ALU satisfies the requirements which is asked for.