UNIVERSITY OF GHANA

COLLEGE OF BASIC AND APPLIED SCIENCE

SCHOOL OF PHYSICAL AND APPLIED SCIENCES

DEPARTMENT OF COMPUTER SCIENCE

B.A/BSc FIRST SEMESTER UNIVERSITY EXAMINATIONS: 2016/2017

CSCD211/CSIT203 - COMPUTER HARDWARE & ARCHITECTURE

(3 CREDITS)

EXAMINER: A. DWUMFOUR ABDULLAI

TIME ALLOWED: HOURS

ANSWER QUESTION ONE (1) AND ANY OTHER TWO (2)

SECTION A: ANSWER ALL QUESTIONS IN THIS SECTION

NB: ALL QUESTIONS THAT INVOLVE CALCULATION, YOU ARE REQUIRED TO SHOW ALL STEPS USED IN ARRIVING AT THE FINAL ANSWER

QUESTION 1[10 marks]

a. What design goal would consider SRAM instead of DRAM? **[1 marks]**

b. Explain the term "Power On Self Test" in relation to the computer BIOS. **[2 marks]**

c. Explain the bottleneck associated with the EPROM that made its choice less attractive compared to the EEPROM **[2 marks]**

d. Explain why the DRAM require frequent refresh. **[1 marks]**

e. Describe the program counter (PC) and state its function. **[2 marks]**

f. State the function of the device controller in respect to the operating system. **[2 marks]**

QUESTION 2[12 marks]

a. Given the number of digits in 2^{10}, what is the maximum unsigned decimal number that can be obtained **[1 marks]**

b. Consider a computer with a 16–bit address space. The machine would have 65,536 (64K = 2^{16}) addressable entities. Compute the maximum memory size on the following addressable entities

I. Byte addressable **[1 marks]**

II. 16-bit word addressable **[2 marks]**

III. 32-bit word addressable **[2 marks]**

a. How many bytes are needed to distinctly address 4GB Memory CPU? [**2 marks]**

a. What is the overall speed up of a 16-bit ARM processor if 60% its program instructions run 40% faster? **[3 marks]**

QUESTION 3 [18 marks]

a. Compute 417_{10}-714_{10} in 1's complement and leave your answer in octonary. **[2 marks]**

b. Compute $-98D9_{16}+ 39716_{10}$ in hexadecimal leaving your final answer in octonary **[2 marks]**

c. Compute $11011.101_{2} * 101.111_{2}$ in binary leaving your final in decimal **[3 marks]**

d. Compute the $-11101.110_2 - 100.10_2$ using 1's complement leaving your final answer in hexadecimal. Verify your results using 10's complement **[3 marks]**

a. Compute $1101100000101_2 - 10100011_2 * 110011_2$ using 10's complement leaving your answer in BCD **[3 marks]**

b. Convert -35.75 to its hexadecimal representation in IEEE- 754 floating-point format **[3 marks]**

c. Convert the hexadecimal IEEE format floating point number 0x40200000 to decimal **[3 marks]**

SECTION B: ANSWER ANY TWO (2) QUESTIONS FROM THIS SECTION

QUESTION1 [30 marks]

a) Explain any two mechanisms of evaluating CPU performance **[2 marks]**

b) Suppose that we have two implementations of the same instruction set

architecture. Machine X has a clock cycle time of 50 ns and a CPI of 4.0 for some program, and machine Y has a clock cycle of 65 ns and a CPI of 2.5 for the same program.

i. Which machine is slower? **[4 marks]**

ii. By how much? **[1 mark]**

c)

I. State Amdahl's law and give a generalized expression of the law. **[3 marks]**

II. Three enhancements with the following speedups are proposed for a new machine: Speedup (1) =30, Speedup (2)=20, and Speedup (3) = 15. Assume that for some set of programs, the fraction of use is 25% for enhancement (1), 30% for enhancement (2), and 45% for enhancement (3).

1. If only one enhancement can be implemented, which should be chosen to maximize the speedup? **[5 marks]**

2. If two enhancements can be implemented, which should be chosen, to maximize the speedup **[5 marks]**

d) A compiler designer is trying to decide between two code sequences for a particular machine. The hardware designers have supplied the following facts:

Instruction Class	**Cycle Per Instruction of instruction Class**
X	1
Y	3
Z	4

For a particular high-level language, the compiler writer is considering two sequences that require the following instruction counts:

	Instruction count in million		
Instruction Count	X	Y	Z
a	2	1	2
b	4	3	1

Assume that the machine's clock Cycle time rate is

I. Which code sequence will execute faster according to MIPS? [5 marks]
II. And according to execution time? [5 marks]

QUESTION 2 [30 marks]

a). State De Morgan's Law and show how is applied to three input function

[2 marks]

b) Construct a block diagram of a ripple Look Ahead carry adder which uses Full adders to illustrate the computation of 4-bit binary expression 1011_2+0011_2 indicate the final results output by the adder

[3 marks]

c) Study the circuit diagram below and answer the questions that follow.

i. Derive a logical expression for the function F. [**2 marks]**

ii. Write the minterms and maxterms from the simplified expression **[2 mark]**

iii. Write the SOP and POS in terms of Minterms and Maxterms symbol. **[2 mark]**

d) Given $m_1 m_3 m_3 m_4 m_6 m_7 m_9 m_{10} m_{11} m_{14} m_2 m_{15}$ obtain the Minterms and simplify the SOP using k-map [**8 marks]**

e) Given $F(W,X,Y,Z)=\Sigma m(0,1,2,5,8,9,10),$ obtain the Maxterms and simplify the POS using the K-map [**8 marks]**

f) Simplify the Boolean expression given by the function using rules of Boolean algebra. **[3 marks]**

QUESTION3[30 marks]

A computer system uses 32-bit memory addresses and it has a main memory consisting of 1Gbytes. It has a 4K-byte cache organized in the block-set-associative manner, with 4 blocks per set and 64 bytes per block.

(a) Calculate the number of bits in each of the

I. Word fields of the memory address **[2 marks]**
II. Set field **[2 marks]**
III. Tag field **[2 marks]**

b) Suppose that a computer has a processor with two L1 caches, one for instructions and one for data, and an L2 cache. Let τ be the access time for the two L1 caches. The miss penalties are approximately 15τ for transferring a block from L2 to L1, and 100τ for transferring a block from the main memory to L2. For the purpose of this problem, assume that the hit rates are the same for instructions and data and that the hit rates in the L1 and L2 caches are 0.96 and 0.80, respectively.

I. What fractions of accesses miss in both the L1 and L2 caches, thus requiring access to the main memory? **[3 marks]**
II. What is the average access time as seen by the processor? **[3 marks]**
III. Suppose that the L2 cache has an ideal hit rate of 1. By what factor would this reduce the average memory access time as seen by the processor? **[2 marks]**

c)

i. Explain the term bus in computer architecture and Describe the three main types of buses used by the CPU. **[3 marks]**

I. Explain the principle of locality and differentiate between the two kinds of

locality in relation to the memory hierarchy **[3 marks]**

iii. What is an advantage of a 3-operand ISA over a 2-operand ISA? **[2 mark]**

d)

i. Describe the defining characteristics of an accumulator-style ISA that distinguishes it from Stack-style ISA. **[2 marks]**

II. Given a 32-bit Address Microprocessor with Register –Memory Architecture, which uses one address instructions, write an instruction that evaluate the expression `X=(A+B)*(C+D)`. All operands are residing in memory. **[3 marks]**

II. Explain Datapath and describe the elements of Datapaths

[3 marks]