UNIVERSITY OF GHANA

B.SC INFORMATION TECHNOLOGY, FIRST SEMESTER UNIVERSITY EXAMINATION

S: 2017/2018

CSIT 203: FUNDAMENTALS OF COMPUTER HARDWARE (3 CREDITS)

INSTRUCTION:

*Answer **Question1** and Any other **One** (1) Question*

TIME ALLOWED:

TWO AND A HALF (2½) HOURS

Question1

PART I [25 Marks]

a. Describe any ***two (2)*** storage technologies employed in the design of storage devices in modern computer systems. **[4 Marks]**

b. Explain why SRAM performs faster than the DRAM as two (2) memory technologies and state which design goal will favor the choice of DRAM over SRAM. **[4 Marks]**

c. Describe the main components and their functions of a modern CPU. **[6 Marks]**

d. Describe the bus architecture and explain the types of internal bus of the computer system. **[4 Marks]**

e. Explain the key difference between the PCI interface technology PCI-Express. **[3 Marks]**

f. Explain any two mechanisms used in measuring the Performance of modern CPU. **[4 Marks]**

PART II [35 Marks]

a. Suppose a program (or a program task) takes 1 billion instructions to execute on a processor running at 2 GHz. Suppose also that 50% of the instructions execute in 3 clock cycles, 30% execute in 4 clock cycles, and 20% execute in 5 clock cycles. What is the execution time for the program or task? **[8 Marks]**

b. Compute the value of $3AB_{16} - 435_{10} - 618_{8}$ using 2's complement arithmetic leaving your final answer in decimal. **[6 Marks]**

c. Compute the value of $256.625_{10} + 64.703125_{10}$ in binary and write your final answer in hexadecimal **[4 Marks]**

a. Suppose that we have two implementations of the same instruction set architecture. Machine X has a clock cycle time of 50 ns and a CPI of 4.0 for some program, and machine Y has a clock cycle of 65 ns and a CPI of 2.5 for the same program. Which machine is faster? And by what margin? **[6 Marks]**

b. Simply the expression  using the rules of Boolean algebra **[3 Marks]**

c. Simplify the following Boolean function using Karnaugh map with canonical sum of product. Construct a logical circuit diagram from the simplified function. **[8 Marks]**

$F(w,x,y,z) = \Sigma(1,3,7,11,15) + dc(0,2,5,8)$

Question2 [40 Marks]

a)

i. State Amdahl's law and derive a generalized expression for the law. **[4 Marks]**

ii. Intel corporation is considering an enhancement of its new core i7 microprocessor for a web server. Three different enhancements have been proposed to exploit parallelism. First enhancement ($\mathbf{first}_{enh}$) will make the CPU 30 times faster at only 25% of the CPU time. The second

enhancement (**second**$_{enh}$) is will make the CPU 20 times faster at only 30% of the CPU time and the third enhancement（**third**$_{enh}$）will make the CPU 15 times faster at only 45% of the CPU time. If only one of the enhancements is can be implemented, which one should be implement to maximize CPU performance.**[11 Marks]**

a)

I. Describe the memory hierarchy and explain how the memory hierarchy helps in solving the design constraint of computers' memory. **[5 Marks]**

II. Explain indirect addressing mode given example**. [2 Marks]**

III. Explain the principle of locality and differentiate between the two kinds of locality in relation to the memory hierarchy **[5 marks].**

IV. Given a 32-bit word represented by the hexadecimal equivalent **0x0A050C08**, stored in memory location **W**.

1. Explain byte-addressability. **[3 Marks]**

2. Show how this word would be stored with byte-addressability using little-endian and big-endian **[6 marks]**

I. Describe the motivation of the CISC architecture that would make its choice paramount over the RISC architecture. **4 Marks]**

Question3 [40 Marks]

a. Define the following terms in relation to cache memory access by the CPU;

i. *Cache hit, Cache hit time, Cache hit ratio, Cache miss, Cache miss penalty, Cache miss ratio*. ***[6 Marks]***

ii. Suppose that a computer has a processor with two L1 caches, one for instructions and one for data, and an L2 cache. Let τ be the access time for the two L1 caches. The miss penalties are approximately 15τ for transferring a block from L2 to L1, and 100τ for transferring a block from the main memory to L2. For the purpose of this problem, assume that the hit rates are the same for instructions and data and that the hit rates in the L1 and L2 caches are 0.96 and 0.80, respectively.

1. What is the average access time by the processor assuming there was a cache hit in L1 cache? **[5 Marks]**
2. What is the average access time assuming there was a cache miss in L1 and cache hit in L2 cache? **[7 Marks]**
3. State any three ways of improving cache performance in terms of average access time. **[3 Marks]**

a.

I. What is an advantage of a 3-operand ISA over a 2-operand ISA? **[3 Marks]**

II. Explain a bi-endian processor? **[2 mark]**

III. Write a RISC-style program that accomplishes the expression below using 2-address instruction with Register –Memory Architecture**:[6 Marks]**

I. Describe the defining characteristics of an accumulator-style ISA that distinguishes it from Stack-style ISA. **[3 Marks]**

II. Explain the main characteristics of the Von Neumann Architecture that has contributed to the Von Neumann bottleneck **[5 marks]**