

A. Course Handout

| Institute/School Name | Chitkara University Institute of Engineering and Technology | | | | |
|-----------------------|---|---|--|--|--|
| Department Name | Department of Interdisciplinary Courses in Engin | Department of Interdisciplinary Courses in Engineering (DICE) | | | |
| Programme Name | Bachelor of Engineering (B.E.), Computer Science & Engineering | | | | |
| Course Name | Digital Electronics and Computer Architecture Session 2023-2024 | | | | |
| Course Code | 23IC001 Semester/Batch 2 nd /2023 | | | | |
| L-T-P (Per Week) | 3-0-2 Course Credits 04 | | | | |
| Course Coordinator | Dr. Gaurav Sharma | | | | |

1. Objectives of the Course

Digital electronics is an area of computer science and a computer facilitates a binary number system for its services. Digital electronics defines the two binary numbers, including 1 and 0, using two voltage levels in a machine known as a logic gate. It contains the data mechanism, the instruction group, and methods for addressing memory. The structural design of a computer system is concerned with the descriptions of the multiple functional modules, including processors and memories, and managing them together into an electronic system. This course provides a wide scope of learning & understanding of basic digital electronics and computer architecture. The main objectives of the course are:

- To familiarize the students with the basic understanding of electronics components and their application in engineering field.
- To apply the concept of basic building blocks of digital electronics.
- To familiarize the students with the basic understanding of computer system architecture and organisation.
- To Interpret the concept of machine instruction, input-output and program interrupt.
- To Illustrate concepts regarding pipelining, parallel processing and Direct Memory Access.

2. Course Learning Outcomes

Student should be able:

| | Course Outcome | POs | CL* | KC** | Sessions |
|----------|---|------------------|-----|---------------------------|----------|
| CLO01 | To understand the basics of electronics elements, their functionality and application to perceive the concept of analog circuits. | PO1,PO3,PO4, PO7 | K2 | Fundamental Conceptual | 12 |
| CLO02 | To apply and analyse the concept of boolean algebra in the field of digital electronics for various digital circuits. | PO1,PO4,PO5 | К3 | Conceptual Procedural | 13 |
| CLO03 | To conceptualize and understand the fundamental organization of the computer system architecture. | PO7,PO11 | K4 | Conceptual Fundamental | 9 |
| CLO04 | To comprehend the register organisation, instruction format and control process in central processing unit of computer. | PO1,PO2,PO12 | K2 | Factual Fundamental | 6 |
| CLO05 | To analyse the concept of parallel processing, pipelining and direct memory access to speed-up the computer processing. | PO3, PO5, PO12 | K4 | Conceptual Procedural | 7 |
| Total Co | ontact Hours | | | | 71 |

Revised Bloom's Taxonomy Terminology

^{*}Cognitive Level =CL

^{**}Knowledge Categories = KC



| Course Learning Outcomes | PO1 | PO2 | PO3 | PO4 | PO5 | PO6 | PO7 | PO8 | PO9 | PO10 | PO11 | PO12 |
|--------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|------|------|------|
| CLO01 | L | | L | М | | | L | | | | | |
| CLO02 | М | | | L | Н | | | | | | | |
| CLO03 | | | | | | | Н | | | | L | |
| CLO04 | М | L | | | | | | | | | | L |
| CLO05 | | | М | | Η | | | | | | | L |

H=High, M=Medium, L=Low

3. ERISE Grid Mapping

| Feature Enablemnet | Level(1-5, 5 being highest) |
|--------------------|-----------------------------|
| Entrepreneurship | 2 |
| Research | 3 |
| Innovation | 3 |
| Skills | 4 |
| Employability | 3 |

4. Recommended Books (Reference Books/Text Books)

- **B1**: Basic Electronics and Linear Circuits by N. N Bhargava, D. C Kulshreshtha, S. C Gupta; McGraw Hill Publications, Second Edition, 2013.
- B2: Modern Digital Electronics by R. P. Jain; McGraw Hill Publications, Fourth Edition, 2010.
- **B3:** Fundamentals of Digital Circuits by A. Anand Kumar; PHI Learning Publications, Second Edition, 2011.
- **B4:** Computer System Architecture by M. Morris Mano; Pearson Education, Revised Third Edition, 2018
- **B5:** Computer Architecture and Organization by John P Hayes, McGraw Hill Publications, Third Edition, 1998
- **B6:** Digital Electronics and Computer Architecture by J. V. Suresh Babu and N. Nagendra Reddy, Falcon Publications, First Edition, 2017.
- **B7:** Basic Electrical and Electronics Engineering by V. Jegathesan, K. Vinoth Kumar, R. Saravana Kumar, Wiley India, First Edition, 2011.

5. Other readings and relevant websites

| Serial No | Link of Journals, Magazines, websites and Research Papers | | | |
|-----------|---|--|--|--|
| 1. | https://www.vedantu.com/evs/capacitor-inductor-resistor | | | |
| 2. | https://www.electronics-tutorials.ws/diode/diode_2.html/ | | | |
| 3. | https://www.electrical4u.com/pnp-transistor/ | | | |
| 4. | https://nptel.ac.in/courses/106104073 | | | |
| 5. | https://nptel.ac.in/courses/106106134 | | | |



6. Recommended Tools and Platforms

Virtual Labs, NPTEL, SWAYAM

7. Course Plan

| Session Number | Topic(s) | Book(page no.) | | | | |
|----------------|---|-----------------------------------|--|--|--|--|
| 1 | Introduction to Course Handout Introduction to Basic Electronics, Digital Electronics and Computer Architecture | B1-B7 | | | | |
| | Active and passive components, Ohm's law, Concept and various types of Resistors | B1 (5) | | | | |
| 2-3 | Capacitors, Inductors and their series and parallel combinations | B1 (12), B7(6, 10, 12) | | | | |
| 4 | n-type and p-type semiconductor, P-N Junction Diode, V-I Characteristics, Ideal Diode, Diode application as a switch | B1 (69), B1 (79) | | | | |
| 5-6 | Rectifiers: Half Wave, Full Wave Rectifier: Centre-tap and Bridge Rectifiers, PIV, Efficiency and Ripple Factors | B1 (89) | | | | |
| 7-9 | Rectification with Filters: Shunt Capacitor, Chock input LC and pi-Filters, Zener Diode, Light Emitting Diode, Bipolar Transistors: NPN and PNP transistor. | B1(105), B1 (137), B7 (436) | | | | |
| 9-10 | Digital Electronics: Digital and analog systems, logic levels, duty cycle & pulse waveform, Number Systems (Decimal, Binary, Octal and hexadecimal), Conversions in Number System, 1's Complement and 2's complement | B3 (1), B2 (28) | | | | |
| | ST-1 | | | | | |
| 11-12 | Representation of Signed Numbers using 1's and 2's Complement Method, Binary Addition, Subtraction and Multiplication, Arithmetic using Complement Method | B3 (31, 36, 39) | | | | |
| 13-14 | Logic Gates, Basic gates, Universal Gates and special purpose gates with their truth table, symbols, logical expression, Boolean algebra - Laws of Boolean algebra, Realization of simplified Boolean Expressions using Logic Gates | B3 (108), B3 (141) | | | | |
| 15-17 | K-Map (upto 4 variables) with don't care conditions, Encoders and Decoders, Multiplexers and Demultiplexers, Basic Latches and Flip-Flops with truth tables. | B3 (196), B3 (330, 345, 354, 459) | | | | |
| 18 | Computer Organisation: Introduction to Computer Organization & Architecture, Basic Computer Organization | B4 (3) | | | | |
| 19-20 | Instruction Codes, Computer Registers, Computer Instructions, Memory Reference, Register Reference and I/O Instructions, instruction Set Completeness | B4 (144,149) | | | | |
| | ST-2 | | | | | |
| 21-22 | Timing and Control, Instruction Cycle, Process to determine the type of instructions, Input-Output and Program Interrupts. | B4 (153, 170) | | | | |
| 23-24 | Central Processing Unit: Introduction, General Register Organization, Operation of Control Unit | B4 (265) | | | | |
| 25-26 | Control Word, Stack Organization and Instruction Format, Various Addressing Modes | B4 (268, 270, 283) | | | | |



| 27-28 | RISC and CISC Characteristics, Introduction to Parallel Processing, Flynn's Classification of Computers | B4 (304, 323) | | | | |
|---------------|---|--------------------|--|--|--|--|
| 29-30 | Pipelining, Pipeline Hazards, Direct Memory Access (DMA), DMA Transfer, Input-Output Processor (IOP), | B4 (329, 446, 450) | | | | |
| | ST-3 | | | | | |
| 31-32 | General Introduction to Computer memory: Memory hierarchy, Main Memory: RAM and ROM, Auxiliary Memory: Magnetic Disks and Tape, Chache Memory | B4(479) | | | | |
| End Term Exam | | | | | | |

8. <u>Delivery/Instructional Resources</u>

| Session | Topics | Web References | Audio-Video |
|---------|--|--|--|
| No. | | | |
| 1-3 | Basics of Electronics: Introduction to Basic Electronics, Active and passive components, Ohm's law, Concept and various types of Resistors, Capacitors, Inductors and their series and parallel combinations, n-type and p- type semiconductor | https://www.electronics- notes.com/articles/basic_conce pts/ http://web.mit.edu/6.012/ww w/SP07-L2.pdf | https://nptel.ac.in/courses/ 122106025 https://nptel.ac.in/courses/ 108101091 |
| 4-7 | P-N Junction Diode, V-I Characteristics, Ideal Diode, Diode application as a switch, Rectifiers: Half Wave, Full Wave Rectifier: Centre-tap and Bridge Rectifiers, PIV, Efficiency and Ripple Factors, Rectification with Filters: Shunt Capacitor, Chock input LC and pi-Filters, Zener Diode, Light Emitting Diode | https://www.physics-and-radio- electronics.com/electronic- devices-and- circuits/semiconductor- diodes/pnjunctionsemiconduct ordiode.html https://ecenotesgeu.files.word press.com/2016/09/rectifiers.p | https://nptel.ac.in/courses/ 122106025 https://nptel.ac.in/courses/ 108101091 |
| 8-9 | Bipolar Transistors : NPN and PNP transistor. | https://www.elprocus.com/diff erence-between-npn-and-pnp- transistor/ | https://nptel.ac.in/courses/ 122106025 |
| 10-13 | Digital Electronics: Digital and analog systems, logic levels, duty cycle & pulse waveform Number Systems (Decimal, Binary, Octal and hexadecimal), Conversions in Number System, 1's Complement and 2's complement, Representation of Signed Numbers using 1's and 2's | https://www.studocu.com/in/d ocument/kannur- university/computer- science/digital-electronics- number-system/32305209 | https://nptel.ac.in/courses/ 108105132 |



| 14-15 | Complement Method, Binary Addition, Subtraction and Multiplication, Arithmetic using Complement Method Logic Gates, Basic gates, Universal Gates and special purpose gates with their truth table, symbols, logical expression, Boolean algebra - Laws of Boolean algebra, Realization of simplified Boolean Expressions using Logic Gates. | https://www.madeeasy.in/uplo ads/examsolution/09.DigitalEle ctronics_UPPSCTheory.pdf | https://nptel.ac.in/courses/ 108105132 |
|-------|--|--|--|
| 16-17 | K-Map (upto 4 variables) with don't care conditions, Encoders and Decoders, Multiplexers and Demultiplexers, Basic Latches and Flip- Flops with truth tables. | https://www.electronicshub.or g/flip-flops/ https://web.ece.ucsb.edu/Facul ty/Johnson/ECE152A/L3%20- %20Karnaugh%20Maps%20&% 20Combinational%20Logic%20 Design.pdf https://www.electronicsforu.co m/technology-trends/learn- electronics/flip-flop-rs-jk-t- d?utm_source=google&utm_m edium=cpc&utm_campaign=Ele .com+- +traffic+Dynamic+Search+-22- 12- 2021&gclid=CjwKCAjwqZSlBhB wEiwAfoZUIGkXdVDy- xW_OHQoDy 4J412LbqZrlzattmewS9IF7eOCO S4yPaxRoCdHsQAvD_BwE | https://nptel.ac.in/courses/ 108105132 |
| 18 | Computer Organisation: Introduction to Computer Organization & Architecture, Basic Computer Organization, Instruction Codes | https://nitsri.ac.in/Department /Electronics%20&%20Communi cation%20Engineering/Chapter 1-Introduction.pdf https://www.geeksforgeeks.org /computer-organization-and- architecture-tutorials/ https://www.codingninjas.com/ studio/library/instruction- codes-and-addresses | https://archive.nptel.ac.in/c ourses/106/105/106105163 / |



| 19-20 | Computer Registers, Computer Instructions, Memory Reference, Register Reference and I/O Instructions, instruction Set Completeness, Timing and Control | https://www.pvpsiddhartha.ac.i n/dep_it/lecture%20notes/COA /CSA%20UNIT%202.pdf https://www.studocu.com/in/d ocument/babu-banarasi-das- university/computer- organization- architecture/computer- architecture-21-40/48437969 | https://archive.nptel.ac.in/c ourses/106/105/106105163 / |
|-------|---|--|---|
| 21-22 | Instruction Cycle, Process to determine the type of instructions, Input-Output and Program Interrupts | https://vardhaman.org/wp-content/uploads/2021/03/COA-Unit-II-part-1.pdf https://www.lkouniv.ac.in/site/writereaddata/siteContent/202004171006162950anshu_singh_engg_input_output.pdf | https://archive.nptel.ac.in/c ourses/106/105/106105163 / |
| 23-25 | Central Processing Unit: Introduction, General Register Organization, Operation of Control Unit, Control Word, Stack Organization and Instruction Format, Various Addressing Modes | http://gacbe.ac.in/pdf/emateri al/18BIT44A-U3.pdf https://gppanchkula.ac.in/wp- content/uploads/2021/06/e_co ntent_of_co-1.pdf | https://nptel.ac.in/courses/ 106103068 https://archive.nptel.ac.in/c ourses/106/105/106105163 / |
| 26-28 | RISC and CISC Characteristics, Introduction to Parallel Processing, Flynn's Classification of Computers, Pipelining, Pipeline Hazards | https://www.geeksforgeeks.org /computer-organization-risc- and-cisc/ https://byjus.com/gate/flynns- classification-notes/ https://www.studytonight.com /computer- architecture/pipelining | https://nptel.ac.in/courses/ 106103068 https://archive.nptel.ac.in/c ourses/106/105/106105163 / |
| 29-32 | Direct Memory Access (DMA), DMA Transfer, Input-Output Processor (IOP), General Introduction to Computer memory: Memory hierarchy, Main Memory: RAM and ROM, Auxiliary Memory: Magnetic Disks and Tape, Chache Memory | https://www.elprocus.com/dire ct-memory-access-dma-in- computer-architecture/ https://www.studytonight.com /computer-architecture/input- output-processor https://www.studytonight.com /computer- architecture/memory- organization | https://archive.nptel.ac.in/c ourses/106/105/106105163 / https://nptel.ac.in/courses/ 106103068 |



9. Action plan for different types of learners

| Slow Learners | Average Learners | Fast Learners |
|---|-------------------------|---|
| Remedial Classes, Doubt Sessions, Guided Tutorials | Workshop, Doubt Session | More Practical Assignments/ Quiz/Competitions, Project |
| | | |

10. Evaluation Scheme & Components

| Evaluation Component | Type of Component | No. of Assessments | Weightage of Component | Mode of Assessment |
|-------------------------|----------------------------|-----------------------|---------------------------|-----------------------|
| Component 1 | Continuous Evaluations | 02* | 25% | Computer Based Test |
| Component 2 | Sessional Tests (STs) | 03** | 25% | Computer Based Test |
| Component 3 | End Term Examination (ETE) | 01*** | 50% | Computer Based Test |
| | Total | | 100% | |

^{*} There will be two Continuous Evaluations (CE) for a lab in a semester as CE-1 and CE-2, one will be considered as mid term/day to day evaluation and another one will be based on developed project. Average marks of CE-1 and CE-2 will be taken as final marks. Lab file record, lab performance in whole semester and internal viva with experiment performance will be taken in consideration of CE-1.

11. Syllabus of the Course

| Subject: | Digital Electronics and Computer Architecture | | |
|----------|---|--------------------|-------------|
| S. No. | Topic (s) | No. of Sessions | Weightage % |
| 1 | Basics of Electronics: Introduction to basic electronics, Active and passive components, Ohm's law, Concept and various types of Resistors, Capacitors, Inductors and their series and parallel combinations, n-type and p-type semiconductor, P-N Junction Diode, V-I Characteristics, Ideal Diode, Diode application as a switch, Rectifiers: Half Wave, Full Wave Rectifier: Centre-tap and Bridge Rectifiers, PIV, Efficiency and Ripple Factors, Rectification with Filters: Shunt Capacitor, Chock input LC and pi-Filters, Zener Diode, Light Emitting Diode, Bipolar Transistors: NPN and PNP transistor. | 12 | 20% |
| 2 | Digital Electronics: Digital and analog systems, logic levels, duty cycle & pulse waveform, Number Systems (Decimal, Binary, Octal and hexadecimal), Conversions in Number System, 1's Complement and 2's complement, Representation of Signed Numbers using 1's and 2's | 13 | 30% |

^{**} All STs are compulsory. ST1 and ST2 have weightage of 25% each and ST3 has 50% out of total weightage of component 2.

^{***}It is mandatory to complete Components 1 and 2. Further, as per Academic Guidelines minimum 75% attendance is required to become eligible for appearing in the End Semester Examination.



| | Complement Method, Binary Addition, Subtraction and Multiplication, | | |
|---|---|----|------|
| | Arithmetic using Complement Method, Logic Gates, Basic gates, | | |
| | Universal Gates and special purpose gates with their truth table, | | |
| | symbols, logical expression, Boolean algebra - Laws of Boolean algebra, | | |
| | Realization of simplified Boolean Expressions using Logic Gates, K-Map | | |
| | (upto 4 variables) with don't care conditions, Encoders and Decoders, | | |
| | Multiplexers and Demultiplexers, Basic Latches and Flip- Flops with | | |
| | truth tables. | | |
| 3 | Computer Organisation: Introduction to Computer Organization & | 9 | 20% |
| | Architecture, Basic Computer Organization, Instruction Codes, | | |
| | Computer Registers, Computer Instructions, Memory Reference, | | |
| | Register Reference and I/O Instructions, instruction Set Completeness, | | |
| | Timing and Control, Instruction Cycle, Process to determine the type of | | |
| | instructions, Input-Output and Program Interrupts. | | |
| | | | |
| 4 | Control Businessins Heits Internalisation Consul Besister Consulation | 42 | 200/ |
| 4 | Central Processing Unit: Introduction, General Register Organization, | 13 | 30% |
| | Operation of Control Unit, Control Word, Stack Organization and | | |
| | Instruction Format, Various Addressing Modes, RISC and CISC | | |
| | Characteristics, Introduction to Parallel Processing, Flynn's | | |
| | Classification of Computers, Pipelining, Pipeline Hazards, Direct | | |
| | Memory Access (DMA), DMA Transfer, Input-Output Processor (IOP), | | |
| | General Introduction to Computer memory: Memory hierarchy, Main | | |
| | Memory: RAM and ROM, Auxiliary Memory: Magnetic Disks and Tape, | | |
| | Chache Memory | | |
| | | | |

12. Complete Lab Course Coverage Plan:

| Session No. | Lab Session | Resource Link |
|----------------|--|--|
| 1 | To familiarize with basic electronic equipments (CRO, DSO, Function Generator, Multimeter, DC Power Supply, Breadboard etc.) and electronics components (resistor, capacitor, inductor, diode, LED, transistor, etc.). | CRO and Function Generator:- http://vlabs.iitkgp.ac.in/psac/newlabs 2020/vlabiitkgpAE/exp1/index.html# |
| | | http://vlabs.iitkgp.ernet.in/be/index.html# |



| 2 | To plot and analyse the forward and reverse characteristics of PN junction Si / Ge diode and determine the knee voltage. | http://vlabs.iitkgp.ernet.in/be/exp5/in dex.html |
|-------|--|--|
| 3 | To analyze and plot Zener diode as voltage regulator and observe the output voltage with variable input voltage. | http://vlabs.iitkgp.ernet.in/be/exp10/index.html# |
| 4 | To study the operation of half wave and full wave rectifiers (with and without filters). | Half Wave Rectifier:- http://vlabs.iitkgp.ernet.in/be/exp6/index.html |
| | | Full Wave Rectifier:- |
| | | http://vlabs.iitkgp.ernet.in/be/exp7/in dex.html |
| 5 | To study and verify the truth tables of various logic gates on digital trainer kit using TTL ICs. | https://de-iitr.vlabs.ac.in/exp/truth- table-gates/theory.html |
| 6 | To study and verify D and J-K Flip-Flop using their respective ICs. | https://de-iitr.vlabs.ac.in/exp/truth- tables-flip-flops/simulation.html |
| 7 | To study and verify the function of BCD (Binary Coded Decimal) to seven segment decoder (IC 7447) and operation of 7-segment LED display on digital trainer kit. | http://vlabs.iitkgp.ernet.in/dec/exp1/i ndex.html# |
| 8 | To implement and study 4:1 multiplexer and 1:4 demultiplexer using logic gates using virtual labs. | https://de- iitr.vlabs.ac.in/exp/multiplexer- demultiplexer/index.html |
| 9 | To study various internal and external hardware components of computer architecture and its organization. | https://gptcthirurangadi.in/download/ pdf/academic-files/4137 AKNMGptc.pdf |
| 10 | To design and simulation of Arithmetic Logic Unit (ALU) using virtual labs. | http://vlabs.iitkgp.ac.in/coa/exp8/inde x.html |
| 11 | Continuous Evaluation-1 (Experiment Performance) | |
| 12-14 | Project Work | |
| 15 | Continuous Evaluation-2 (Based on Project Work) | |

This Document is approved by:

| Designation | Name | Signature |
|--------------------|---------------------|-----------|
| Course Coordinator | Dr. Gaurav Sharma | |
| Dean-DICE | Dr. Rajneesh Talwar | |
| Date (DD-MM-YYYY) | 03-01-2024 | |