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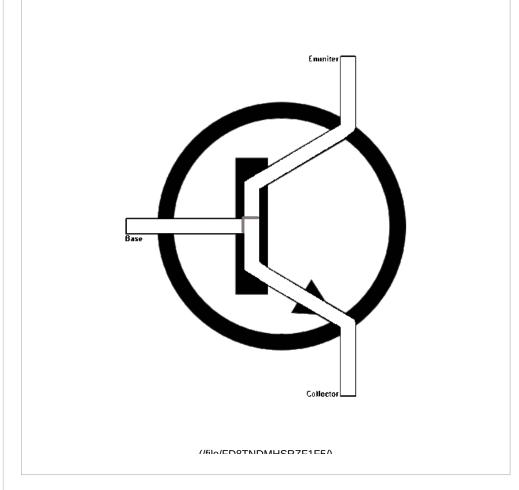
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(/member/Szabolcs/) More by Szabolcs:





Hi guys, in this tutorial I will show you some NPN transistor based logic gates.

What you need

- -A breadboard
- -A bunch of 5k and 10k resistors, and transistors
- -A LED

You can use any NPN type transistor (for example 2N3904, BC547, BC548, BC549 etc.)

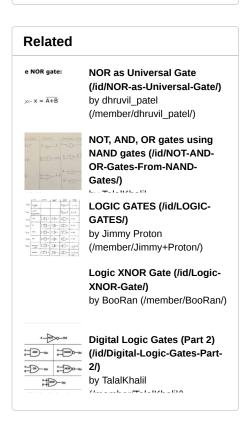
These are basic circuits, so they can be improved (with diodes for reverse voltage protection, for example), or can be simplified (XOR, XNOR gates), but for start we will stick with these basic circuits.

These circuits are extremely easy to understand. I think if you know a little bit about NPN transistors, you will be fine. The use of transistors for the construction of logic gates depends upon their utility as fast switches. When the base-emitter diode is turned on enough to be driven into saturation, the collector voltage with respect to the emitter may be near zero and can be used to construct gates for the TTL logic family.

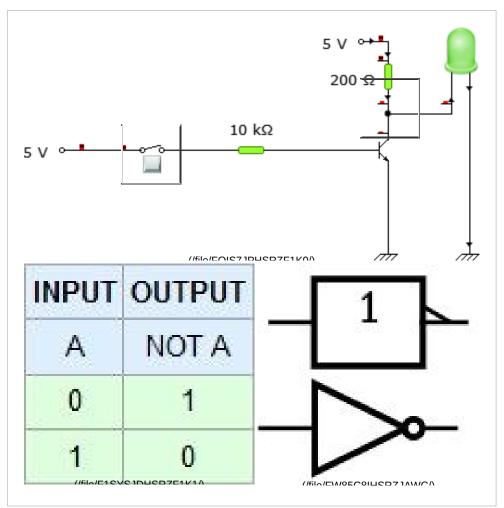
I am going to show the logic gate's symbols, truth tables and schematics. I will also show this circuits on the breadboard. (As i mentioned before these are easy circuits, so on a breadboard I wont show them step-by-step) There is a small text and a gif for every logic gate.

I attached three images for beginners. The third image is the most important.





Step 1: NOT gate



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A NOT gate is often referred to an inverter. Inverters simply output the opposite as the input. When the input is forced to logic HIGH (1) the output is forced to logic LOW (0) and vice versa.

This is the easiest one.

For the NOT logic, there is only one transistor and the output is driven to the ground (LOW or 0) if it is conducting.

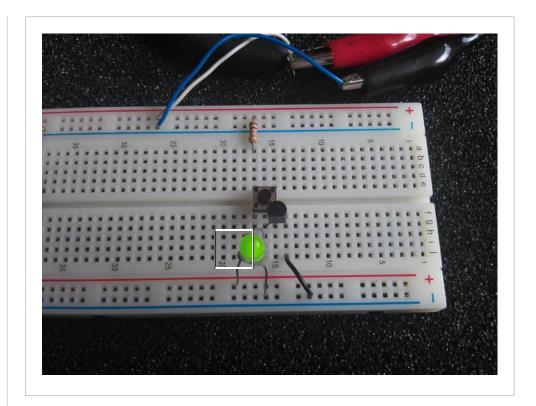


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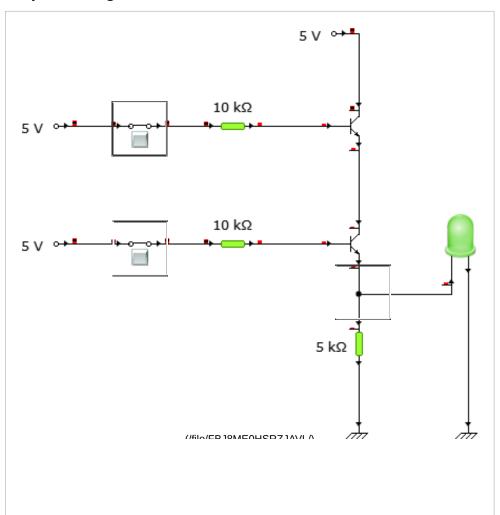
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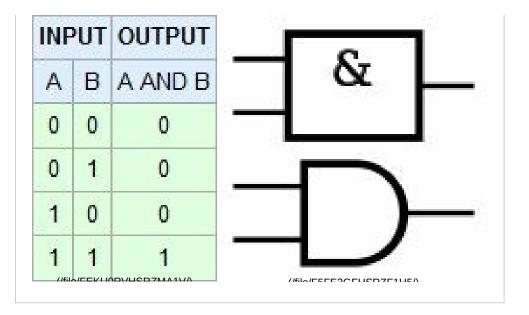
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NOT gate on a breadboard

Step 3: AND gate

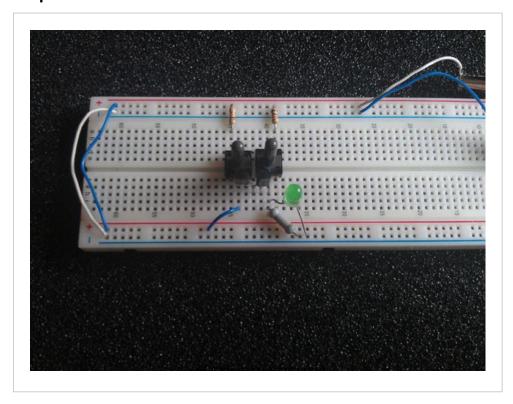




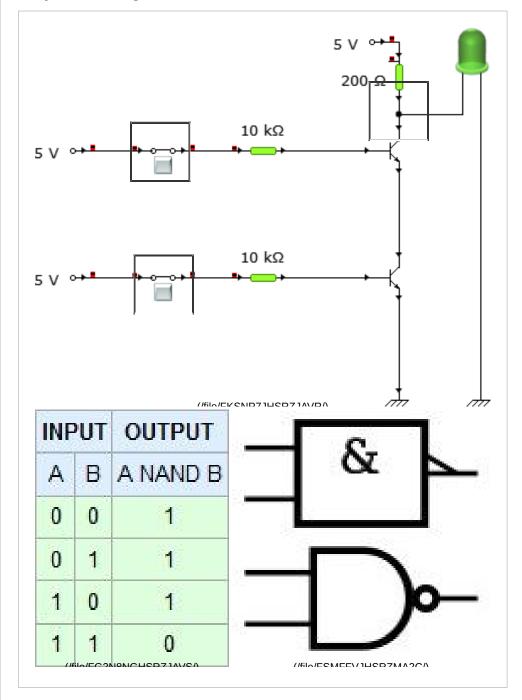
The AND gate is a logic Boolean gate that represents multiplication in basic algebra. When both input to the AND gate are forced to a logic HIGH (1) level, the output will be forced to a logic HIGH (1) level. But if either of the inputs are forced to logic LOW (0) the output will be forced to a logic LOW (0). This is the equivalent of a multiplication statement where only Boolean variables are allowed.

For the AND logic, the transistors are in series and both transistors must be in the conducting state to drive the output high.

Step 4:



Step 5: NAND gate

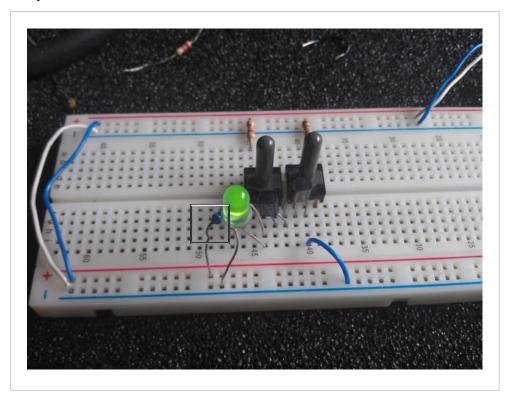


A NAND gate is also referred to as a NEGATED AND gate. It is the opposite or inverse of a simple AND gate. With the AND gate the output was forced to a logic HIGH (1) only when both inputs where forced to logic HIGH (1), but with a NAND gate the output is forced to logic LOW (0) when both inputs are forced to logic HIGH (1) and the output is forced to logic HIGH (1) in all other situations.

For the NAND logic, the transistors are in series, but the output is above them. The output is high unless both A and B inputs are high, in which case the output is taken down close to ground potential.

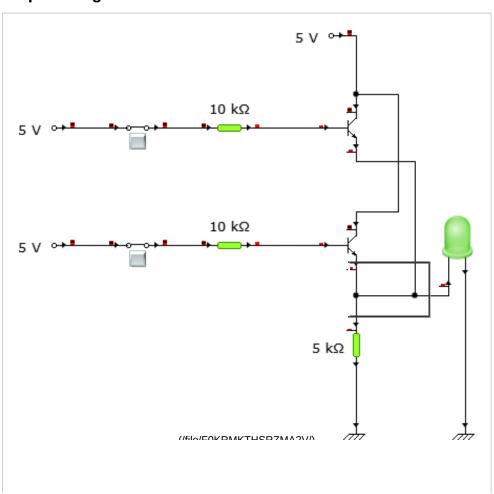
In the simulator I accidentally used a 2000hm resistor, but in reality you should use around 1K or something like that.

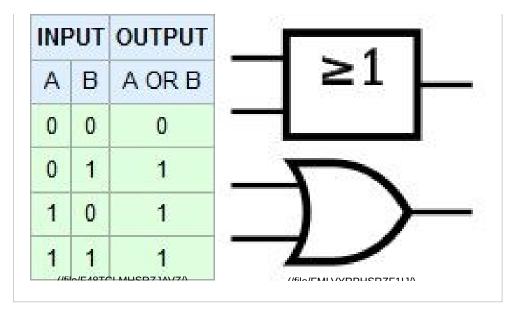
Step 6:



NAND gate on a breadboard

Step 7: OR gate

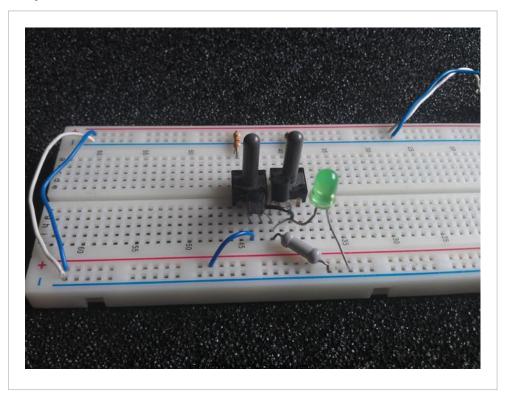




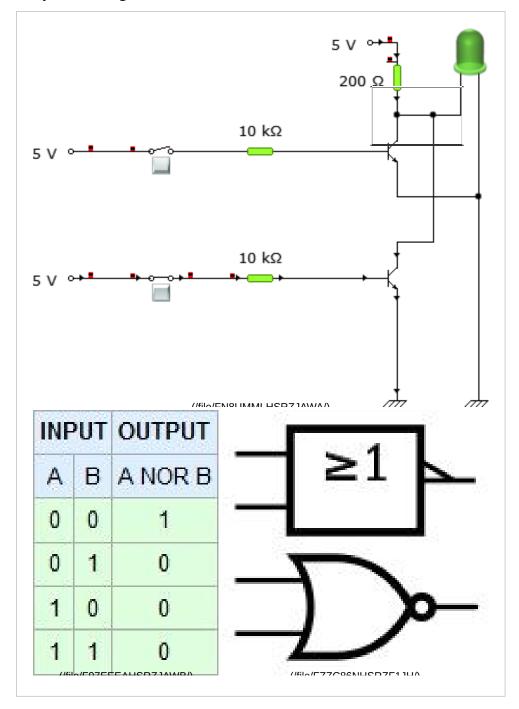
The OR gate is a logic Boolean gate that represents addition in basic algebra. If either of the inputs or both inputs to a basic OR gate are forced to logic HIGH (1) the output is forced to logic HIGH (1). If both of the inputs are forced to a logic LOW (0) the output is forced to a logic LOW (0). This closely resembles the addition statement where only Boolean variables are allowed.

For the OR logic, the transistors are in parallel and the output is driven high if either of the transistors is conducting.

Step 8:



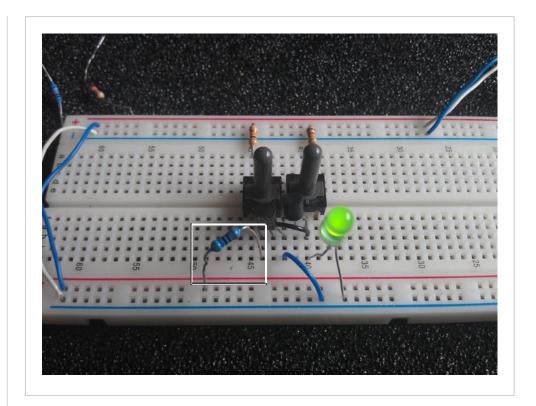
Step 9: NOR gate



A NOR gate is also referred to as a NEGATED OR gate. It is the opposite or inverse of a simple OR gate. With the OR gate the output was forced to logic LOW (0) when both inputs were forced to logic LOW (0) and the output was logic HIGH (1) in all other situations, but with a NOR gate the output is forced to logic HIGH (1) when both inputs are forced to logic LOW (0) and the output is forced to logic LOW (0) in all other situations.

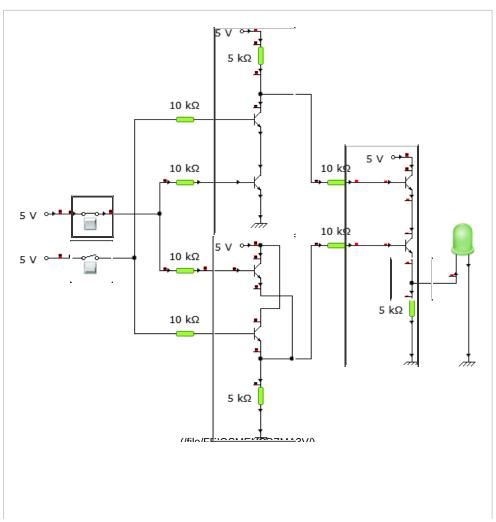
For the NOR logic, the transistors are in parallel with the output above them so that if either or both of the inputs are high, the output is driven low.

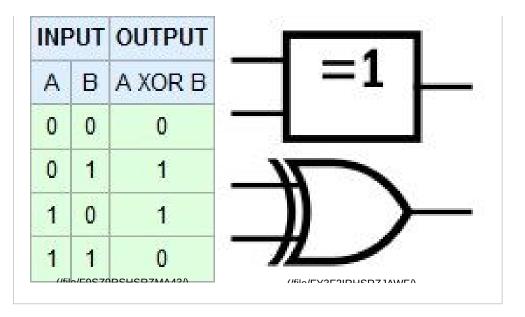
In the simulator I used a 200 Ohms resistor, but you should use one around 1K.



NOR gate on a breadboard

Step 11: XOR gate

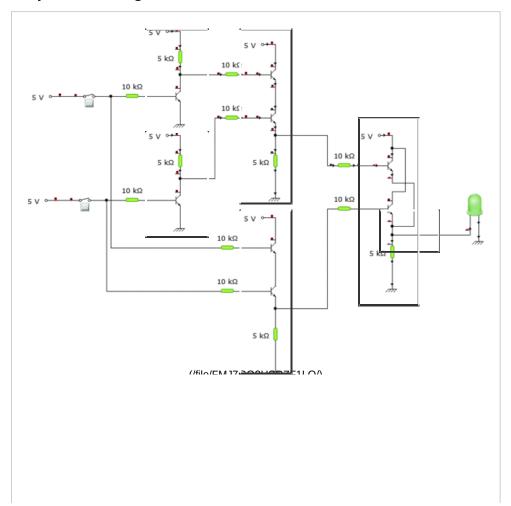


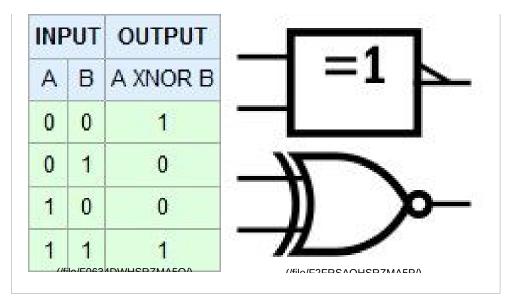


A XOR gate is also referred to as EXCLUSIVE OR. With a XOR gate the output is forced to logic HIGH (1) when one input is exclusively forced to logic HIGH (1). If both inputs are forced to either logic LOW (0) or logic HIGH (1) the output is forced to logic LOW (0). This is similar to the OR gate with the exception of both input being logic HIGH (1).

As you can see I constructed this one with other gates. In this circuit I used a NAND, OR and an AND gate.

Step 12: XNOR gate

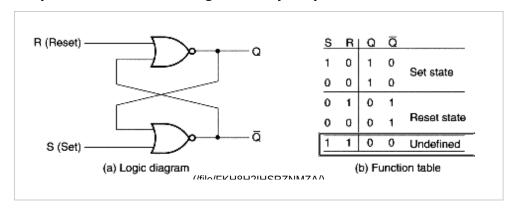




A XNOR gate, like the XOR gate, is also referred to EXCLUSIVE NOR. With the XNOR gate the output is forced to logic LOW (0) when one of the inputs are exclusively forced to logic HIGH (1). If both of the inputs are forced to either logic LOW (0) or logic HIGH (1) the output is forced to logic HIGH (1). This is similar to the XOR gate but is inverted.

As you can see I constructed this one with other gates. I used two inverter, two AND and an OR gate in this circuit.

Step 13: Build something! - SR flip-flop



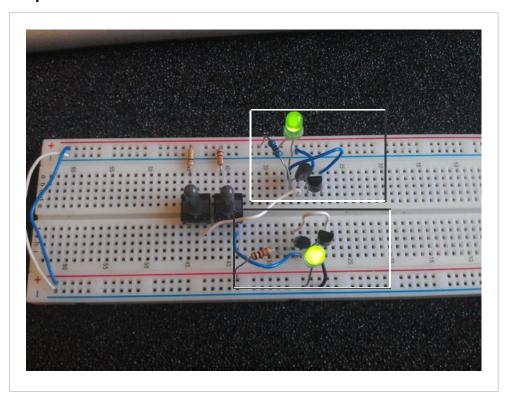
Now we know the transistor gates, lets make something with them. :) For example, here is an SR flip-flop. (SR latch)

When using static gates as building blocks, the most fundamental latch is the simple SR latch, where S and R stand for set and reset. It can be constructed from a pair of cross-coupled NOR logic gates. The stored bit is present on the output marked Q.

The output usually marked as Q, but sometimes it is marked as X, Y or F.

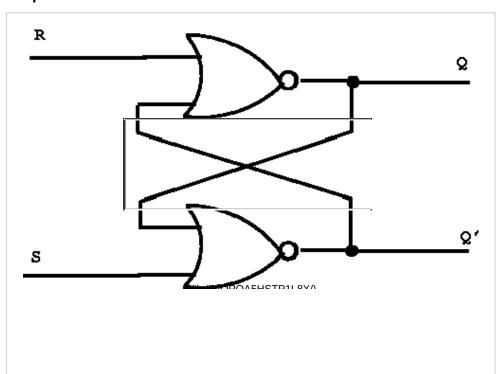
While the S and R inputs are both low, feedback maintains the Q and Q' outputs in a constant state, with Q' the complement of Q. If S (Set) is pulsed high (=when you push the button) while R (Reset) is held low, then the Q output is forced high, and stays high when S returns to low; similarly, if R is pulsed high while S is held low, then the Q output is forced low, and stays low when R returns to low.

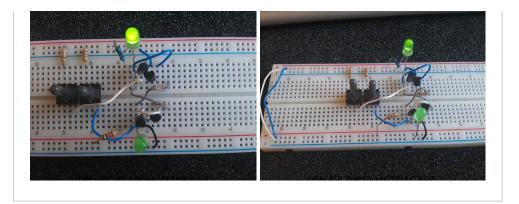
Step 14:



First of all, build two independent NOR gate on your breadboard. (step 9) Do not connect both of their inputs the the push buttons, you only have to connect the A inputs of each gate.

Step 15:





Now connect the B inputs to the other NOR gate's output trough a 10k resistor.

Now we are ready, you made an SR flip-flop or SR latch.

When you press the button one, the Q LED goes out, and the Q' LED lights up. Then if you press the button two, the Q LED light up, and the Q' goes out. Technically you can store data with it, this is why we call it "latch". You shouldt press the two buttons at once, its a forbidden state, it can make the flip-flop unstable.



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neumanngregor (/member/neumanngregor)

5 months ago

O Reply

Reply

Very, very good instructable and with the Yenka simulation is easy to understand, you did a excellent job.



JRV31 (/member/JRV31)

9 months ago

Great instructable, I enjoyed building all the gates.

In you picture on the intro page you show the emitter and the collector reversed.