Task1 - RISC-V Reference SoC — Functional and GLS Replication (SCL180) on your own IITGN Machine

Deadline: Today EOD
Action: Push results to your individual GitHub repository

Objective

You must replicate the complete **functional simulation** and **gate-level simulation (GLS)** of the **vsdcaravel** RISC-V SoC using **SCL180 PDKs**, exactly as demonstrated in the reference repository:

Reference:
https://github.com/vsdip/vsdRiscvScl180/tree/iitgn

This task ensures that you understand the SoC structure, RTL integration, simulation flow, synthesis readiness, and overall bring-up flow required for the SCL180 tapeout process.

Task Breakdown

1. Study the Reference Repository

Review the structure and purpose of each folder:
`rtl/`, `dv/`, `synthesis/`, `gl/`, `gls/`, `images/`.

Understand the top module (`vsdcaravel.v`), integration of VexRiscv, RAM128, POR, housekeeping, IO pads, and the hkspi block.

2. Run Functional (RTL) Simulation

Inside `dv/hkspi/`:

1. Set paths in the Makefile:
    - `GCC_Path` → Your RISC-V GCC
    - `scl_io_PATH` → SCL IO models
2. Run:

```
make clean
make
vvp hkspi.vvp
gtkwave hkspi.vcd hkspi_tb.v
```

7. Expected results:
    - Successful console output
    - Clean waveform confirming correct hkspi operation

Upload the VCD, logs, and waveform screenshots to your repo.

3. Run Gate-Level Simulation (GLS)

Inside `gls/`:

1. Modify the synthesized netlist:
    - Remove black-box entries for: `dummy_por`, `RAM128`, `housekeeping`
    - Add the following at the top:
    - `` `include "dummy_por.v" ``
    - `` `include "RAM128.v" ``
    - `` `include "housekeeping.v" ``
2. In `vsdcaravel.v`, replace `1'b0` with `vssa` for power pin wiring.
3. Update `gls/Makefile`:
    - Add paths for SCL PDK, RISC-V GCC, and IO libraries.
4. Run GLS:
5. `make clean`
6. `make`
7. `vvp hkspi.vvp`
8. `gtkwave hkspi.vcd hkspi_tb.v`
9. Expected results:
    - GLS waveform closely matching RTL waveform
    - No unknown states on critical paths

Upload the netlist, logs, VCD, and waveform screenshots.

4. Update Your Repository

Create a folder named **`Day1_Task_Replication/`** containing:

- Functional simulation evidence
- GLS evidence
- A README summarizing:
    - Steps taken
    - System details
    - Issues encountered and resolved

Deliverables Checklist

Task	Deliverable
Functional Simulation	Log, VCD, waveform screenshot
GLS	Netlist, log, VCD, waveform screenshot
Repository Update	README + evidence folder

Deadline

Today – 11:59 PM
Submissions without evidence will be considered incomplete.