Task4: Full Management SoC DV Validation on SCL-180 (POR-Free Design)

Duration: 2 Days (Today + Tomorrow)
Deadline: End of Day Tomorrow (11:59 PM IST)
Submission: Mandatory GitHub documentation + evidence
Tools: Synopsys VCS, DC_TOPO, SCL-180 PDK

Reference DV tests link -
https://github.com/efabless/caravel/tree/main/verilog/dv/caravel/mgmt_soc

Objective

The objective of this task is to **prove that our POR-free RTL is production-ready** by:

1. Running **all Management SoC (mgmt_soc) DV tests** originally written for Caravel
2. Using a **new SCL-180 netlist generated via DC_TOPO**
3. Running the same tests **twice**:
    - **Phase-A:** Using RTL SRAM models
    - **Phase-B:** Using **DC_TOPO synthesized SRAM**
4. Demonstrating that **behavior is identical** across:
    - RTL simulation
    - GLS with RTL SRAM
    - GLS with synthesized SRAM

This task confirms that:

- Removing POR is safe
- Reset architecture is correct
- SRAM integration is robust
- RTL has no hidden power-up assumptions

Background (Why this task exists)

The original Caravel `mgmt_soc` DV suite validates:

- Housekeeping SPI
- GPIO configuration and transfer logic
- User project control
- Storage interfaces
- IRQ behavior

These tests **do not rely on POR** — they rely on:

- External reset (`RSTB`)
- Correct pad behavior
- Proper reset distribution

Running these tests on **SCL-180 with a POR-free netlist** is a strong industry-grade validation.

Scope of Work

Participants must run **all Management SoC DV tests** using:

- **SCL-180 PDK**
- **Synopsys VCS**
- **DC_TOPO-generated netlist**

mgmt_soc DV coverage includes:

- hkspi
- gpio
- mprj_ctrl
- storage
- irq

Phase-1: Environment Setup (Mandatory)

1. Toolchain Requirements

- Synopsys **VCS** (functional + GLS)
- Synopsys **DC_TOPO**
- SCL-180 standard cell libraries
- SCL-180 IO models

Phase-2: POR-Free Netlist Generation

2. RTL Preparation

- Confirm:
  - No `dummy_por`, `simple_por`, or POR logic exists
  - Single external reset pin (`reset_n` / `RSTB`)
- Reset must be driven **only from testbench**

3. DC_TOPO Synthesis (Baseline Netlist)

- Synthesize full SoC using DC_TOPO
- SRAM remains **RTL model** in this phase
- Generate:
  - Synthesized netlist
  - Area, timing, and power reports

Deliverable:

- `netlist_rtl_sram/`

- DC reports + logs

Phase-3: Management SoC DV – Run-1 (RTL SRAM)

4. VCS Functional + GLS with RTL SRAM

For **each mgmt_soc DV test**:

- hkspi
- gpio
- mprj_ctrl
- storage
- irq

Participants must:

- Use **VCS**
- Include:
  - DC_TOPO netlist
  - RTL SRAM models
  - SCL-180 standard cell models
- Drive:
  - External reset from testbench
  - Power rails as per DV

Expected Results:

- All tests pass
- No X-propagation after reset
- Identical behavior to reference DV intent

Deliverables (per test):

- Simulation log
- FSDB/VPD waveform
- Screenshot of key pass condition

Phase-4: SRAM Synthesis (Critical Validation Phase)

5. DC_TOPO SRAM Synthesis

- Identify SRAM RTL used in SoC
- Synthesize SRAM using DC_TOPO
- Generate:
  - SRAM gate-level netlist
  - Timing reports

No behavioral SRAM allowed in this phase.

Deliverable:

- `sram_dc_topo/`
- Netlist + reports

Phase-5: Management SoC DV – Run-2 (Synthesized SRAM)

6. VCS GLS with Synthesized SRAM

Re-run **all mgmt_soc DV tests again**, but now with:

- DC_TOPO SoC netlist
- **DC_TOPO SRAM netlist**
- SCL-180 standard cell models

Expected Results:

- Same behavior as Phase-3
- No new X-states
- No reset-related failures
- No memory corruption

This is the **final proof of RTL correctness**.

Deliverables (per test):

- GLS log
- FSDB/VPD waveform
- Screenshot showing correct operation

Phase-6: Engineering Documentation (Mandatory)

7. Final Report (Most Important)

Create a document titled:

"Management SoC DV Validation on SCL-180 (POR-Free Architecture)"

It must include:

1. Why POR was removed
2. Why mgmt_soc DV does not require POR
3. Reset strategy used
4. Differences between:
    - RTL SRAM
    - Synthesized SRAM
5. Observations from both runs

6. Issues faced and how they were resolved

This document should read like a **design sign-off note**, not a lab report.

Submission Structure

```
Task_MgmtSoC_SCL180_Final/
├── netlist_rtl_sram/
├── sram_dc_topo/
├── dv_run_rtl_sram/
│   ├── hkspi/
│   ├── gpio/
│   ├── mprj_ctrl/
│   ├── storage/
│   └── irq/
├── dv_run_synth_sram/
│   ├── hkspi/
│   ├── gpio/
│   ├── mprj_ctrl/
│   ├── storage/
│   └── irq/
├── reports/
└── README.md
```

Evaluation Criteria

Area	Weight
Correct tool usage (VCS + DC_TOPO)	High
POR-free correctness	Very High
DV pass completeness	Very High
Synthesized SRAM validation	Extremely High
Documentation clarity	Extremely High

Low-effort or partial submissions will be rejected.