

Task3 - Removal of On-Chip POR and Final GLS Validation (SCL-180)

Deadline: Tomorrow EOD

Submission: Mandatory GitHub documentation + evidence

Tools: Synopsys VCS, DC_TOPO, SCL-180 PDK

Status: Research-driven, industry-style task

Objective

The objective of this task is to **formally remove the on-chip Power-On Reset (POR)** from the VSD Caravel-based RISC-V SoC and **prove—using design reasoning, pad analysis, synthesis, and gate-level simulation—that an external reset-only strategy is safe and correct** for SCL-180.

By the end of this task, participants must demonstrate:

1. A **POR-free SoC RTL** that relies only on an **external reset pin**
2. A **clear technical justification**, based on **pad behavior and power assumptions**, for why this is safe
3. A **clean DC_TOPO synthesis**
4. A **final VCS-based GLS with SCL-180 standard cells**
5. Industry-quality documentation explaining *why* POR was removed—not just *how*

Context (Why this task exists)

In earlier flows, a behavioral dummy_por was used to model reset sequencing. However:

- Behavioral PORs are **not synthesizable**
- True PORs are **analog macros**, not RTL
- In sane pad libraries (e.g., SCL-180), **pads and reset pins are usable immediately after power-up**
- Therefore, a **single external reset pin** is architecturally sufficient

This task validates that decision rigorously.

Task Breakdown

Phase-1: POR Dependency Analysis (Research Phase)

1. Study and Document Existing POR Usage

You must:

- Identify **where and how** dummy_por is used in:
 - vsdcaravel.v
 - Housekeeping logic
 - Reset distribution paths
- Create a short document explaining:
 - What signals porb_h, porb_l, por_l drive
 - Which blocks *actually* depend on POR versus generic reset

Deliverable:

- Markdown or PDF:
POR_Usage_Analysis.md

2. PAD Library Study (Critical Thinking Section)

Study the **SCL-180 I/O pad documentation** and answer:

- Does the reset pad require:
 - Internal enable?
 - POR-driven gating?
- Is the reset pin:
 - Asynchronous?
 - Available immediately after VDD?
- Are there documented power-up sequencing constraints that *mandate* a POR?

This section must **explicitly contrast SCL-180 with SKY130**, explaining why POR was mandatory in SKY130 but not here.

Deliverable:

- PAD_Reset_Analysis.md
- Include references to pad datasheets or comments from PDK files

Phase-2: RTL Refactoring (Engineering Phase)

3. Remove POR from RTL

You must:

- Completely remove:
 - dummy_por
 - All POR-related signals
- Introduce a **single top-level reset pin**:
 - reset_n (active-low, external)
- Ensure:
 - All sequential logic resets off this signal
 - No hidden POR assumptions remain

Rules:

- No digital POR
- No counters
- No power-pin edge detection
- Reset behavior must be **explicit and visible**

Deliverable:

- POR-free RTL committed to GitHub
- Commit message must clearly state:

“Removed on-chip POR; migrated to external reset-only architecture”

Phase-3: Synthesis with DC_TOPO

4. DC_TOPO Synthesis (POR-Free)

Run synthesis using **DC_TOPO** with:

- SCL-180 standard cell libraries
- Proper reset constraints

- No POR blackboxes

You must generate:

- Synthesized netlist
- Area, timing, and power reports

Key Check:

- No unresolved reset nets
- No floating enable pins
- No inferred latches due to reset removal

Deliverable:

- synthesis/ folder containing:
 - Netlist
 - Reports
 - DC logs

Phase-4: Final Gate-Level Simulation (GLS)

5. VCS-Based GLS (Final Proof)

Run **full chip GLS** using:

- VCS
- DC_TOPO netlist
- SCL-180 functional cell models
- External reset asserted from testbench

You must show:

- Clean reset assertion and de-assertion
- No X-propagation
- Functional equivalence with RTL behavior

Important:

- Reset must be driven **from the testbench**

- No internal reset generation logic allowed

Deliverable:

- GLS log
- FSDB/VPD waveform
- Screenshot showing reset release and normal operation

Phase-5: Engineering Justification (Most Important Part)

6. Final Decision Document

Create a **clear, technical justification** titled:

“Why External Reset Is Sufficient in SCL-180 (No POR)”

This must include:

- Why POR is an **analog problem**
- Why RTL-based POR is unsafe
- Why SCL-180 pads allow safe external reset
- Risks considered and mitigations
- Comparison with SKY130

This document is **non-negotiable** and will be evaluated like a design review.

Deliverable:

- POR_Removal_Justification.md

Submission Structure (Mandatory)

Task_NoPOR_Final_GLS/

```

├── POR_Usage_Analysis.md
├── PAD_Reset_Analysis.md
└── POR_Removal_Justification.md
├── rtl/
└── synthesis/

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└── gls/  
└── waveforms/  
└── README.md
```

Evaluation Criteria

Area	Weight
Technical correctness	High
PAD & reset reasoning	Very High
Clean synthesis	High
Clean GLS	High
Documentation clarity	Extremely High

Superficial “it works” submissions **will be rejected**.