Task 5: SoC Floorplanning Using ICC2 (Floorplan Only)

Deadline: Today – EOD (11:59 PM IST)
Tools: Synopsys **ICC2**
Scope: FLOORPLAN ONLY (No placement, CTS, routing)

Objective

The objective of this task is to **create a correct SoC floorplan using ICC2**, meeting **exact die size and IO pad placement targets**, and to develop hands-on familiarity with **ICC2 floorplanning commands and concepts**.

This task is **intentionally limited to floorplanning only**.
No timing closure, placement optimization, CTS, or routing is expected.

Target Floorplan Requirements

1. Die Area (Mandatory)

Create a die with the **exact dimensions**:

- **Width:** `3.588 mm`
- **Height:** `5.188 mm`

You must explicitly set:

- Die area
- Core area (with reasonable margins)

2. IO Pad Placement (Mandatory)

- Place **IO pads around the die boundary**
- Pads must be:
  - Evenly distributed
  - Properly oriented (top / bottom / left / right)
  - Aligned to edges (no floating pads)

⚠️ *Exact pad order is not important for now, but distribution and correctness are.*

Starting Point (Reference Scripts)

Use the following **ICC2 standalone flow scripts as a learning reference**:

https://github.com/kunalg123/icc2_workshop_collaterals/blob/master/standaloneFlow/top.tcl

Important Notes

- This reference:
  - Uses a **different PDK**
  - Uses a **different design**
- You are **NOT expected** to reproduce the same flow
- You must:
  - Understand the commands
  - Modify them appropriately
  - Adapt them to your SoC and target dimensions

What You Must Do

1. Clone and Study the Reference Script

- Understand:
  - `create_floorplan`
  - Die vs core area
  - Pad placement commands
  - Floorplan visualization

2. Modify the Script for Your Design

Your modified script must:

- Set die area to **3.588 mm × 5.188 mm**
- Define a reasonable core offset
- Place IO pads around all four sides
- Run cleanly in ICC2

3. Stop at Floorplan Stage

You **must NOT**:

- Run placement
- Run CTS
- Run routing
- Add power straps or PDN

This task ends **immediately after floorplan creation**.

Deliverables (Mandatory)

Create a GitHub folder:

```
Task_Floorplan_ICC2/
├── scripts/
│   └── floorplan.tcl
├── reports/
```

```
│   └── floorplan_report.txt
├── images/
│   └── floorplan_screenshot.png
└── README.md
```

README Must Include:

- Die size used
- Core margin used
- IO placement strategy
- What commands were modified from the reference script

Success Criteria

Your submission is considered **complete** if:

- ICC2 runs without errors
- Die size matches **exactly** `3.588mm × 5.188mm`
- IO pads are clearly visible and evenly distributed
- Screenshot clearly shows:
  - Die boundary
  - Core boundary
  - Pad locations

Evaluation Focus

Aspect	Priority
Correct die size	Extremely High
Proper IO pad distribution	Extremely High
Understanding of ICC2 floorplan commands	High
Clean documentation	High

Final Reminder

This is a floorplan-only task.
Do not over-engineer.
Focus on **die size, IO placement, and ICC2 fundamentals**.

This task prepares you for **real SoC physical design flows**, one step at a time.