1. Revision History

Sl. No.	Date	Edited By	Comments
1	15-4-2022	Rajat Raj, Sharat kumar miskin, Naman Bhatia , Huma Tabassum and Jeevita J	Brief description on AMBA-APB
2	17-4-2022	Rajat Raj, Sharat kumar miskin, Naman Bhatia , Huma Tabassum and Jeevita J	Block diagram of the Master-slave and information about working of the master.
3	18-4-2022	Rajat Raj, Sharat kumar miskin, Naman Bhatia , Huma Tabassum and Jeevita J	Information on the operating states and the expected waveforms
4	19-4-2022	Rajat Raj, Sharat kumar miskin, Naman Bhatia , Huma Tabassum and Jeevita J	Design verification and working of two slaves

2 a. Brief description

APB is a low-bandwidth, low-performance bus. The bridge connects the high-performance AHB or ASB bus to the APB bus. As a result, with APB, the bridge serves as the master, while all devices connected to the APB bus serve as slaves.

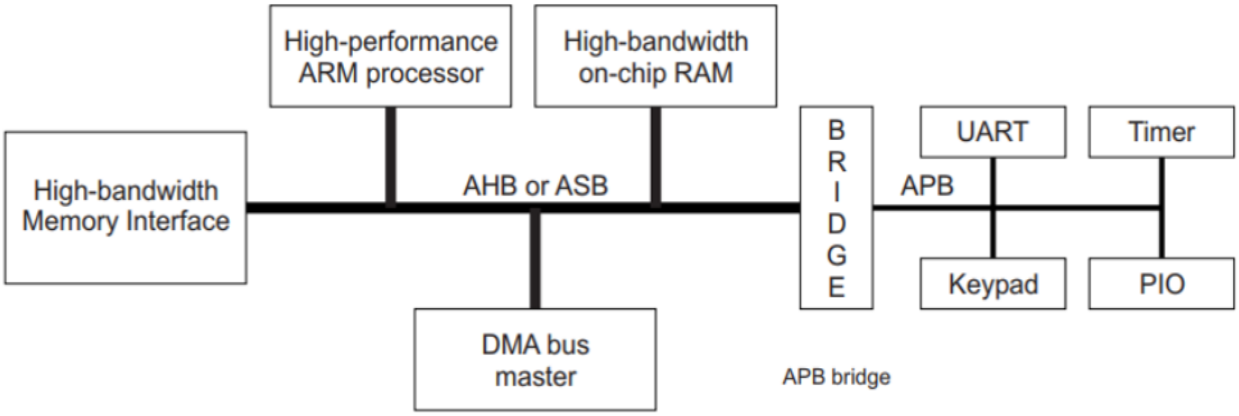

High-performance ARM processor
High-bandwidth on-chip RAM
High-bandwidth Memory Interface
AHB or ASB
DMA bus master
B R I D G E
APB
UART
Timer
Keypad
PIO
APB bridge

Fig: AMBA Architecture

APB Specification

1. Parallel bus operation: At the rising edge clock, all data will be collected.
2. Two slave design.
3. Signal priority: 1.PRESET (active low) 2. PSEL (active high) 3. PENABLE (active high) 4. PREADY (active high) 5. PWRITE
4. Data width 8 bit and address width 9 bit.
5. PWRITE=1 indicates write PWDATA to slave. PWRITE=0 indicates read PRDATA from slave.
6. When PENABLE goes from low to high, data transmission begins. The end of transmission is signaled by a change in PREADY from high to low.

2 b. Block Diagram

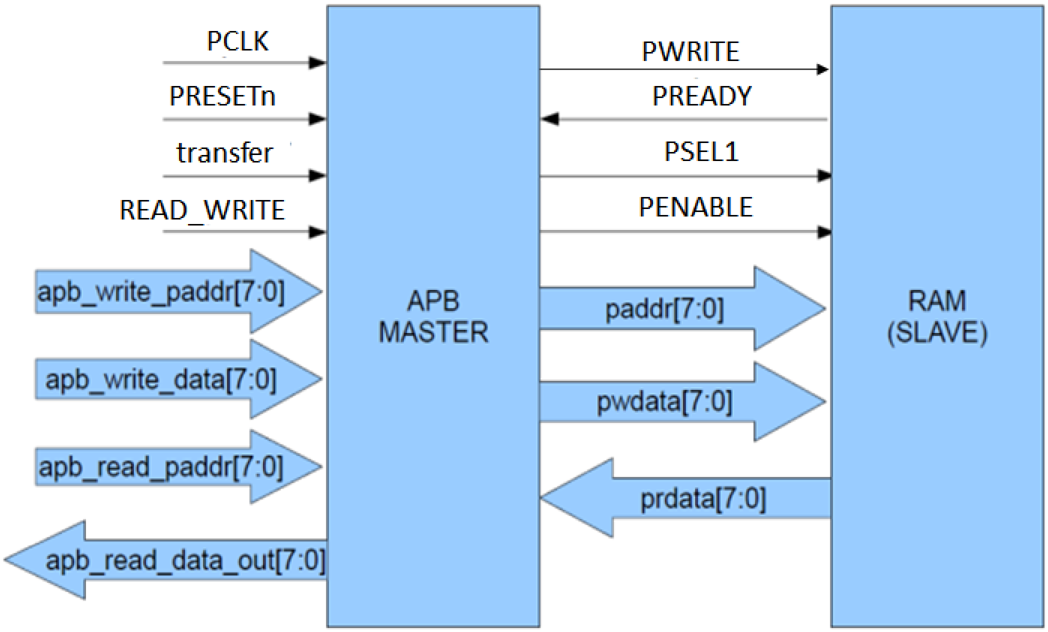


Fig: APB Master Slave Interface

APB protocol is being used to develop a dual port RAM (64 X 8) having one input data line and one output data line. This RAM would be act as APB slave which would be driven by a master present in the APB bridge. The APB slave which we would design as the APB slave would have the following the following signals and functions-

1. Pwrite- This input signal would act as an enable signal of the slave which would tell us if the slave would read or write. Thus, if the Pwrite is equal to 1, the data would be written into the RAM or if it is equal to zero the data would be read from the RAM.
2. PREADY- This signal is present to denote if the slave ie, the RAM is ready to read or write data. Therefore the data would be read or written only if the data ready is 1. It is a output signal of the slave.
3. Psel1- Using this signal we can decide which slave has to be choosen, in this there is only RAM which will be enabled to use when Psel is equal to 1.
4. Penable- An 1 bit input signal given to slave which enables the slave for use
5. Paddr[7:0]- The RAM being designed here takes in 8 address lines as the input therefore, total address locations that can be accessed are 2^(8)=64. This signal is an input to the slave.
6. Pwdata[7:0]- Another 8 bit input signal used to write a 8 bit data onto the slave.
7. Pread[7:0]- Output 8 bit signal used to read a 8 bit data from the slave.

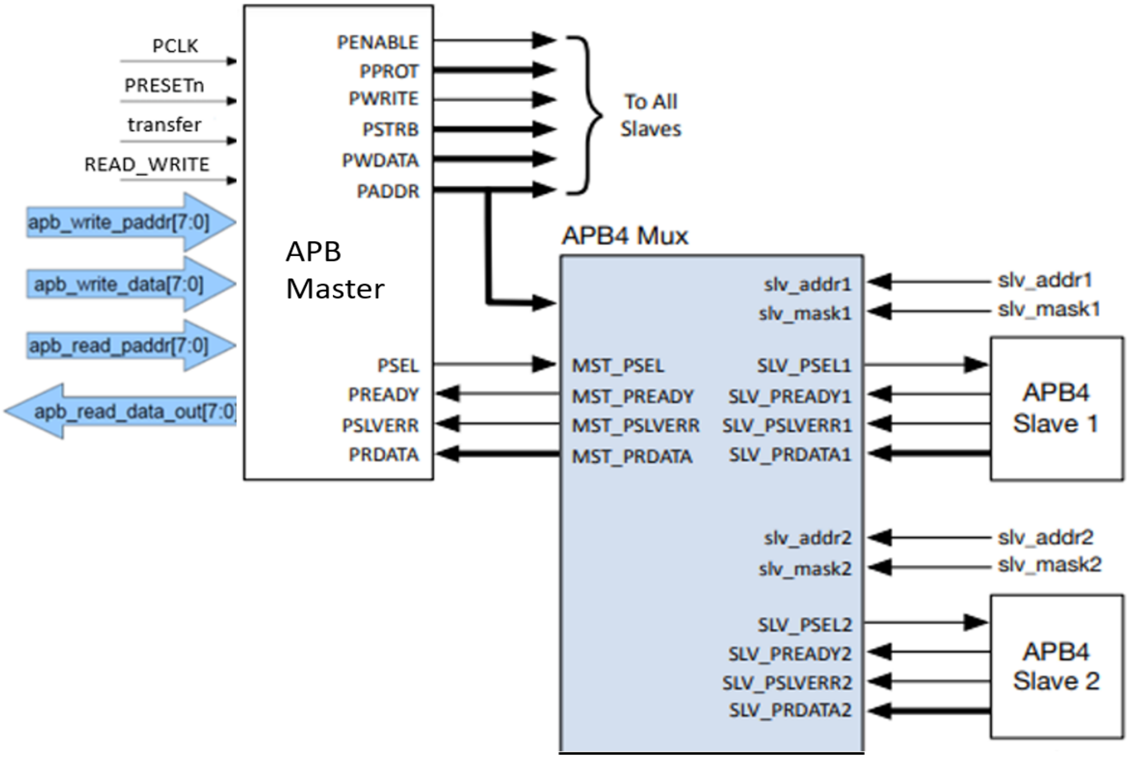


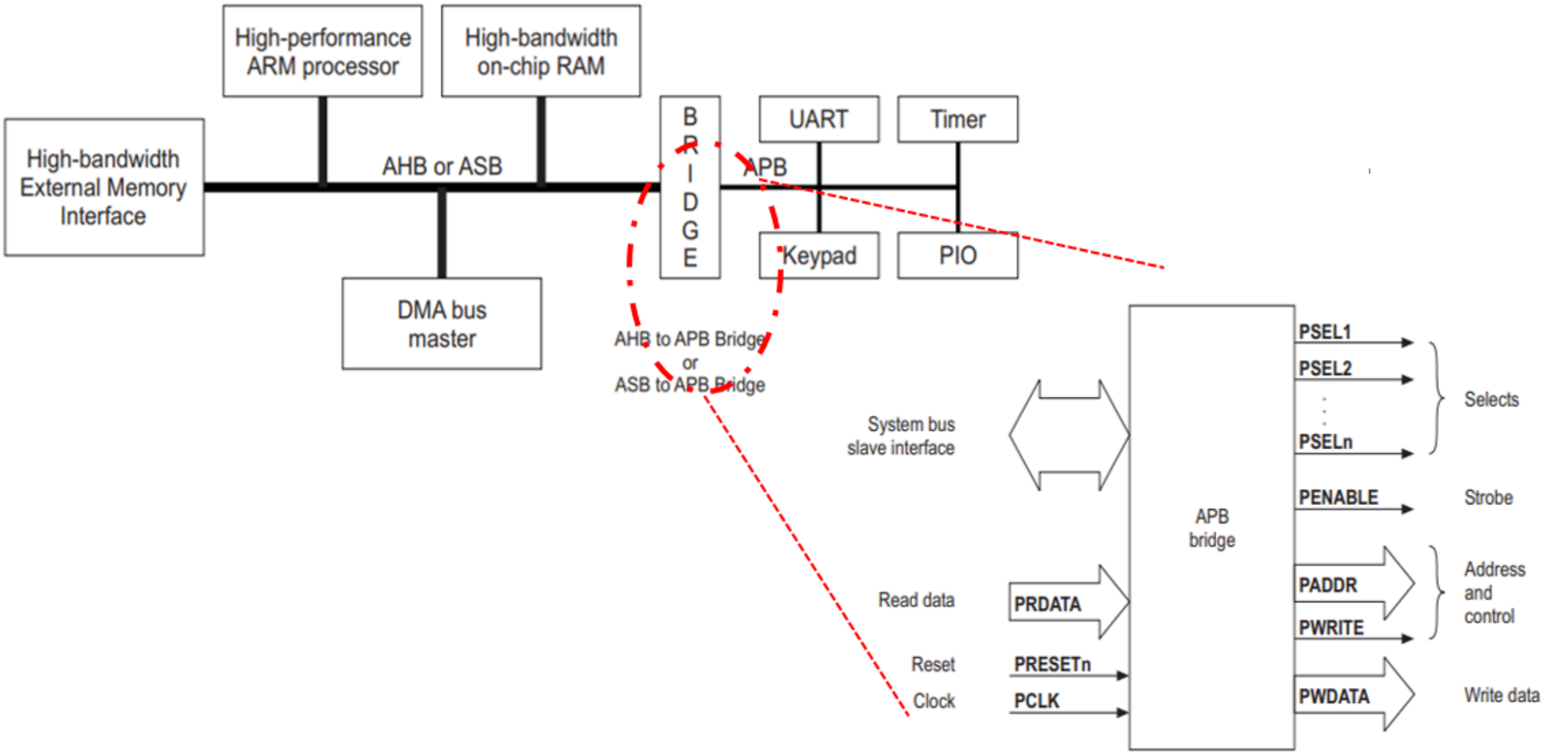
Fig: APB Interface Block Diagram With Slaves

Working of Master-

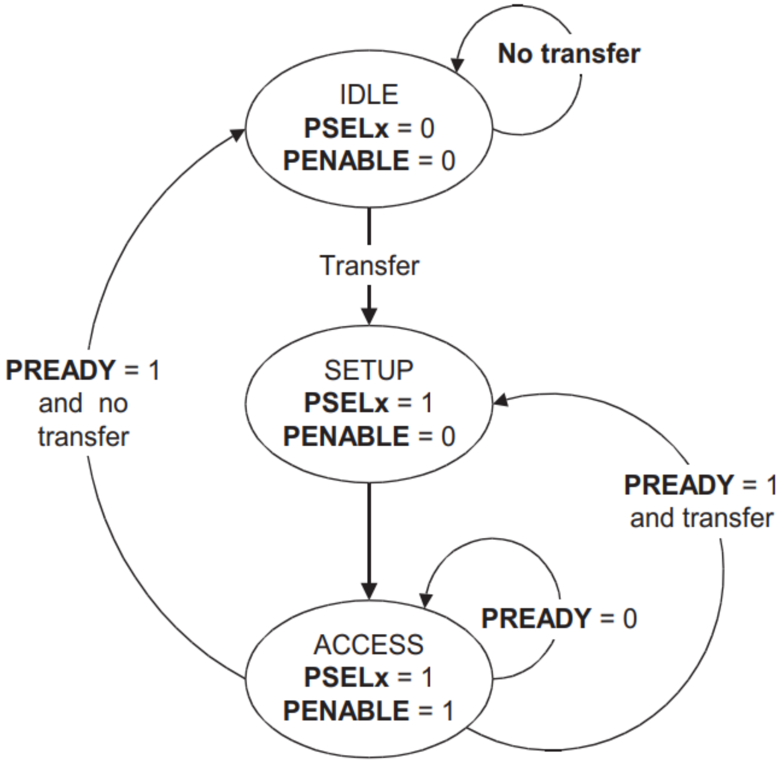
In the AMBA architecture there are mainly two portions present. One follows the AHB protocol that deals with high bandwidth data transmission and the other portion follows APB protocol that deals with low bandwidth data transmission. The bridge in between these two portions contains the AHB slave connected with the APB master responsible for driving the APB slave. The APB master has the following signals-

1) Pselx- This is an output signal from the master to the slave which is used to select the slave which is needed for the operation.
2) Pready- This is an input signal from the slave which tells when the slave is ready to read or write the data.
3) Prdata- This signal is used to read the 8 bit data from the 64X8 bit RAM we are designing in this case.

4) Pslverr- This signal is 1 if the slave gets comes across an error while operating. This signal comes as an input from the slave. PSLVERR is only considered valid during the last cycle of an APB transfer, when PSEL, PENABLE, and PREADY are all HIGH.
5) Penable- Output signal from the master to enable the slave thats has to be used to complete it's operation.
6) Paddr- An output signal from the master that sends the address from which data has to read or written in a case where the slave acts as a RAM.
7) Pwdata- Another output signal to write the data to the location specified by Paddr.
8) Pclk,Present - These signals act as input to the master. The clock provides the frequency of operation and the other signal is used to reset the master whenever its low as it is a octave log the
9) Prdata- An input to master that brings in the data read from the slave.
10) Transfer- This signal is the input to the master which decides whether the APB bus needs to be activated or not.
11) apb_write_paddr/ apb_read_paddr- These two are 8 bit input signals that provide the address from which the data has to be read or written.
12) apb_write_data- 8 bit input signal which sends the data that has to be written into the RAM which acts as a slave.



Operation Of APB

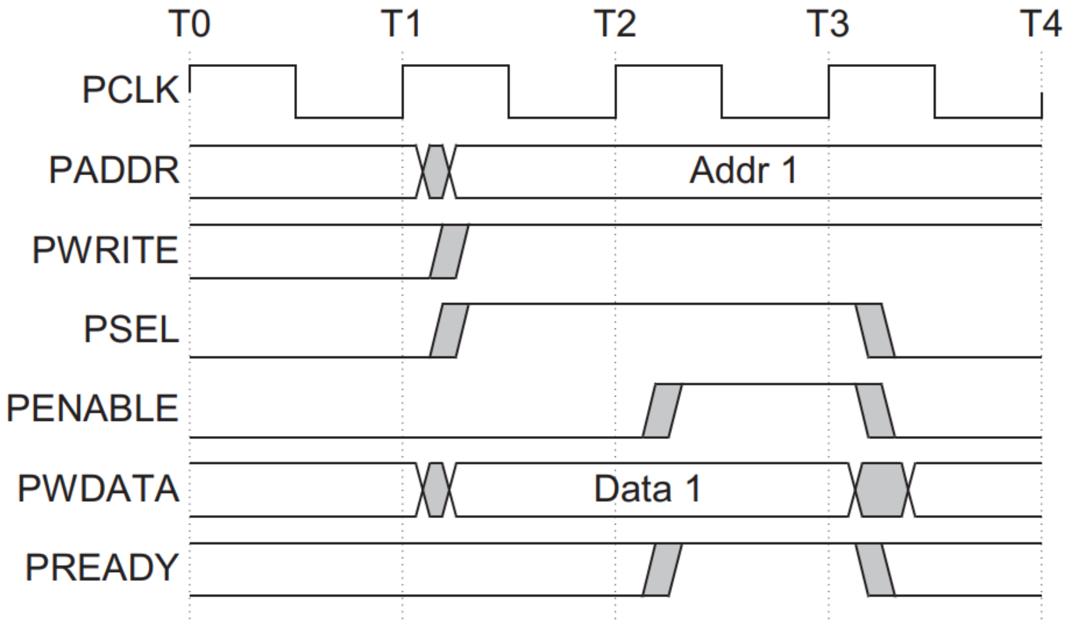


APB PIN Description:

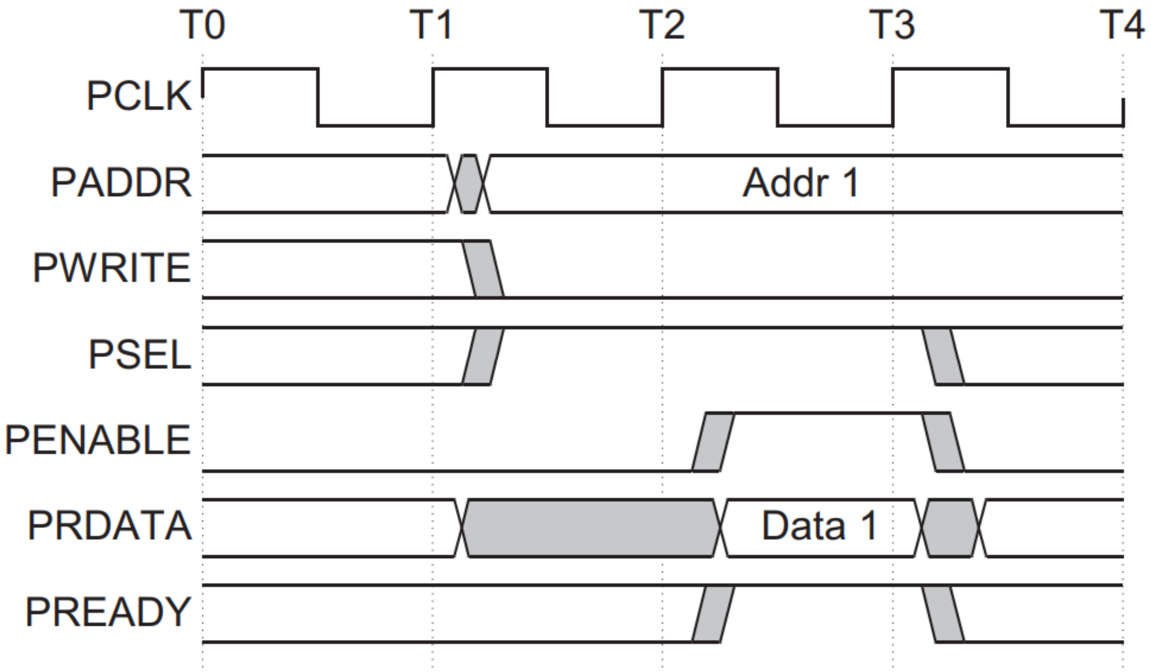
SIGNAL	SOURCE	Description	Bits
Transfer	System Bus	APB enable signal. If high APB is activated else APB is disabled	1
PCLK	Clock Source	All APB functionality occurs at a rising edge.	1
PRESETn	System Bus	An active low signal.	1
PADDR	APB bridge	The APB address bus can be up to 32 bits.	8
PSEL1	APB bridge	There is a PSEL for each slave. It’s an active high signal.	1

PENABLE	APB bridge	It indicates the 2nd cycle of a data transfer. It's an active high signal.	1
PWRITE	APB bridge	Indicates the data transfer direction. PWRITE=1 indicates APB write access(Master to slave) PWRITE=0 indicates APB read access(Slave to master)	1
PREADY	Slave Interface	This is an input from Slave. It is used to enter the access state. If all the conditions for transfer are met then this signal is made high by the slave	1
PSLVERR	Slave Interface	This indicates a transfer failure by the slave.	1
PRDATA	Slave Interface	Read Data. The selected slave drives this bus during reading operation	8
PWDATA	Slave Interface	Write data. This bus is driven by the peripheral bus bridge unit during write cycles when PWRITE is high.	8

Write transfer with no wait states



Read transfer with no wait states



The design verification is done by writing testbenches in verilog HDL.

Initially PRESETn, transfer, READ_WRITE is 0, when we change PRESETn to 1 @ posedge of clock, with transfer is 1 (this implies no write address available but request for write operation).
This will activate the write operation for the slaves.

For write operation, data input is taken as apb_write_data at address apd_write_address.

For READ_WRITE =1, PRESETn=0 and transfer=0, when we change the PRESETn to 1 @ posedge of clk with transfer =1(this implies no read address available but request for read operation).

This will activate the Read operation.

SLAVE 1

INPUTS	PCLK,PRESETn, PSEL, PENABLE, PWRITE, [7:0] PADDR, [7:0]PWDATA
OUTPUTS	[7:0]PRDATA2, PREADY

If PRESETn=0 ⇒ PREADY=0
Else if (PSEL && !PENABLE && !PWRITE)=1 ⇒ PREADY=0

Else if (PSEL && PENABLE && !PWRITE)=1 ⇒ PREADY=1
And input the PADDR on a temporary reg [7:0]reg_addr.

Else if(PSEL && !PENABLE && PWRITE)=1 ⇒ PREADY=0

Else if(PSEL && PENABLE && PWRITE)=1 ⇒ PREADY=1
We will write the data on mem1[PADDR]

Else PREADY=0.

SLAVE 2

INPUTS	PCLK,PRESETn, PSEL, PENABLE, PWRITE, [7:0] PADDR, [7:0]PWDATA
OUTPUTS	[7:0]PRDATA2, PREADY

If PRESETn=0 ⇒ PREADY=0
Else if (PSEL && !PENABLE && !PWRITE)=1 ⇒ PREADY=0

Else if (PSEL && PENABLE && !PWRITE)=1 ⇒ PREADY=1
And input the PADDR on a temporary reg [7:0]reg_addr.

Else if(PSEL && !PENABLE && PWRITE)=1 ⇒ PREADY=0

Else if(PSEL && PENABLE && PWRITE)=1 ⇒ PREADY=1
We will write the data on mem2[PADDR].

Else PREADY=0.

APB MASTER

INPUTS	**[7:0] apb_write_paddr, apb_read_paddr, [7:0] apb_write_data,PRDATA, PRESETn,PCLK,READ_WRITE,transfer,PREADY,**
OUTPUTS	**PSEL1,PSEL2, PENABLE,[7:0]PADDR, PWRITE, [7:0]PWDATA,apb_read_data_out, PSLVERR**

If PRESETn=0 ⇒ State ⇐ IDLE
Else State ⇐ next_state
IDLE STATE
If PENABLE= 0, and no transfer then next_state= IDLE, else next_state is SETUP.
SETUP STATE
If PENABLE =0, with READ_WRITE=1 , APB bridge receives the address of the peripheral register from the ASB from which the ASB wants to read the data from.
PADDR takes the address
Else if READ_WRITE =0 then the APB receives the address and the data of the low bandwidth peripheral register from the ASB to which the ASB wanted to write the data.
PADDR takes the address. PWDATA takes the data to be written
If transfer = 1 and PSLVERR =0 , then the next_state is ACCESS
If transfer = 0 and PSLVERR =1 , then the next_state is IDLE

ACCESS STATE

If transfer and !PSLVERR, when PREADY =1
If READ_WRITE=0 ⇒ next_state is SETUP, apd_data_out = PRDATA

Default state: IDLE

PSLVERR LOGIC

When PRESETn=0

```
        setup_error=0;
        invalid_read_paddr= 0;
        invalid_write_data=0;
        invalid_write_paddr=0;
```

If ((apb_write_data===8'dx) && (!READ_WRITE) && (state==SETUP || state==ENABLE))
⇒ invalid_write_data=1

If((apb_read_paddr===8'dx) && READ_WRITE && (state==SETUP || state==ENABLE))
⇒ invalid_read_paddr=1

if((apb_write_paddr===8'dx) && (!READ_WRITE) && (state==SETUP || state==ENABLE))
⇒invalid_write_paddr =1

If STATE== SETUP

if(PADDR==apb_write_paddr && PWDATA==apb_write_data)=0 ⇒ setup_error=1

if(PADDR==apb_read_paddr)=0 ⇒ setup_error=1

PSLVERR = setup_error || invalid_read_paddr || invalid_write_data || invalid_write_paddr