Design of 9-Transistor Single Bit Full Adder

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ABSTRACT
Here, new low power single bit full adder using 9 transistors has been presented. The proposed adder has the advantage of low power consumption with less area requirements due fewer numbers of transistors. Low power goal has been achieved at circuit level by designing the adder with optimized XNOR gates and multiplexer approach. Direct path between supply voltage and ground have been minimized in the design. The circuits have been simulated in 0.18µm CMOS technology with SPICE. The adder shows power dissipation of 2.0773mW with maximum output delay of 1.86ps at supply voltage of 3.3V. Simulations have been carried out with varying supply voltage 3.3V to 2.7V. Power consumption of proposed full adder has been compared with earlier reported circuits and proposed circuit shows better results.

Keywords
CMOS, exclusive-NOR (XNOR), full adder, power consumption and power delay product.

1. INTRODUCTION
In recent years, rapid growth in mobile communication and other handheld portable devices added rapid research efforts in the field of low power CMOS circuit design. Low power design also increases the operation time of battery operated devices. With added functionality and complexity, numbers of components on integrated circuits are increases and power consumption of VLSI (very large scale integration) circuits is rising exponentially. With increase in power consumption temperature of circuit rises, this further creates reliability problems and performance degradation of the system. Packaging and cooling costs of system also goes high with the rise in temperature and power consumption. Three major sources of power consumption exist in CMOS circuits: 1) dynamic power due to output switching 2) short circuit power due to current between supply voltage and ground during transition 3) static power due to leakage and static currents. Despite the scaling of device dimension and supply voltage, the total power consumption of VLSI circuits is going up due to increase in operating frequency and rise in number of components [1].

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One of the most important operations in computer arithmetic is addition and efficient adders are highly desirable in computer arithmetic. Full adders are the core element of various VLSI circuits like comparators, parity checkers, multiplier and compressors [2]. Improvement in performance of full adder circuit in terms of power consumption, delay and other performance parameters will affect system performance as a whole. Design optimizations at circuit level are highly attractive to improve the performance in terms of power dissipation, delay and output logic level.

A variety of full adder circuits has been reported in literature with diverse techniques and numbers of transistors. Conventional static CMOS full adder implemented with pull up and pull down with NMOS and PMOS networks uses 28 transistors [2],[3]. Complementary pass-transistor logic (CPL) adder with 32 transistors with superior driving capability at the cost of large power dissipation has been presented [4]. Transmission gate CMOS adder (TGA) based on transmission gates with 20 transistors has been reported [5]. Major drawback of TGA is that it employs twice the number of transistors that of PTL (pass transistor logic) for implementations of same logic functionality. Another drawback of CMOS transmission gate is that it needs complementary signals to control gates of PMOS and NMOS transistors. A full adder cell implemented with 14 transistors using XOR and transmission gates has been reported [6]. A transmission function full adder (TFA) with 16 transistors based on transmission function theory has been reported [7]. Multiplexer based adder (MBA) with elimination of direct path to power supply with 12 transistors has been reported [8]. Static energy recovery full (SERF) adder with 10 transistors gives reduced power consumption at the cost of large propagation delay is reported in [9]. Performance analysis of various arithmetic circuits also has been presented [10]. Another design for full adder with XOR/XNOR having 10 transistors has been reported in [11]. Full adder circuits using 22 transistors based on hybrid logic has been presented [12], [13]. In [14] a 16 transistor full adder cell with XOR/XNOR, pass transistors and transmission gate has been reported. Structured approach with disintegration of full adder cell into small modules using XOR/XNOR gates [15] is shown in figure 1. First stage is to generate intermediate XNOR/XOR functions and output of first stage is fed to second stage to generate Sum and C_{out}. With partitioning the full adder cell into small sub-module, Sum and C_{out} (Carry out) signals are obtained as

$$\text{Sum} = H \text{ xor } Cin = H.\ Cin' + H'\ Cin \quad (1)$$

$$Cout = A.\ H' + Cin.\ H \quad (2)$$

Where H is half sum (A xor B) and H' is complement of H.

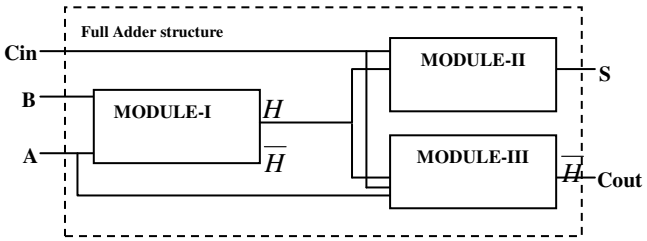


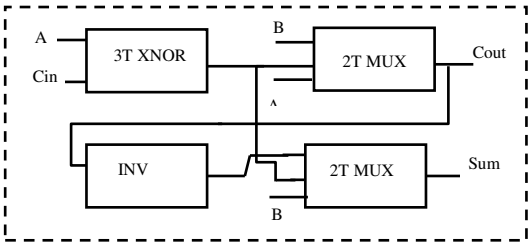
Figure. 1 Structure of single bit full adder

Improvement in design at circuit level can results in reduced power consumption, propagation delay, area with adequate output voltage level. Here, in current work energy efficient single bit full adders using nine and ten transistors have been presented. Full adder cell has been anatomized into smaller modules. Optimized XNOR gates and multiplexer have been used for implementation of proposed adders. Rest of paper is organized as follows: In Section II, novel designs for single bit full adder has been presented. In Section III results of power consumption, maximum output delay and power delay product (PDP) have been obtained. Finally conclusions have been drawn in Section IV.

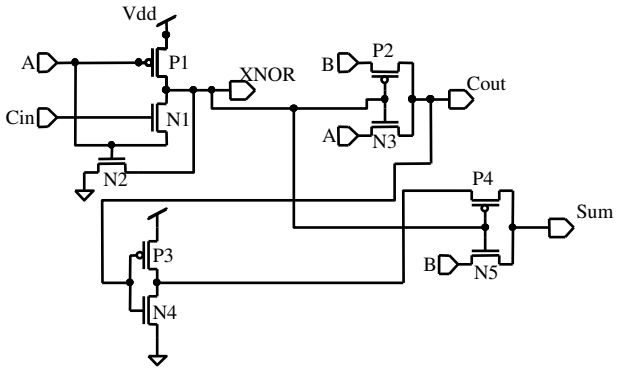
2. SYSTEM DESCRIPTION

The single bit full adder circuit having nine transistors has been implemented with optimized XNOR gate, one inverter and two multiplexer block as shown in figure 2(a). Carry out C_{out} is generated by combination of XNOR and 2T multiplexer. Sum is generated by another two transistors multiplexer with inputs signal B, $\overline{H}$ and $\overline{C_{out}}$ as shown in figure 2(b).

Gate lengths of all transistors have been taken as 0.18µm. In XNOR gate width of transistors P1 has been taken as 0.5µm. Width of transistor N1 and N2 have been taken as 4.0 µm and 0.25µm respectively. Width of PMOS (P2 to P4) transistors used in multiplexer and inverter section has been taken s 5.0µm. Width of NMOS transistors (N3 to N5) has been taken as 4.0µm used in inverter and multiplexer sections.



(a)



(b)

Figure. 2 (a) Block diagram (b) Circuit diagram of 9 transistor adder

3. RESULTS AND DISCUSSIONS

Table I shows the results for power consumption, maximum output delay and power delay product (PDP) of single bit full adder with nine transistors. Simulations have been performed using an input pattern that contains all possible input combination. Input and output waveforms at supply voltage of 3.3V are depicted in figure 3. Circuit of adder is simulated in SPICE using CMOS TSMC 0.18µm technology with supply voltage of [3.3 - 2.7]V. Power consumption of adder varies from [2.0773 to1.1402] mW with variation of supply voltage [3.3 – 2.7] V. Output delay a shows variation of [1.86 to 2.82] ps.

Table 1. Power consumption, delay and PDP of 9T adder

Supply voltage (V)	Power consumption (mW)	Maximum output delay(ps)
3.3	2.0773	1.86
3.2	1.8984	1.89
3.1	1.7289	1.91
3.0	1.5684	1.93
2.9	1.4170	1.93
2.8	1.2743	2.82
2.7	1.1402	2.82

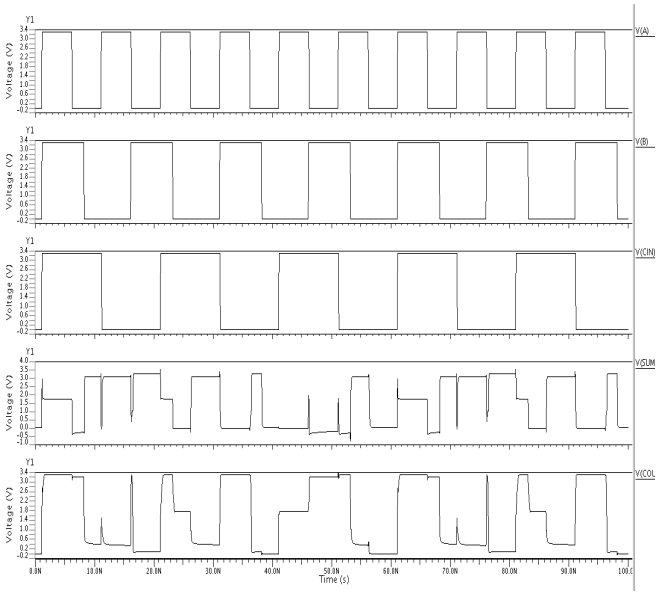


Figure.3 Input and output waveforms for 9T adder at 3.3 V

Figure 4 show that power consumption variation for proposed adder with supply voltage variations. Figure 5 shows the variation of output delay of proposed circuit with power supply variations. Finally the figure 6 shows power versus delay variations. The designed circuit has the advantage of low power consumption due to less number of transistors and elimination of direct path to ground from supply voltage. With reduced numbers of transistors, magnitudes and numbers of internal node capacitances reduces which have great effect on power consumption. Power consumption during charging and discharging of nodes also decreases due to less capacitance**.**

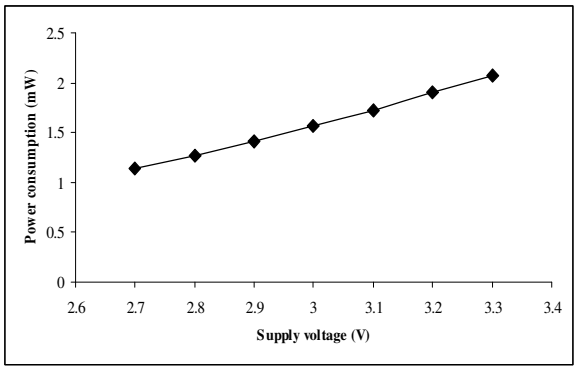


Figure. 4 Power consumption variations of proposed adder with supply voltage

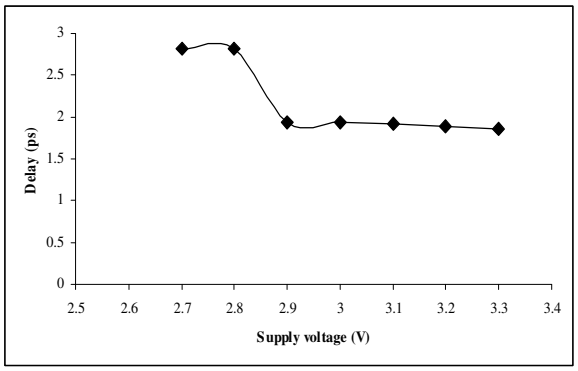


Figure. 5 Output delay variations of proposed adder with supply voltage

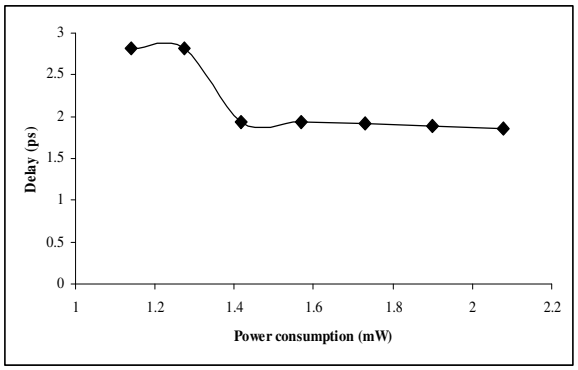


Figure. 6 Power versus delay variations of proposed adder

Earlier reported adder circuits namely TGA, 16T, 22T, 18T, 10T have been prototyped in 0.18µm technology and simulated in SPICE with same input pattern as for proposed adders. Table 2 shows comparisons of power consumption of proposed circuit with earlier reported circuits.

Table 2. Power consumptions comparisons with earlier reported circuits

Adder configuration	Power consumption	Numbers of transistors
20T TGA[7]	357.5880µW	20
16T [14]	167.2136µW	16
22T [12]	533.9007µW	22
18T [3]	548.257µW	18
10T SERF[9]	152.9083µW	10
Present work [9T adder]	2.0773mW	9

4. CONCLUSIONS

New design for low power single bit full adder cell has been presented. The adder design is based on optimized XNOR circuit with combinations of inverter and multiplexer blocks.

Proposed circuit shows power consumption of 2.0773mW with maximum output delay of 1.86 ps with supply voltage of 3.3V. Adder performance has been obtained for varying supply voltage from 3.3V to 2.7V. Comparisons with earlier reported circuits have been made and the new cell outperforms the earlier reported circuits in terms of power consumption.

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