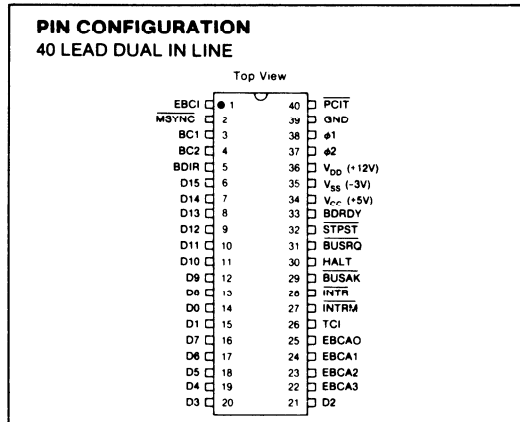# 16-Bit Microprocessor

FEATURES

- 8 program accessible 16-bit general purpose registers
- 86 basic instructions
- 4 addressing modes: immediate, direct, indirect, relative
- Conditional branching on status word and 16 external conditions
- Unlimited interrupt nesting and priority resolution
- 16-bit logic and 2's complement arithmetic
- Status logic and word: carry, overflow, sign, zero
- Direct memory access (DMA) for high speed data transfer
- 64K memory using single address
- TTL compatible/simple bus structure
- CP1610: $1\mu s$ cycle time, 2MHz 2 phase clock

DESCRIPTION

The CP1610 is a compatible member of the Series 1600 Microprocessor products family. It is a complete, 16-bit, single chip, high speed MOS-LSI Microprocessor. The Series 1600 family is fabricated with the General Instrument N-Channel Ion-Implant process, insuring high performance with proven reliability and production history. All members of the Series 1600 family are fully compatible with the CP1610.

The Microprocessor has been designed for high speed data processing and real time applications. Typical applications include programable TV games, home computer systems/home information centers, programable calculator systems, peripheral controllers, process controllers, intelligent terminals and instruments, data acquisition and digital communications processors, numerical control systems and many general purpose mini-computer applications. The Microprocessor can readily support a variety of peripheral equipment such as TTY, CRT display, tape reader/punch, A/D & D/A converter, keyboard,

PIN CONFIGURATION
40 LEAD DUAL IN LINE

Top View

EBCI	1		40	PCIT
MSYNC	2		39	GND
BC1	3		38	⌀1
BC2	4		37	⌀2
BDIR	5		36	V_{DD} (+12V)
D15	6		35	V_{SS} (-3V)
D14	7		34	V_{CC} (+5V)
D13	8		33	BDRDY
D12	9		32	STPST
D11	10		31	BUSRQ
D10	11		30	HALT
D9	12		29	BUSAK
D8	13		28	INTR
D0	14		27	INTRM
D1	15		26	TCI
D7	16		25	EBCAO
D6	17		24	EBCA1
D5	18		23	EBCA2
D4	19		22	EBCA3
D3	20		21	D2

cassette tape, floppy disk, and RS-232C data communication lines.

The CP1610 utilizes third generation minicomputer architecture with eight general purpose registers to achieve a versatile, sophisticated microcomputer system. The 16-bit word enables fast and efficient processing of alphanumeric or byte oriented data. The 16-bit address capability permits access to 65,536 words in any combination of the program memory, data memory, or peripheral devices. This single address space concept, combined with a powerful instruction set, provides an efficient solution to microcomputer and many minicomputer-based product requirements.

CP1610 SYSTEM DIAGRAM
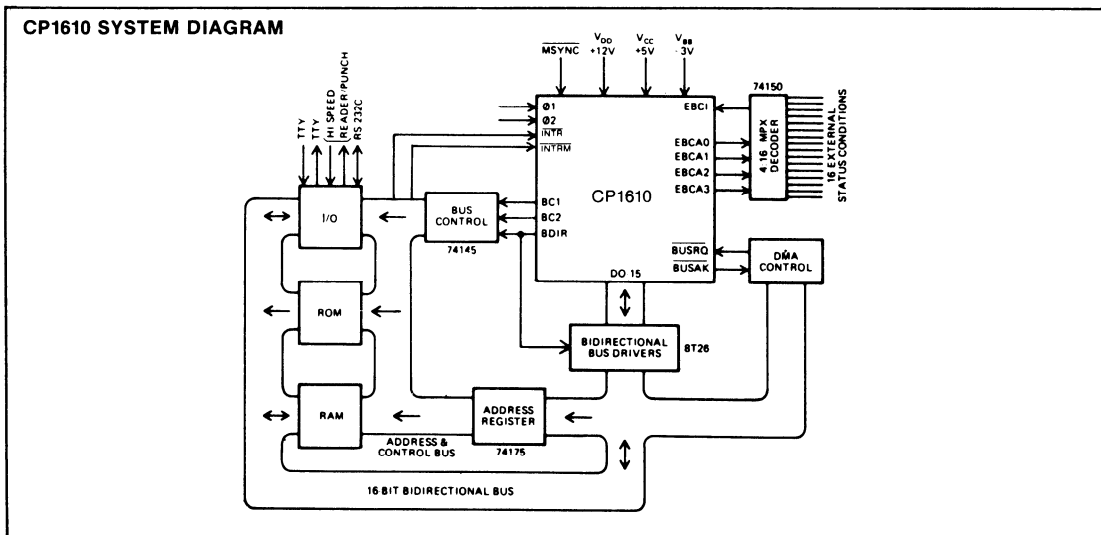
PROCESSOR SIGNALS

DATA BUS

D0-D15
Input/Output/High Impedance

Data 0-15: 16-bit bidirectional bus used to transfer data, addresses, and instructions between the microprocessor, memory, and peripheral devices.

PROCESSOR CONTROL

STPST
Input
SToP-STart: Edge-triggered by negative transition; used to control the running condition of the microprocessor.

HALT
Output
HALT: indicates that the microprocessor is in a stopped mode.

MSYNC
Input
Master SYNC: Active low input synchronizes the microprocessor to the $\phi1$, $\phi2$ clocks during power-up initialization.

EBCA 0-3
Outputs
External Branch Condition Addresses 0-3: Address for one-of-16 external digital state tests via the BEXT (Branch on EXTernal) instruction.

EBCI
Input
External Branch Condition Input: Return signal from the one-of-16 selection made by EBCA 0-3.

BUS CONTROL

BDIR, BC1, BC2
Outputs
Bus DIRection, Bus Controls 1, 2: Bus control signals externally decoded to define the state of bus operations (see State Flow Diagram).

BUSRQ
Input
BUSAK
Output
BUS ReQuest, BUS AcKnowledge: BUSRQ* requests the microprocessor to relinquish control of the bus indefinitely. BUSAK* informs devices that the bus has been released.

BDRDY
Input
Bus Data ReaDY: causes the microprocessor to "wait" and resynchronize to slow memory and peripheral devices.

INTR , INTRM
INTeRupt, INTeRupt Masked: request the microprocessor to service an interrupt upon completion of current instruction.

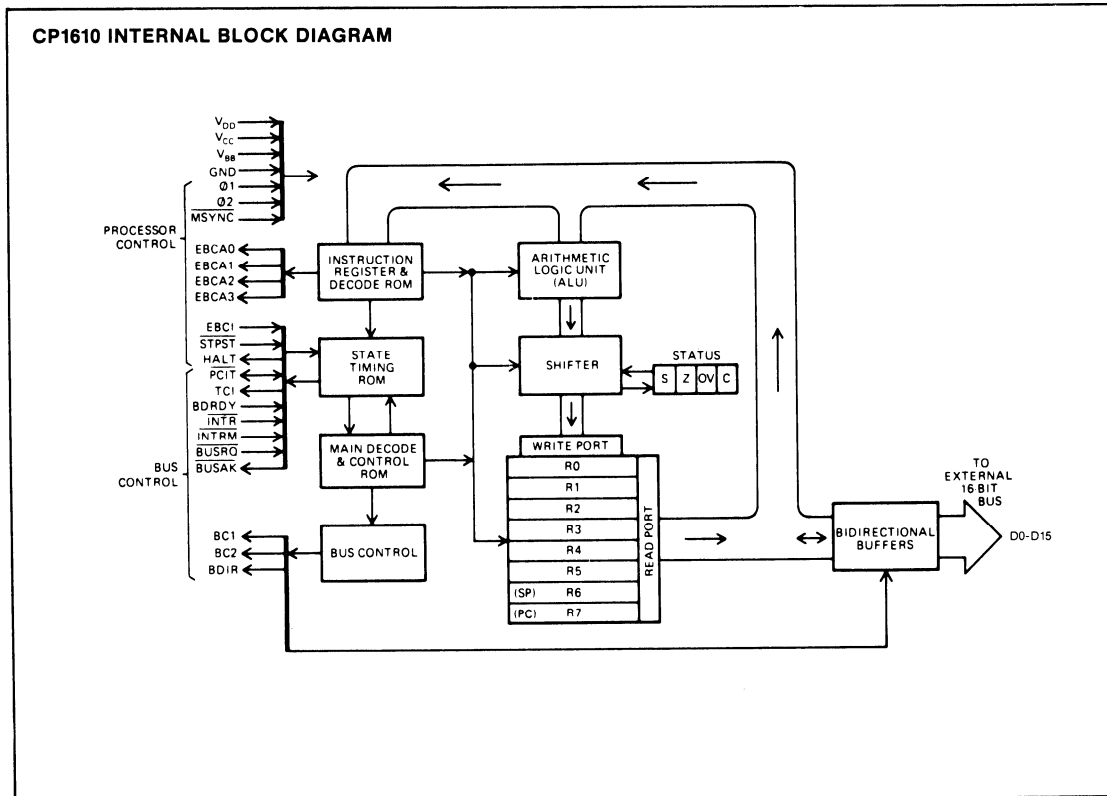**TCI**
Output
Terminate Current Interrupt: pulse outputted by the microprocessor in response to the TCI instruction.
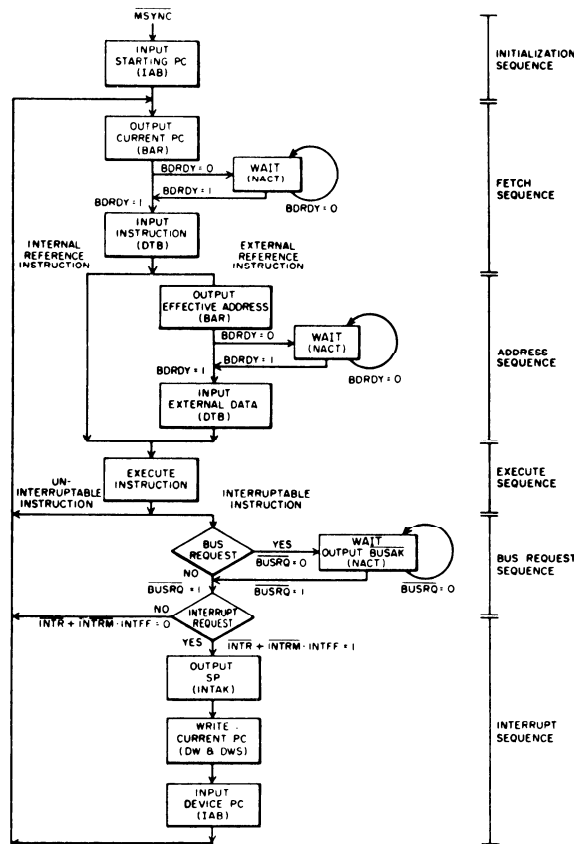
PCIT
Input/output
Program Counter Inhibit/Trap: As an input, inhibits incrementation of the Program Counter during the instruction fetch sequence. As an output, generates a pulse during execution of a Software INterrupt (SIN) instruction.

CP1610 INTERNAL BLOCK DIAGRAM

SIMPLIFIED STATE FLOW DIAGRAM

MSYNC

INPUT
STARTING PC
(IAB)

— INITIALIZATION SEQUENCE

OUTPUT
CURRENT PC
(BAR)

BDRDY = 0 → WAIT (NACT) ↺ BDRDY = 0

BDRDY = I

BDRDY = I

INPUT
INSTRUCTION
(DTB)

— FETCH SEQUENCE

INTERNAL REFERENCE INSTRUCTION   EXTERNAL REFERENCE INSTRUCTION

OUTPUT
EFFECTIVE ADDRESS
(BAR)

BDRDY = 0 → WAIT (NACT) ↺ BDRDY = 0

BDRDY = I   BDRDY = I

INPUT
EXTERNAL DATA
(DTB)

— ADDRESS SEQUENCE

EXECUTE
INSTRUCTION

UN-INTERRUPTABLE INSTRUCTION   INTERRUPTABLE INSTRUCTION

— EXECUTE SEQUENCE

BUS REQUEST — YES → WAIT OUTPUT BUSAK (NACT) ↺ BUSRQ = 0

BUSRQ = 0

NO

BUSRQ = I   BUSRQ = I   BUSRQ = 0

— BUS REQUEST SEQUENCE

NO
INTR + INTRM · INTFF = 0

INTERRUPT REQUEST

YES   INTR + INTRM · INTFF = I

OUTPUT
SP
(INTAK)

WRITE
CURRENT PC
(DW & DWS)

INPUT
DEVICE PC
(IAB)

— INTERRUPT SEQUENCE

BUS CONTROL SIGNALS

BDIR	BC2	BC1	Signal	Decoded Function
0	0	0	NACT	No ACTion, D0-D15 = high impedance
0	0	1	ADAR	Address Data to Address Register, D0-D15 = high impedance
0	1	0	IAB	Interrupt Address to Bus, D0-D15 = Input
0	1	1	DTB	Data To Bus, D0-D15 = Input
1	0	0	BAR	Bus to Address Register
1	0	1	DW	Data Write
1	1	0	DWS	Data Write Strobe
1	1	1	INTAK	INTerrupt AcKnowledge

VIDEO

INSTRUCTION SET (SUMMARY LISTING)

		Mnemonics	Operation	Microcycles				Comments
INTERNAL REFERENCE INSTRUCTIONS	**Register to Register**	MOVR	MOVe Register	6/7				MOVR to itself
		TSTR	TeST Register	6/7				MOVR to PC
		JR	Jump to address in Register	7				
		ADDR	ADD contents of Registers	6				
		SUBR	SUBtract contents of Registers	6				
		CMPR	CoMPare Registers by subtr.	6				Results not stored
		ANDR	logical AND Registers	6				
		XORR	eXclusive OR Registers	6				
		CLRR	CLeaR Register	6				XORR with itself
	Single Register	INCR	INCrement Register	6				
		DECR	DECrement Register	6				
		COMR	COMplement Register	6				One's Complement
		NEGR	NEGate Register	6				Two's Complement
		ADCR	ADd Carry Bit to Register	6				
		GSWD	Get Status WorD	6				
		NOP	No OPeration	6				
		SIN	Software INterrupt	6				Pulse to $\overline{PCIT}$ pin
		RSWD	Return Status WorD	6				
	Register Shift	SWAP	SWAP 8-bit bytes	6	Add two cycles for 2-position shift			Not interruptable. One or two position shift capability. Two position SWAP not supported.
		SLL	Shift Logical Left	6				
		RLC	Rotate Left thru Carry	6				
		SLLC	Shift Logical Left thru Carry	6				
		SLR	Shift Logical Right	6				
		SAR	Shift Arithmetic Right	6				
		RRC	Rotate Right thru Carry	6				
		SARC	Shift Arithmetic Right thru Carry	6				
	Control Instructions	HLT	HaLT	4				Must precede external reference to double byte data
		SDBD	Set Double Byte Data	4				
		EIS	Enable Interrupt System	4				
		DIS	Disable Interrupt System	4				
		TCI	Terminate Current Interrupt	4				Not interruptable
		CLRC	CLeaR Carry to zero	4				
		SETC	SET Carry to one	4				
	Jump Instructions	J	Jump	12				
		JE	Jump, Enable, interrupt	12				
		JD	Jump, Disable interrupt	12				
		JSR	Jump, Save Return	12				Return Address saved in R4, 5 or 6.
		JSRE	Jump, Save Return & Enable	12				
		JSRD	Jump, Save Return & Disable interrupt	12				
EXTERNAL REFERENCE INSTRUCTIONS	**Conditional Branch Instructions**	B	unconditional Branch	9*	Add 2 cycles if test condition is true, except *			Two words
		NOPP	No OPeration	7*				C=1
		BC (BLGE)	Branch on Carry	7				C=0
		BNC (BLLT)	Branch on No Carry	7				OV=1
		BOV	Branch on OVerflow	7				OV=0
		BNOV	Branch on No OVerflow	7				S=0
		BPL	Branch on PLus	7				S=1
		BMI	Branch on Minus	7				Z=1
		BZE (BEQ)	Branch on ZEro or EQual	7				Z=0
		BNZE (BNEQ)	Branch if Not ZEro or Not EQual	7				S∀OV=1
		BLT	Branch if Less Than	7				S∀OV=0
		BGE	Branch if Greater than or Equal	7				ZV(S∀OV)=1
		BLE	Branch if Less than or Equal	7				ZV(S∀OV)=0
		BGT	Branch if Greater Than	7				C∀S=1
		BUSC	Branch if Sign ≠ Carry	7				C∀S=0
		BESC	Branch if Sign = Carry	7				4 LSB of instruction are decoded select 1 of 16 external conditions.
		BEXT	Branch if External condition is True	7				

(right margin notes for Conditional Branch: Displacement in PC+1, PC→PC±Displacement)

				Dir.	Imm.	Indir.	Stack	
	I/O	MVO	MoVe Out	11	9	9	9	Not interruptable
		PSHR	PuSH Register to stack	—	—	—	9	PSHR=MVO@R6. Not interruptable
		MVI	MoVe In	10	8	8	11	
		PULR	PULl from stack to Register	—	—	—	11	PULR=MVI@R6.
	Arithmetic & Logic	ADD	ADD	10	8	8	11	
		SUB	SUBtract	10	8	8	11	
		CMP	CoMPare	10	8	8	11	Result not saved
		AND	logical AND	10	8	8	11	
		XOR	eXclusive OR	10	8	8	11	

1 MICROCYCLE = 2 CLOCK CYCLES

VIDEO

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{DD}, V_{CC}, GND and all other Input/Output Voltages
with Respect to V_{BB} .... −0.3V to +18.0V
Storage Temperature .... −55°C to +150°C
Operating Temperature .... 0°C to +70°C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions: (unless otherwise noted)
V_{DD}=+11V±5%, 70mA(typ) , 110mA(max.) V_{BB} = −2.2V ± 5%, 0.2mA(typ), 2mA(max.)
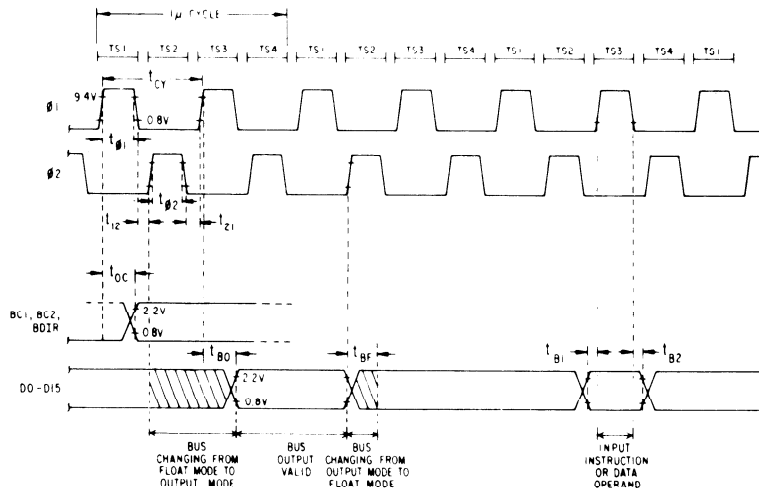V_{CC}=+5V±5%, 12mA(typ) , 25mA(max.)   Operating Temperature (T_A)=0°C to +70°C

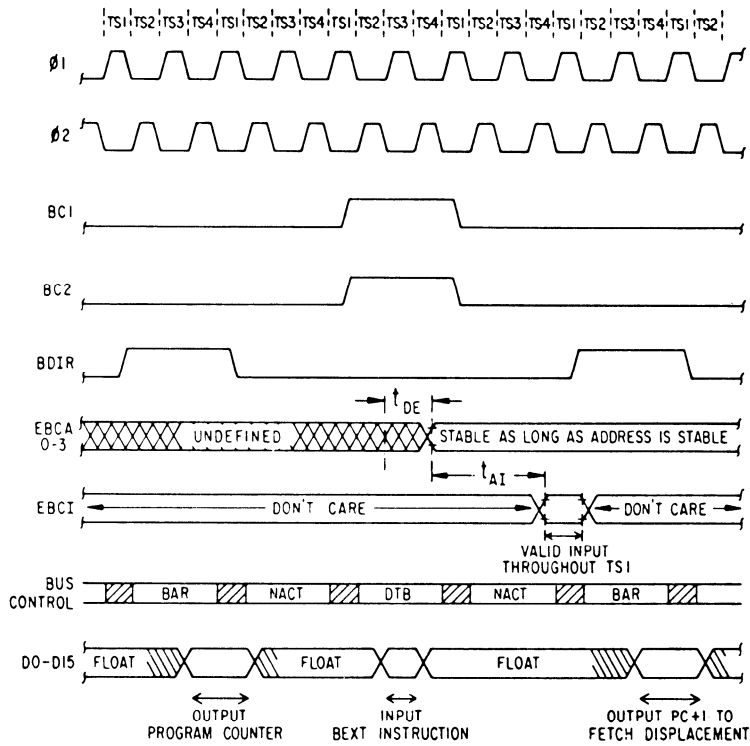| Characteristic	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
Clock Inputs						
High	V_{IHC}	10	—	V_{DD}	V	
Low	V_{ILC}	0	—	0.6	V	
Input current	I_C	—	—	15	mA	$V_{IHC} = (V_{DD} -1)V$
Logic Inputs						
Low	V_{IL}	0	—	0.65	V	
High (All Lines except BDRDY)	V_{IH}	2.4	—	V_{CC}	V	
High (Bus Data Ready Line See Note)	V_{IHB}	3	—	V_{CC}	V	
Logic Outputs						
High	V_{OH}	2.4	V_{CC}	—	V	$I_{OH} = 100\mu A$
Low (Data Bus Lines D0-D15)	V_{OL}	—	—	0.5	V	$I_{OL} = 1.6mA$
Low (Bus Control Lines, BC1,BC2,BDIR)	V_{OL}	—	—	0.45	V	$I_{OL} = 2.0mA$
Low (All Others)	V_{OL}	—	—	0.45	V	$I_{OL} = 1.6mA$
AC CHARACTERISTICS						
Clock Pulse Inputs, ϕ1 or ϕ2						
Pulse Width	$t\phi2, t\phi2$	250		—	ns	
Skew (ϕ1, ϕ2 delay)	t_{12}, t_{21}	0	—	—	ns	
Clock Period	t_{cy}	0.5	—	2	μs	
Rise & Fall Times	tr, tf	—	—	15	ns	
Master SYNC:						
Delay from ϕ	tms	—	—	30	ns	
D0-D15 Bus Signals						
Output delay from ϕ1 (float to output)	t_{BO}	—	—	100	ns	1 TTL Load & 100pF
Output delay from ϕ2 (output to float)	t_{BF}	—	50	—	ns	
Input setup time before ϕ1	t_{B1}	0	—	—	ns	
Input hold time after ϕ1	t_{B2}	10	—	—	ns	
Bus Control Signals BC1,BC2,BDIR						
Output delay from ϕ1	t_{DC}	—	—	100	ns	
Skew		—	—	30	ns	
BUSAK Output delay from ϕ1	t_{BU}	—	150	—	ns	
TCI Output delay from ϕ1	t_{TO}	—	200	—	ns	
TCI Pulse Width	t_{TW}	—	300	—	ns	
EBCA output delay from BEXT input	t_{DE}	—	—	150	ns	
EBCA wait time for EBCI input	t_{AI}	—	—	400	ns	
CAPACITANCE						TA = +25°C; V_{DD} = +12V; V_{CC} = +5V; V_{BB} = −3V; tϕ1 = tϕ2 = 120ns
ϕ1, ϕ2 Clock Input capacitance	Cϕ1, Cϕ2	—	20	30	pF	
D0-D15		—	8	15	pF	
All Other		—	5	10	pF	

**Typical values are at +25°C and nominal voltages.
NOTE: The Bus Data ReaDY(BDRDY) line is sampled during time period TSI after a BAR or ADAR bus control signal. BDRDY must go low requesting a wait state 50 ns before the end of TS1 and remain low for 50 ns minimum. BDRDY may go high asynchronously. In response to BDRDY, the CPU will extend bus cycles by adding additional microcycles up to a maximum of 40 μsec duration.

VIDEO

CLOCK AND BUS TIMING

BUS CHANGING FROM FLOAT MODE TO OUTPUT MODE

BUS OUTPUT VALID

BUS CHANGING FROM OUTPUT MODE TO FLOAT MODE

INPUT INSTRUCTION OR DATA OPERAND

TYPICAL INSTRUCTION SEQUENCE (EXTERNAL BRANCH TIMING)

EBCA 0-3   UNDEFINED   STABLE AS LONG AS ADDRESS IS STABLE

EBCI   DON'T CARE   DON'T CARE

VALID INPUT THROUGHOUT TS1

BUS CONTROL   BAR   NACT   DTB   NACT   BAR

DO-DI5   FLOAT   FLOAT   FLOAT

OUTPUT PROGRAM COUNTER

INPUT BEXT INSTRUCTION

OUTPUT PC+1 TO FETCH DISPLACEMENT

LEGEND: DO-DI5 BUS CHANGING DIRECTION

VIDEO