CS224
Lab 6
Section 4

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7/12/2024

QUESTION 1)

Assume that main memory size is 4GB.

Index Size: No. of bits needed to express the set number in an address

Block Offset: No. of bits needed to indicate the word offset in a block

Byte Offset: No. of bits needed to indicate the byte offset in a word.

Word Block Offset Size in bits: Log2(No. of words in a block)

Byte Offset Size in bits: Log2(No. of bytes in a word)

Block Replacement Policy Needed: Indicate if a block replacement policy such as FIFO, LRU, LFU etc. is needed (yes) or not (no). If some combinations are not possible mark them.

No.	Cache Size KB	N way cache	Word Size	Block size (no. of words)	No. of Sets	Tag Size in bits	Index Size (Set No.) in bits	Word Block Offset Size in Bits)	Byte Offset Size in bits2	Block Replacement Policy Needed
1	64	1	32 bits	4	4096	16	12	2	2	No
2	64	2	32 bits	4	2048	17	11	2	2	Yes
3	64	4	32 bits	8	512	18	9	3	2	Yes
4	64	Full	32 bits	8	1	27	0	3	2	Yes
9	128	1	16 bits	4	16384	15	14	2	1	No
10	128	2	16 bits	4	8192	16	13	2	1	Yes
11	128	4	16 bits	16	1024	17	10	4	1	Yes
12	128	Full	16 bits	16	1	27	0	4	1	Yes

QUESTION 2)
Cache Capacity: 8 words
Block Size: 2 words
N = 1

```
      addi $t0, $0, 5
loop: beq $t0, $0, done
      lw $t1, 0x4($0)
      lw $t2, 0xC($0)
      lw $t3, 0x8($0)
      addi $t0, $t0, -1
      j loop
done:
```

a) Indicate the type of miss, if any: Compulsory, Conflict, Capacity.

Instruction	**Iteration No.**				
	1	**2**	**3**	**4**	**5**
lw $t1, 0x4($0)	Compulsary				
lw $t2, 0xC($0)	Compulsary				
lw $t3, 0x8($0)					

b) What is the total cache memory size in number of bits? Include the V bit your calculations. Show the details of your calculation

Tag part has 27 bits as byte offset = 2 bits (word = 32 bits), block offset = 1 bit (as block size is 2) and index size = 2 bits as there are 4 sets. 27 = 32-2-1-2

Valid bit = 1 bit. And there are 64 bit for data part (2 word). Total bit in a block is 1(V) + 27(Tag) +64(Data)= 92 bits. There are 4 sets = $92 \cdot 4 =$ *368 bits*.

c) State the number of AND and OR gates, EQUALITY COMPARATORs and MULTIPLEXERs needed to implement the cache memory.

Number of Equality Comparator = 1
Number of And Gates =1
Number of Or Gates =0
Number of multiplexers: 1 2-to-1 mux

QUESTION 3)
Consider the above MIPS code segment.
Cache capacity: 2 words
Block size: 1 word.
There is only 1 set.
The block replacement policy is LRU.

a) Indicate the type of miss, if any: Compulsory, Conflict, Capacity.

Instruction	**Iteration No.**				
	1	**2**	**3**	**4**	**5**
lw $t1, 0x4($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t2, 0xC($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t3, 0x8($0)	Compulsory	Capacity	Capacity	Capacity	Capacity

b) How many bits are needed for the implementation of LRU policy? What is the total cache memory size in number of bits? Include the V bit and the bit(s) used for LRU in your calculations. Show the details of your calculation.

Number of bits to implement LRU policy: 1 as there are 2 words and it can be specified with 1 bit. If the data in first block is used recently its LRU bit is made 0 , otherwise it is made 1.

Total bits in a block: Valid bit = 1, Tag bit = 30 bit, Data part = 32 bit. And we have 2 block, and also a LRU bit. ((1+30+32)*2)+1 = *127 bits*.

c) State the number of AND and OR gates, EQUALITY COMPARATORs and MULTIPLEXERs needed to implement the cache memory.

Number of Equality Comparator =2.
Number of And Gates =2.
Number of Or Gates =1.
Number of multiplexers: 1 2-to-1 Mux.

QUESTION 4)

Consider a three level memory: L1 and L2 are for cache memory and the third level is for the main memory. Access time for L1 is 1 clock cycle, the access time for L2 is 4 times more than L1 and main memory access time is 10 times more than L2. The miss rate for L1 is 20% and the miss rate for L2 is 5%. What is the effective clock cycle for memory access (AMAT in number of clock cycles)?

With 4 GHz clock rate how much time is needed for a program with 10^{12} instructions to execute?

I've assumed L2 is 5 as it says 4 times more than L1.

$$\text{AMAT(clock cycle)} = t_{L1} + MR_{L1}(t_{L2} + MR_{L2}(t_{MM}))$$
$$= 1 + 0.2(5 + 0.05(55))$$
$$= 2.55$$

Execution Time = Total Cycles / Clock Rate

Total Cycles = Number of Instructions × AMAT = $10^{12} \times 2.55 = 255 \times 10^{10}$

Clock Rate = 4×10^9

Execution Time = $(255 \times 10^{10}) / (4 \times 10^9) = 2550 / 4 = 637.5$ second