CS223

DIGITAL DESIGN

PROJECT

Basys3 Simple Calculator with SystemVerilog

İREM SEVEN

21704269

Section: 2

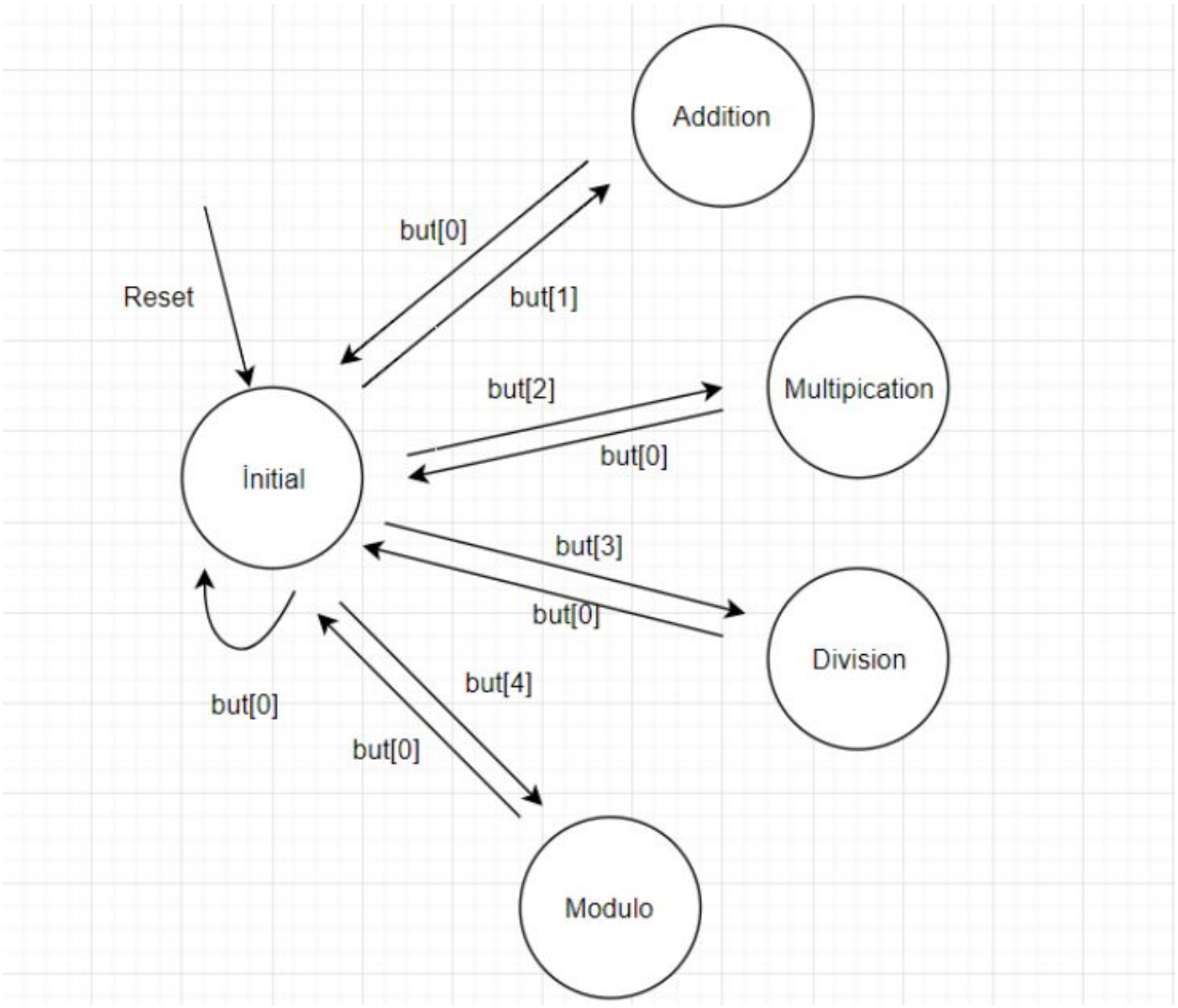
Date: 13.05.19

1- Introduction

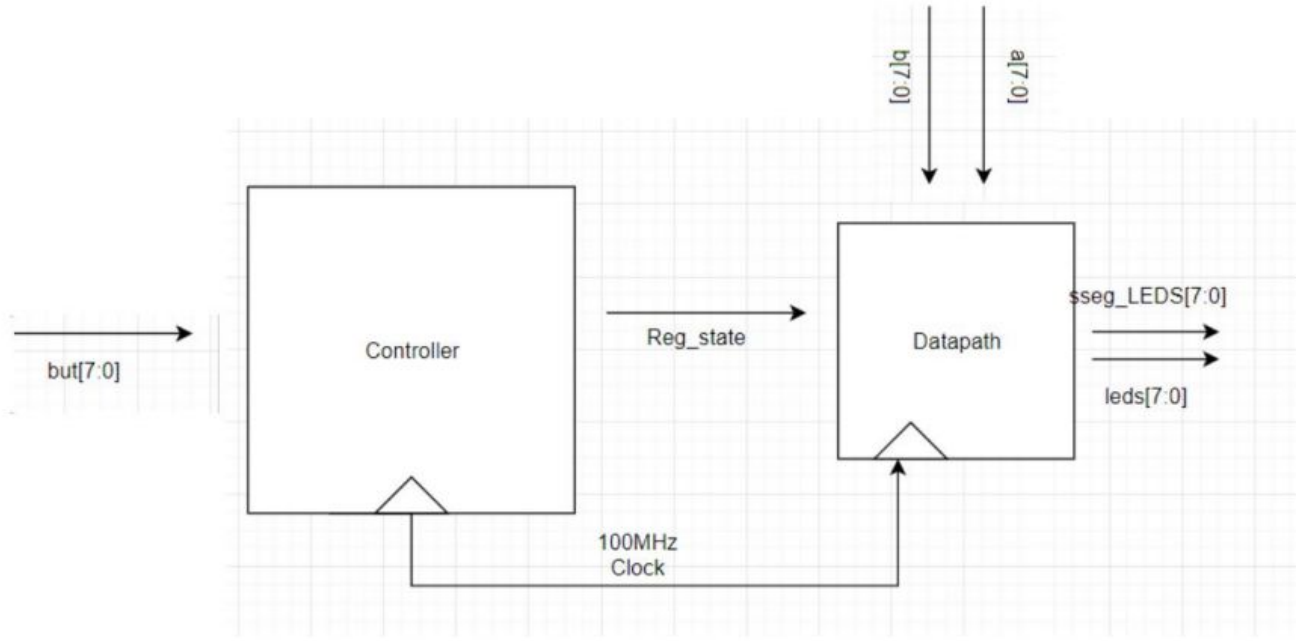
The aim of this project is to build a simple calculator on Basys3 by using SystemVerilog. Calculator consists of mathematical operations which are addition, multiplication, division, and division remainder. It basically takes two 8 bit numbers in 2's complement form from switches and calculates results by corresponding button actions. Also, it is aimed to blink results on the display on for 500ms and off for 1500ms. Since the calculator is an example of interfacing multiple components, it is designed by creating its FSM and HSLM logic.

2 – Diagrams

Simple version of FSM :



Top Logic Diagram:



3 – Design Information

In this project, Basys3 FGPA is used as a controller which includes 5 buttons and control cases with but[7:0] inputs. 16 switches are used as inputs of data path with a[7:0] and b[7:0]. Basys3 LEDs and seven segments display LEDs are also used for the output of the datapath which is sseg_LEDS[7:0].

The working mechanism of the calculator is that it mainly consists of two logic blocks: controller and datapath. It provides users to enter the data as two 8 bit numbers from switches in 2s complement form. Also, in the controller block, the user selects the wanted operation from corresponding buttons which are but[7:0] inputs from Basys3. Buttons and switches hold the values

for input for the main module. For each switch, which are a[7:0] and b[7:0], a led is assigned to its value, which are leds[7:0]. In the project main module consists of a register for the state changes. If the button for reset state is selected it stays in the reset state, initial state. If not, it changes its state for the next-state and this is done by the button selection. In code, this part is done by case and if statements. Thus, there are mainly five states, cases, which are initial, addition, multiplication, division, and modulo. States are changing by flip flop with every clock rising edge. In this project, the clock period is 100 Mhz. After the case is selected the calculations are performed for each state. Since the numbers are in 2's complement form for negative sign numbers, which has 1's in their most significant bit, first a new variable for values a and b are set to them and then added one to the values of the new variables. In project code, anew is for a's complement form and bnew is for the b's complement form. Then each calculation is done with different if statements for their sign operations. For instance, in addition, case first a[7] and b[7] are checked, which are their most significant bits. If they both equal to 1 then the addition is done by anew and bnew. After that, in seven segments the last digit which is sseg_LEDS[7] is set to 7'1111111 which is the default value. Similarly, if a[7] and b[7] both equal to 0 then the addition of a and b made and adjusted for not to show any sign character seven segment display. If a[7] and b[7] are different then calculations are made accordingly.

In seven segments display numbers are shown in the decimal system. For this reason, the conversation is made in each case in the main module. This is made by finding the corresponding digit by several calculations. For instance the least second number is found by (result % 100) - (result % 10) / 10 . In the multiplication part, other calculations are made for numbers that are larger than 4 bits.

Another part of the implementation is that showing the result in seven segment display for 0.5s and not to display for 1.5s. Thus, it has a 2s period for blinking. For this purpose, 100 Mhz system clock is first converted to ms which is equal to 500.000.000ms. Then, it is found that to get this new period a counter should be incremented while the display is 1 till it reaches 50.000.000 after that display is 0. Also, since its period is 500.000.000*4 counter is set to zero at 500.000.000*4. These calculations are made in a different block that works in every clock rising edge. The display is also connected to the sevenSegment module as an input.

4 – Conclusion

To create a simple calculator on the Basys3 with SystemVerilog first FSM diagram is created and then HLSM blocks are made. By observing their logic the main module with register and several combinational logic has been created in SystemVerilog. Also, to display blinking results new CLK value for the seven-segment display has been calculated by using counter logic in the main module. For displaying results on the display another module for seven segment display was created. Numbers are shown in the decimal system on display and corresponding calculations are made in each case for each operation. Consequently, the aim of the project is achieved successfully with all aspects.