

Operating system HW 1

- (1.0g)
  - a) To initiate a DMA transfer, the CDV will set Up the DMA registers first, which contains a pointer byte for transferring, a pointer to the destination transfer & finally a counter of the number of transfers. While the CPU is available to finish another work.
  - b) once the transfers are done, the DMA controller will interupt the CPV
  - c) The CPU & DIYA controllers are bus masters. A problem is formed when both the cPU & DMA masters wants to access the memory at the same time. The cpu will momentarily prevented from accessing main memory when the DMA controller selzes the memory bus accordingly. However, if the CPU is still allowed to access data in its primary & secondary caches, a convency issue may be created if both CPU & DMA controller update the same memory location.
- (2.7)

shared memory a message passing

Strength: shared memory is avick compared to the message passing model if the techniques one on a similar

weakness: various techniques are reavired to confirm which they aren't composing to the similar direction machine. concurrently.

(2.19)

by It is easier to extend the operating system. All new services are added to userspace & consequently do not require

b provides more security & reliability, since the components included can disrupt the functionality of the system

b microterrel architecture is isolated & small so it can function better.

by Its more accessible since it can be added to the system application without disturbing the kernel.

Lo By using interprocess communication mechanisms such as messaging which are conveyed by operating system

## Disadvantage:

b It is expensive compared to monouthic system.

by A context switch or a function call is needed when the drivers are implemented as procedures or processes.

b the performance can be indifferent & may lead to some problems.

long term	Medium - term	Short-term
h job screduler	15 swapping scheduler	6 cpu scheduler
is the speed is slower than short term	b, the speed is in between wag & Shortterm	b the fastest among the three.
5 controls the degree of multiprogramming.	b) reduces the degree of multiprogramming.	L) provides lesser control over the degree of multi programming.
by almost zero or minimal in time	b a part of the time sharing	to minimal time sharing system

is can reintroduce the process into

memory & execution can be

5 selects those processes that

are ready to execute.



sharing system

execution

is selects processes from the pool &

wads them into me mory for

benefit: allows a rendezvous between sender & receives

Disadvantage: rendezvous might not be required & the message could be delivered asynchronously.

As a result, message passing systems of synchronization.

system

continued.

- b) Automatic buffering provides a queue with indefinite length, which ensures the sender will never have to block while waiting to copy a message. There are no specification one how automatic buffering will be provided; are scheme might reserve enough carge memory where most of the momory is waited. Explicit buffering specifies how large the buffer is. In this situation, the sender might be blocked while waiting for available space in the queue. However, it less likely that memory will be wasted with explicit buffering.
- c) send by copy doesn't allow the receiver to alter the state of parameter; send by reference does allow it a berefit of send by reference it that it allows the programmer to write a distributed version of a centralized application. Java RMI provides both; but I passing a parameter by reference requires declaring the parameter as a remote object as well.
- d) The implication of this are mostly related to buffering issues; with fixed-size message, a buffer with a specific size can would a known number of messages, a buffer with a specific size can hold = 9 known number of messages. The number of variable sized messages that can be neld by such a buffer is unknown