ECE528 Project report

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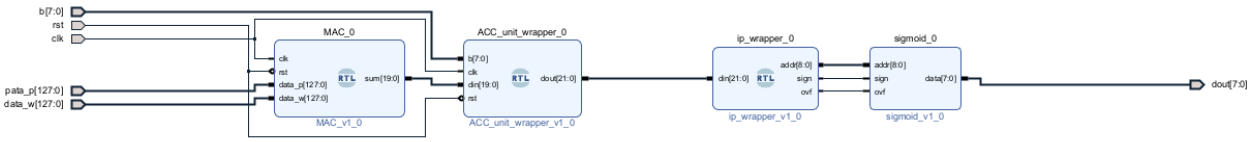
We have completed all three milestones of the project and are explained as follows.

Design

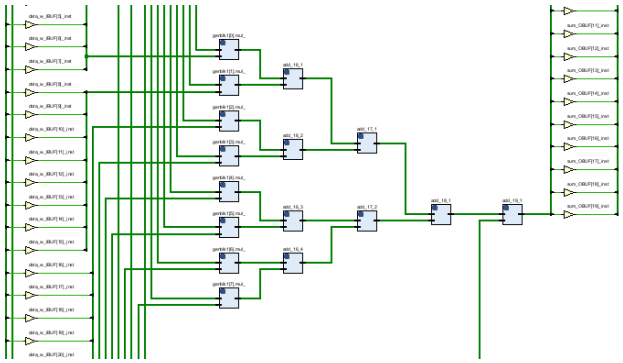
The Design can be divided in to three parts,

- Multiplier and adder unit – MAC
- Accumulator unit – ACC
- Sigmoid activation function unit – SIG



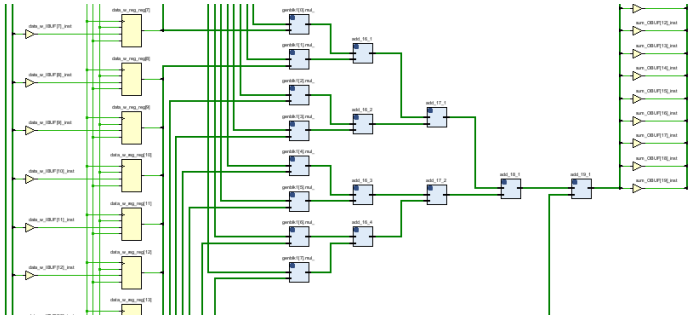
MAC design

This module contains 16, 8bit multipliers and there product is added together by a series of cascaded adders. In order to optimize the throughput of the multiplier adder unit we implemented 3 pipe ling stages within this unit.

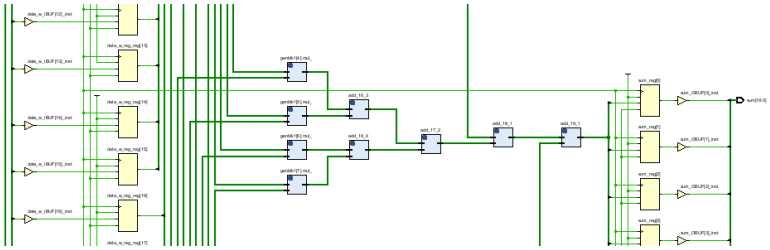


Part of the design without pipe ling

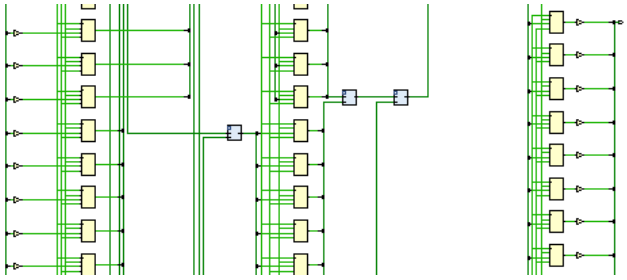
After adding flops to inputs



After adding pipe ling to inputs and outputs

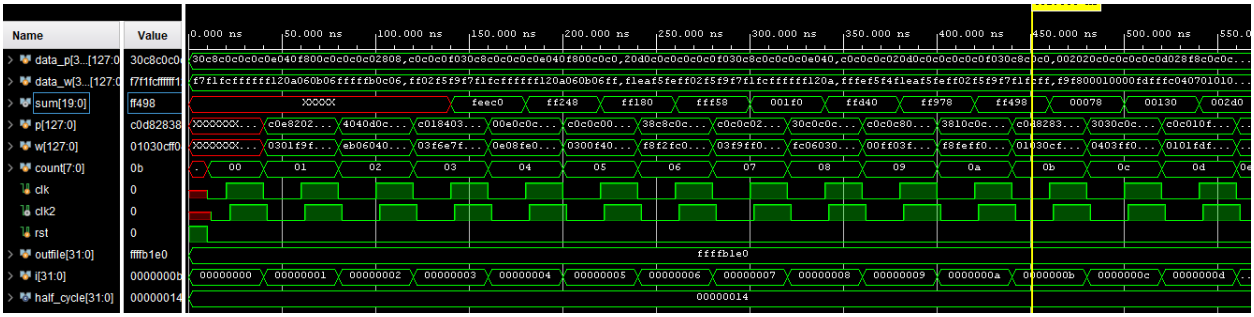


Worst negative slack (@clk 100Mhz) wns = 2.076ns



As the multipliers are responsible for the majority of the combinational delay in the circuit we add a pipeline stage right after the multipliers this further improved the slack of the circuit.
wns – 5.058ns

Simulation behavioral

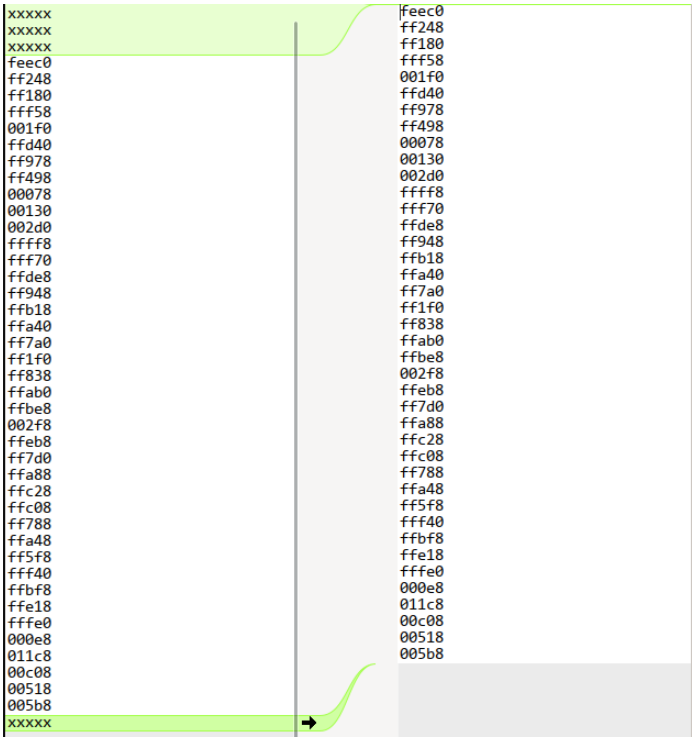


Simulation – post synthesis timing

Simulation output

In order to validate the performance of the MAC unit a simulation was done with the data in “digits_hex.txt” and “weights_hex”.

Due to pipe ling our design takes additional 3 clock cycles to produce the first result, this is the reason for the “xxxxx” in the beginning of the data dumped by the simulation.

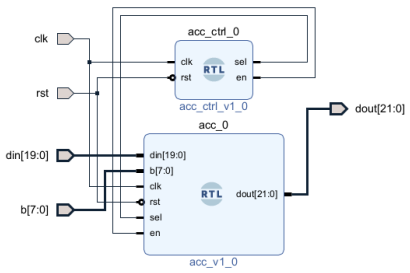


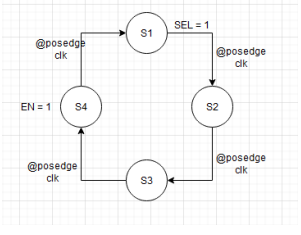
xxxxx	feec0
xxxxx	ff248
xxxxx	ff180
feec0	fff58
ff248	001f0
ff180	ffd40
fff58	ff978
001f0	ff498
ffd40	00078
ff978	00130
ff498	002d0
00078	ffff8
00130	fff70
002d0	ffde8
ffff8	ff948
fff70	ffb18
ffde8	ffa40
ff948	ff7a0
ffb18	ff1f0
ffa40	ff838
ff7a0	ffab0
ff1f0	ffbe8
ff838	002f8
ffab0	ffeb8
ffbe8	ff7d0
002f8	ffa88
ffeb8	ffc28
ff7d0	ffc08
ffa88	ff788
ffc28	ffa48
ffc08	ff5f8
ff788	fff40
ffa48	ffbf8
ff5f8	ffe18
fff40	fffe0
ffbf8	000e8
ffe18	011c8
fffe0	00c08
000e8	00518
011c8	005b8
00c08	
00518	
005b8	
xxxxx	

Data comparison (simulated left/ given right)

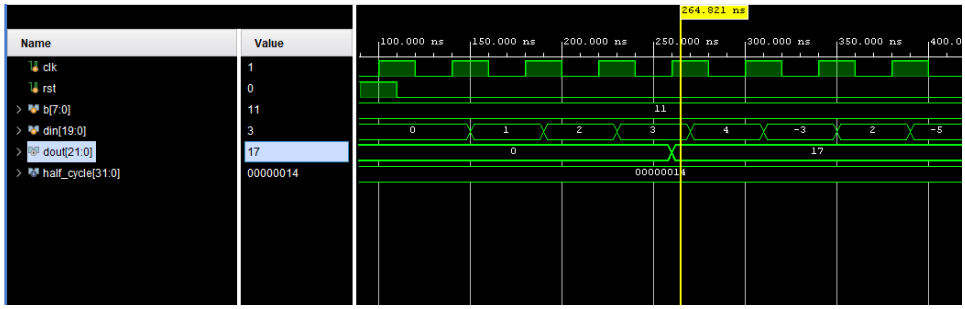
ACC unit

This unit is used to add 4 consecutive values from the MAC unit. This unit needs its own FSM to function and it is implemented in a separate module called acc_ctrl

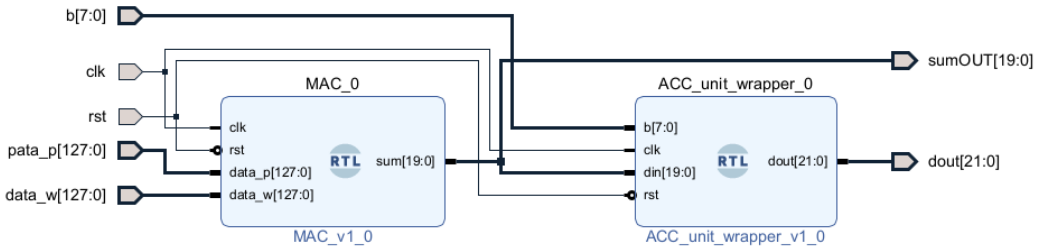




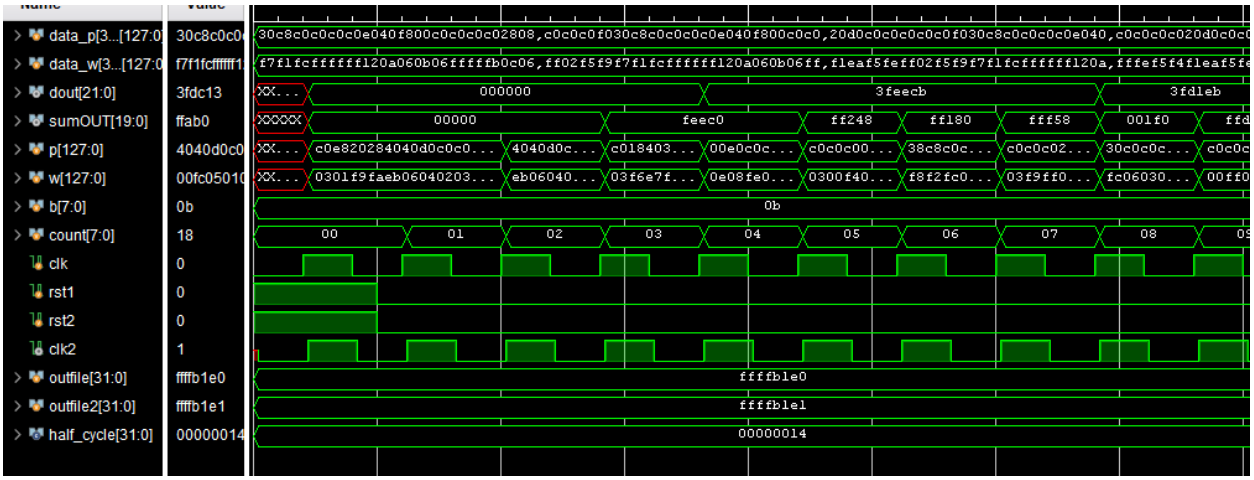
FSM of acc_strl



Then we combined the acc with the previously discussed MAC and ran the simulation.



Simulation waveform



Simulation data

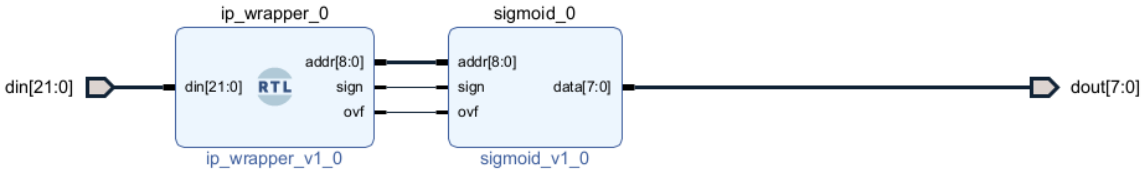
3fd1eb	3fd1eb
3fed4b	3fed4b
00047b	00047b
3ff1c3	3ff1c3
3fdc13	3fdc13
3ff853	3ff853
3fea93	3fea93
3fe713	3fe713
3ffae3	3ffae3
0028ab	0028ab

Dumped data matches exactly with the results files that were given

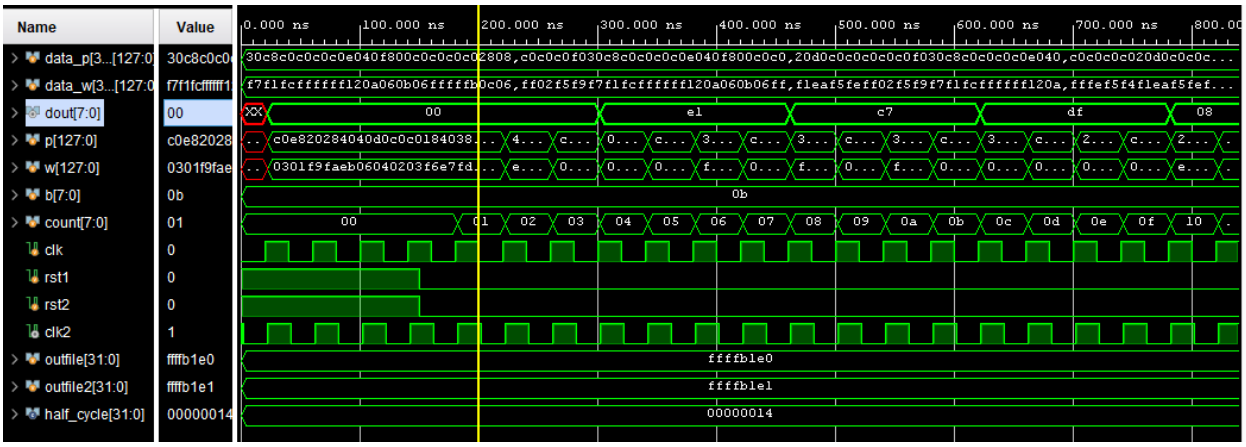
Sigmoid activation unit

This unit was added as an IP to the design, due to vivado version mismatch it did not synthesize, therefore only behavioral simulation was done after integrating with all modules.

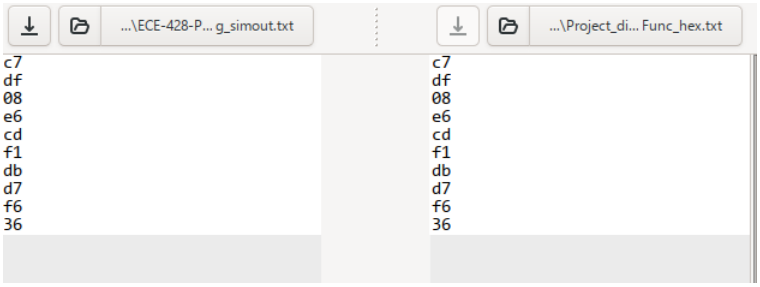
In order to intergrate this a sigmoid ip wrapper was implemented.



Simulation wave form



Simulation data



Design considerations

During the design we tried to find balance between hardware utilization and performance. As we need to reduce the amount of hardware that is used to reduce the cost of mass manufacturing, we used an accumulator to add 4 results from the Multiplier circuitry. The aim of implanting the neural network on hardware was to enhance the performance of it we added pipeline stage to reduce the combinational delay in the MAC resulting higher throughput. The circuit works on 100Mhz which is not very high depending on modern standards resulting lower harmonic distortions to the

environment, which will result less electromagnetic radiation that could cause health issues to the users. Also due to this we managed to reduce the power consumption of the device while easily meeting timing.