ECE528 Project report

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We have completed all three milestones of the project and are explained as follows.

Design

The Design can be divided in to three parts,

* Multiplier and adder unit – MAC
* Accumulator unit – ACC
* Sigmoid activation function unit – SIG

A diagram of a diagram

Description automatically generated

MAC design

This module contains 16, 8bit multipliers and there product is added together by a series of cascaded adders. In order to optimize the throughput of the multiplier adder unit we implemented 3 pipe ling stages within this unit.

A computer diagram of a network

Description automatically generated with medium confidence

Part of the design without pipe ling

After adding flops to inputs

A computer diagram of a computer network

Description automatically generated with medium confidence

After adding pipe ling to inputs and outputs

A diagram of a computer network

Description automatically generated

Worst negative slack (@clk 100Mhz) wns = 2.076ns

A diagram of a computer network

Description automatically generated

As the multipliers are responsible for the majority of the combinational delay in the circuit we add a pipeline stage right after the multipliers this further improved the slack of the circuit.

wns – 5.058ns

Simulation behavioral

A screen shot of a computer

Description automatically generated

Simulation – post synthesis timing

A screenshot of a computer

Description automatically generated

Simulation output

In order to validate the performance of the MAC unit a simulation was done with the data in “digits\_hex.txt” and “weights\_hex”.

Due to pipe ling our design takes additional 3 clock cycles to produce the first result, this is the reason for the “xxxxx” in the beginning of the data dumped by the simulation.

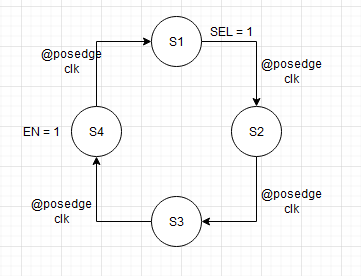
A screenshot of a computer

Description automatically generated

Data comparison (simulated left/ given right)

ACC unit

This unit is used to add 4 consecutive values from the MAC unit. This unit needs its own FSM to function and it is implemented in a separate module called acc\_ctrl

A diagram of a computer program

Description automatically generated

FSM of acc\_strl

A screenshot of a computer

Description automatically generated

A diagram of a computer circuit

Description automatically generatedThen we combined the acc with the previously discussed MAC and ran the simulation.

Simulation waveform

A screenshot of a computer

Description automatically generated

Simulation data

A screenshot of a computer

Description automatically generated

Dumped data matches exactly with the results files that were given

Sigmoid activation unit

This unit was added as an IP to the design, due to vivado version mismatch it did not synthesize, therefore only behavioral simulation was done after integrating with all modules.

In order to intergrate this a sigmoid ip wrapper was implemented.

A close-up of a circuit

Description automatically generated

Simulation wave form

A screenshot of a computer

Description automatically generated

Simulation data

A screenshot of a computer

Description automatically generated

Design considerations

During the design we tried to find balance between hardware utilization and performance. As we need to reduce the amount of hardware that is used to reduce the cost of mass manufacturing, we used an accumulator to add 4 results from the Multiplier circuitry. The aim of implanting the neural network on hardware was to enhance the performance of it we added pipeline stage to reduce the combinational delay in the MAC resulting higher throughput. The circuit works on 100Mhz which is not very high depending on modern standards resulting lower harmonic distortions to the environment, which will result less electromagnetic radiation that could cause health issues to the users. Also due to this we managed to reduce the power consumption of the device while easily meeting timing.