**2. Introduction**

**2.1 Objective**

State the primary goal of the project.  
*Example*:  
"The primary objective is to design a 9-bit SAR ADC with high energy efficiency and low power consumption, suitable for [specific applications]."

**2.2 Background**

Discuss SAR ADC fundamentals, the rationale behind the chosen architecture, and its significance in mixed-signal applications.

**2.3 Design Specifications**

* Resolution: 9 bits
* Sampling Rate: [e.g., 1 MS/s]
* Power Consumption: [Target value, e.g., <1 mW]
* Supply Voltage: [e.g., 1.2 V]
* Process Technology: GPDK 90nm

**3. Methodology**

**3.1 SAR ADC Architecture**

Explain the architecture, including a block diagram of the SAR ADC.

* **Sub-circuits**:
  + Sample-and-Hold Circuit
  + DAC (Digital-to-Analog Converter)
  + Comparator
  + SAR Logic

**3.2 Technology and Tools**

* **Process**: GPDK 90nm CMOS
* **Simulation Tools**: Cadence Virtuoso, Spectre, etc.
* **Design Flow**: Include the design, simulation, layout, and verification steps.

**3.3 Design Trade-offs**

Discuss the trade-offs between speed, power, and resolution.

**4. Circuit Design**

**4.1 CS Capacitor array**

Explain the design of the sample-and-hold stage, with schematics and equations for sizing.

**4.3 Comparator**

Discuss the design of the comparator, its speed, and noise considerations.

**4.4 SAR Logic**

Explain the SAR logic design, including clocking and control signals.

**5. Simulation Results**

**5.1 Pre-layout Simulations**

Provide key results with graphs/plots for:

* ADC transfer characteristics
* Dynamic performance (e.g., INL, DNL)
* Power consumption
* Timing analysis

**5.2 Post-layout Simulations**

Summarize results from post-layout simulations, highlighting parasitics' impact.

**5.3 Performance Metrics**

Present a table comparing your ADC's performance with other similar designs.

| **Metric** | **This Work** | **Reference 1** | **Reference 2** |
| --- | --- | --- | --- |
| Resolution | 9 bits |  |  |
| Sampling Rate |  |  |  |
| Power |  |  |  |

**6. Layout**

**6.1 Layout Overview**

Include the layout image with annotations.

**6.2 Design Rule Check (DRC) and Layout vs. Schematic (LVS)**

Discuss DRC and LVS results and how any issues were resolved.

**7. Conclusion**

Summarize the achievements, challenges, and potential improvements for future work.