National University of Sciences and Technology (NUST)
School of Electrical Engineering and Computer Science

Department of Electrical Engineering

Faculty Member: Engr. Arshad Nazir **Dated:** 26th October 2023

Semester: 3rd **Section:** D

Group No.: 10

EE-241: Digital Logic Design

Lab 07: Design a display system of a rolling dice.

		PLO4/CLO4	PLO4/CLO4	PLO5/CLO5	PLO8/CLO6	PLO9/CLO7	
Name	**Reg. No**	**Viva / Lab Performance** **5 Marks**	**Analysis of data in Lab Report** **5 Marks**	**Modern Tool Usage** **5 Marks**	**Ethics and Safety** **5 Marks**	**Individual and Teamwork** **5 Marks**	**Total marks Obtained** **25 Marks**
Ahmad Nasir	409959						
Arooj Fatima	423365						
Haseeb Umer	427442						
Irfa Farooq	412564						

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Lab7: Design a system that display from 1 to 6. It displays the result on a dice. The dice has seven lights.

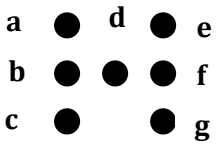
This Lab Activity has been designed to practice the use of basic gates for designing a system.

- Simplification of Combinational Circuits
- Design and Implementation of a design a system to display dice values.
- Values-Segment Decoder for Selected Digit Display
- There are related questions at the end of this activity. Give complete answers.

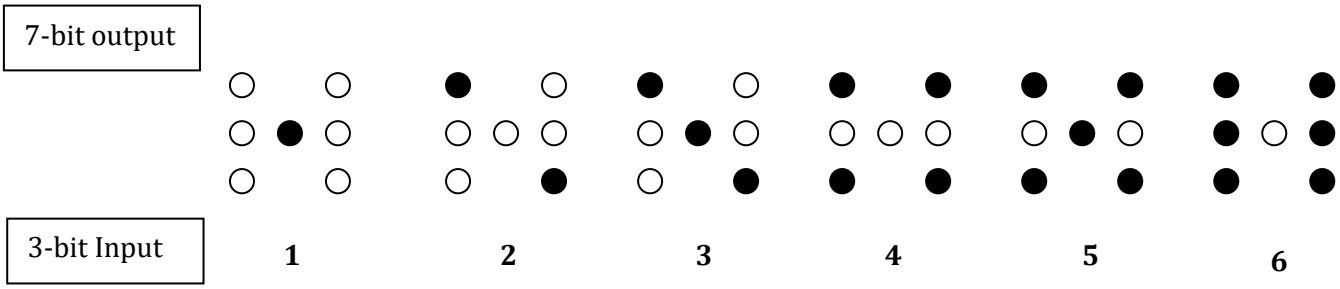
Use diagrams if needed for clarity.

Prelab Task (5 marks – Individual and teamwork)

Design a system that display from 1 to 6 (ONLY)i.e., it shows no output in case of illegal input like 0 and 7. It displays the result on dice. The dice has seven LEDs a,b,c,d,e,f,g, placed in H shape pattern as shown on the diagram below.



A 1 for each segment (a, b, c, d, e, f, g) indicates that it is lit (on); and a 0 that it is off. The arrangement is the six numbers on a dice are shown below; where the darkened circles depicts LED is ON. (**Make sure to switch off all the lights in Don't care case**)



- Design a driver that produces the seven LED (a, b, c, d, e, f, g) to drive the display.

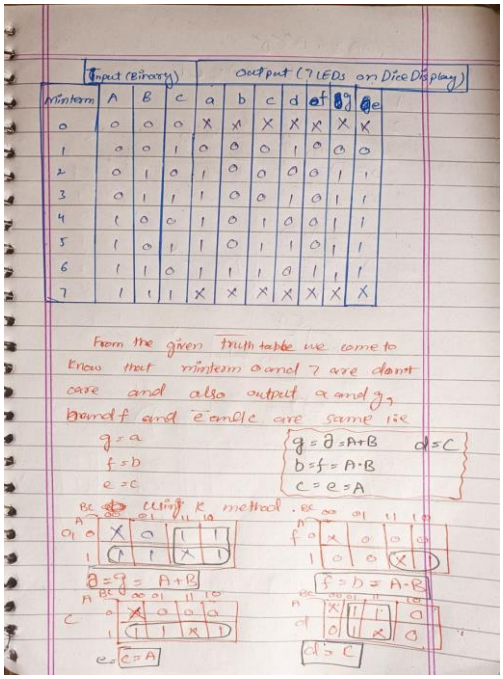
1. Complete the following table. (**Make sure to switch off all the lights in Don't care case**)
   (First 3 inputs are filled for guidance)

Truth Table:

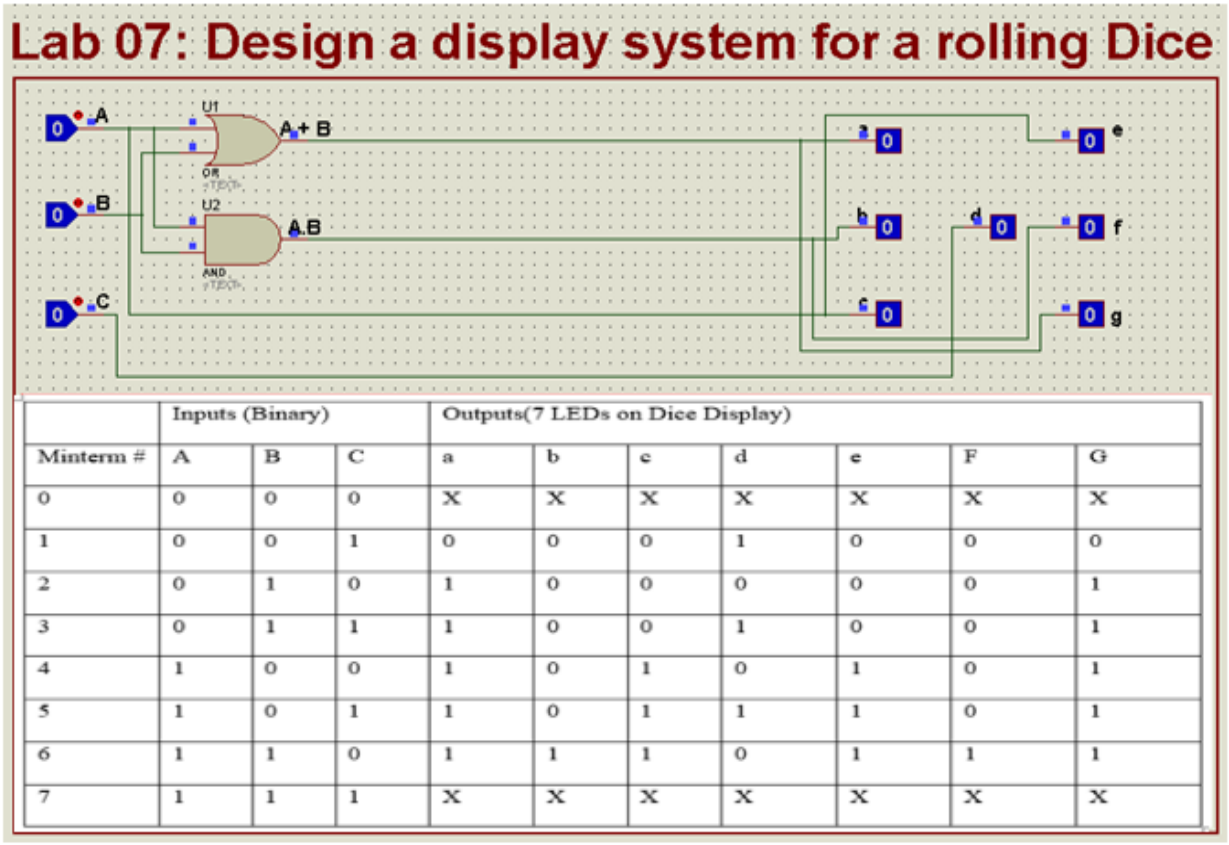
	Inputs (Binary)			Outputs(7 LEDs on Dice Display)						
Minterm #	A	B	C	a	b	c	d	e	F	g
0	0	0	0	X	X	X	X	X	X	X
1	0	0	1	0	0	0	1	0	0	0
2	0	1	0	1	0	0	0	0	0	1
3	0	1	1	1	0	0	1	0	0	1
4	1	0	0	1	0	1	0	1	0	1
5	1	0	1	1	0	1	1	1	0	1
6	1	1	0	1	1	1	0	1	1	1
7	1	1	1	X	X	X	X	X	X	X

- Write minimum possible functions to realize outputs (Either using k-mapping/ or minimization of Boolean function) (**Make sure to switch off all the lights in Don't care case**). Show and get verified the minimized Boolean Function expressions to Lab Engineer before implementation. Hint: You will get 7 output expressions. Output expression for 'a' and 'g' will be same. Output expression for 'b', and 'f' will be same. Output expression for 'c' , and 'e' will be same.

- **a=g=A+B**
- **b=f=A.B**
- **c=e=A**
- **d=C**



- Draw the complete logic circuit diagram of the system from simplified equations.



	Inputs (Binary)			Outputs(7 LEDs on Dice Display)						
Minterm #	A	B	C	a	b	c	d	e	F	G
0	0	0	0	X	X	X	X	X	X	X
1	0	0	1	0	0	0	1	0	0	0
2	0	1	0	1	0	0	0	0	0	1
3	0	1	1	1	0	0	1	0	0	1
4	1	0	0	1	0	1	0	1	0	1
5	1	0	1	1	0	1	1	1	0	1
6	1	1	0	1	1	1	0	1	1	1
7	1	1	1	X	X	X	X	X	X	X

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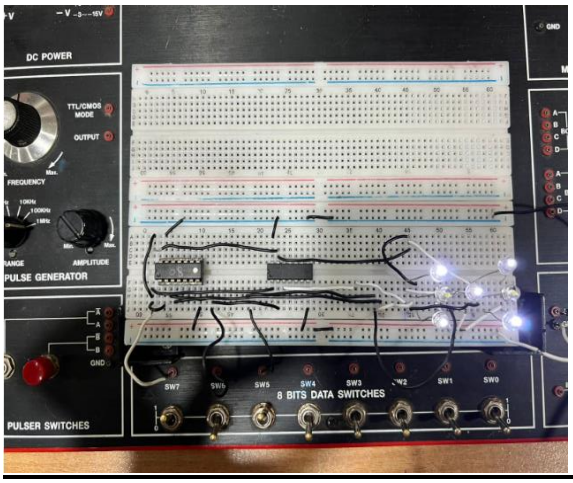
Lab Task 1 (5 marks – Analysis of Lab report)

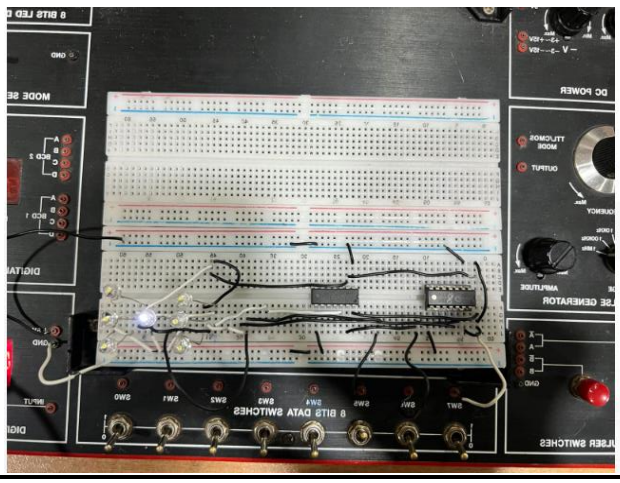
- Implement the designed logic circuit on hardware. Utilize your creativity to make the Dice display **model.**

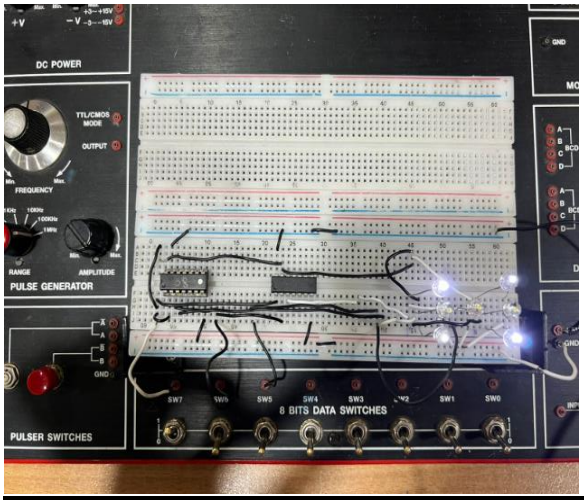
Truth table:

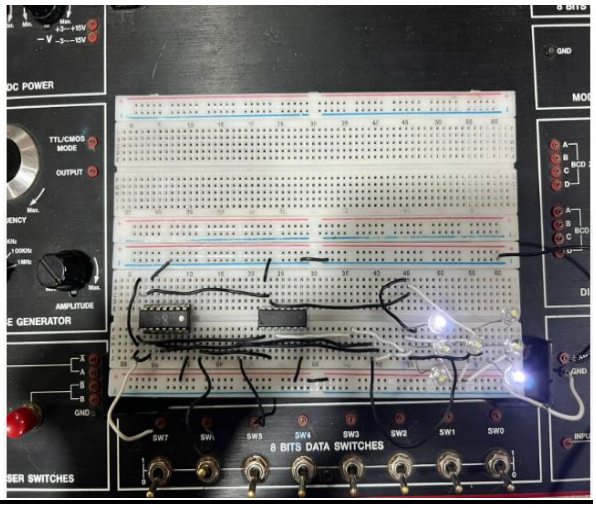
	Inputs (Binary)			Outputs(7 LEDs on Dice Display)						
Minterm #	A	B	C	a	B	c	d	E	F	G
0	0	0	0	X	X	X	X	X	X	X
1	0	0	1	0	0	0	1	0	0	0
2	0	1	0	1	0	0	0	0	0	1
3	0	1	1	1	0	0	1	0	0	1
4	1	0	0	1	0	1	0	1	0	1
5	1	0	1	1	0	1	1	1	0	1
6	1	1	0	1	1	1	0	1	1	1
7	1	1	1	X	X	X	X	X	X	X

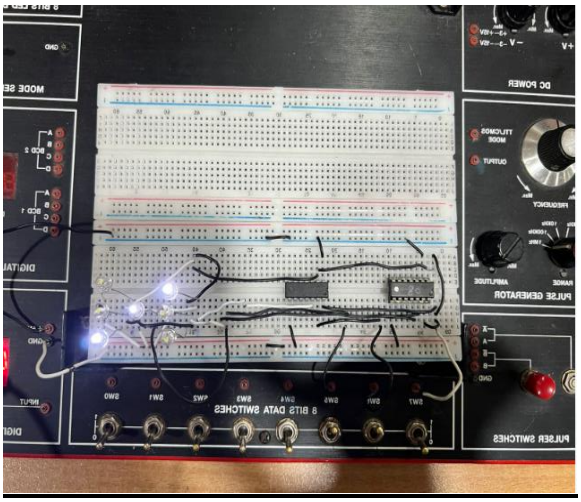
Hardware Screenshots:











Lab Task 2 (5 marks – Modern tool usage)

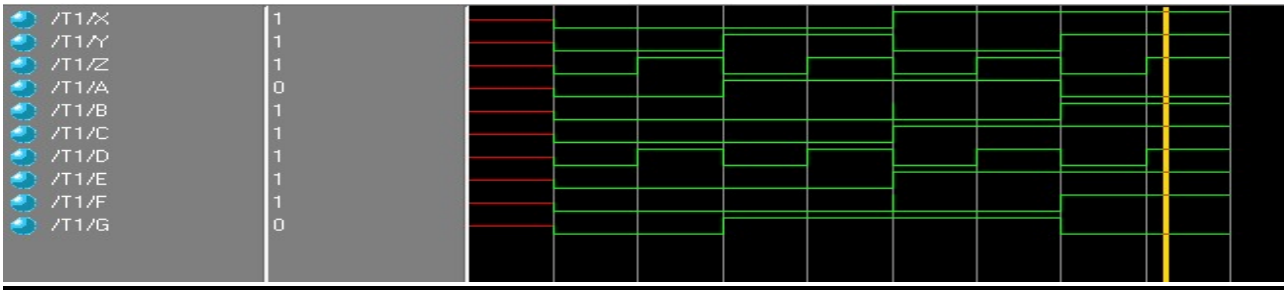
- Write Verilog code to realize the design using dataflow model. Design also test bench to check the valid outputs. Include all the timing diagram snap shots and Verilog code in the report.

Verilog Code:

```
module Lab_07(a, b, c, d, e, f, g, x, y, z);
output a, b, c, d, e, f, g;
input x, y, z;
assign a = x + y;
assign b = x & y;
assign c = x;
assign d = z;
assign e = x;
assign f = x & y;
assign g = x + y;
endmodule

module T1;
reg X, Y, Z;
wire A, B, C, D, E, F, G;
Lab_07 T1(A, B, C, D, E, F, G, X, Y, Z);
initial
begin
        #100 X=1'b0; Y=1'b0; Z=1'b0;
        #100 X=1'b0; Y=1'b0; Z=1'b1;
        #100 X=1'b0; Y=1'b1; Z=1'b0;
        #100 X=1'b0; Y=1'b1; Z=1'b1;
        #100 X=1'b1; Y=1'b0; Z=1'b0;
        #100 X=1'b1; Y=1'b0; Z=1'b1;
        #100 X=1'b1; Y=1'b1; Z=1'b0;
        #100 X=1'b1; Y=1'b1; Z=1'b1;
end
endmodule
```

Output Waveform:



Conclusion:

In this Digital Logic Design (DLD) lab, we were tasked with designing a system that simulates the functionality of a 6-sided dice display. The system is composed of seven lights that represent the numbers 1 to 6. This lab allowed us to design a system that effectively mimics a 6-sided dice using a dataflow model in Verilog. By creating a comprehensive test bench and conducting various tests, we verified that our design correctly displays the numbers 1 to 6, demonstrating its suitability for its intended purpose.