National University of Sciences and Technology (NUST)
School of Electrical Engineering and Computer Science

Department of Electrical Engineering

Faculty Member: Sir Arshad Nazir **Dated: 14th September 2023**

Semester: 3rd **Section: D**

Group No.: 22

EE-221: Digital Logic Design

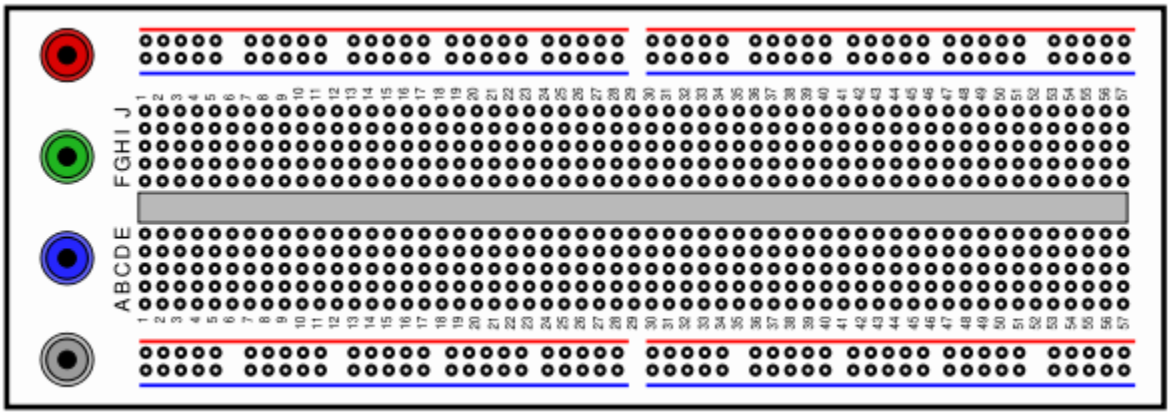
Lab 1: FAM of Basic gates and ICs

		PLO4/CLO4	PLO4/CLO4	PLO5/CLO5	PLO8/CLO6	PLO9/CLO7	
Name	**Reg. No**	**Viva / Lab Performance** 5 Marks	**Analysis of data in Lab Report** 5 Marks	**Modern Tool Usage** 5 Marks	**Ethics and Safety** 5 Marks	**Individual and Team Work** 5 Marks	**Total marks Obtained** 25 Marks
Ahmed Nasir	**409959**						
Haseeb Umer	**427442**						
Arooj Fatima	**423365**						
Irfa Farooq	**412564**						

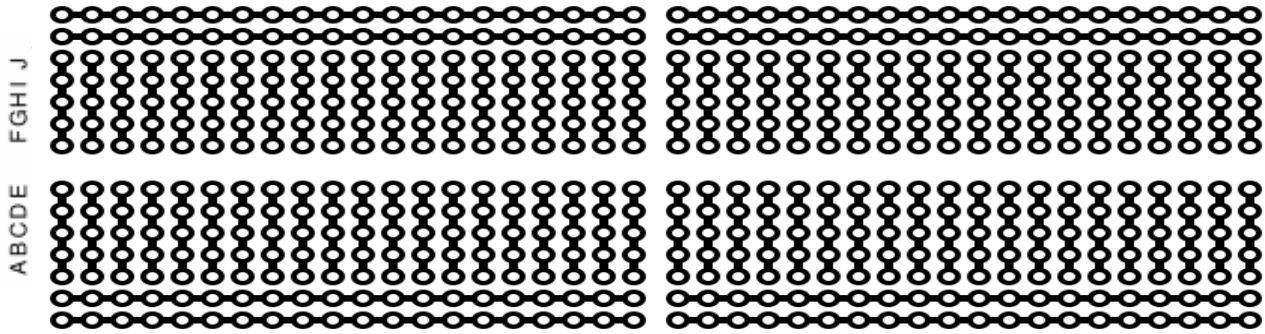
Getting Started with Circuit Patching

Breadboard:

Breadboards are usually used for patching small circuits and prototypes. A typical breadboard would look like this.

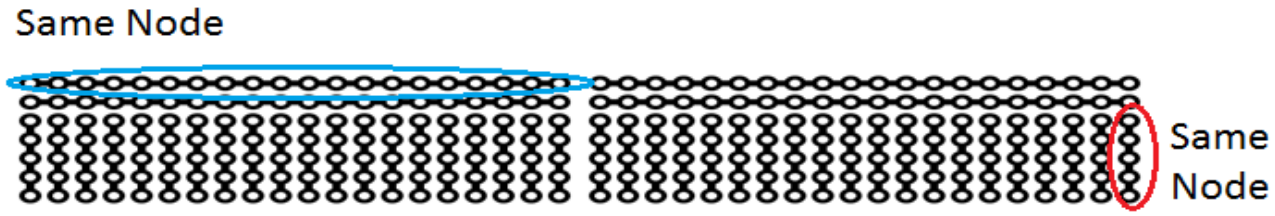


The internal connections are as shown below:



The points in ABCDE (and FGHIJ) grid are vertically connected as indicated by red circle. So, all 5 points on are actually the same point. It makes No difference whether you connect a wire on any one of these points. The next vertical strip is a different point and so on.

It should be noted that upper and lower grids are horizontally connected indicated below. Each grid consists of 4

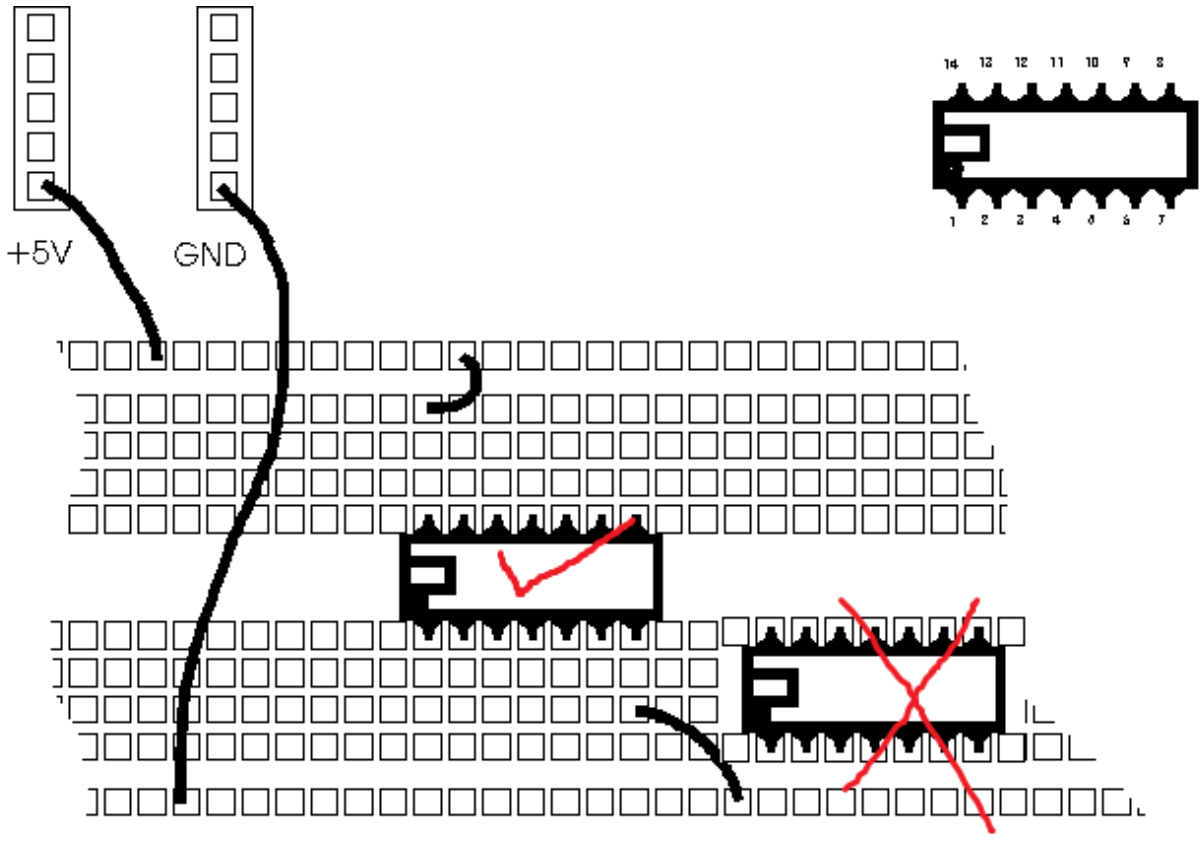


such separate horizontal strips:

IC Placement on Breadboard

A typical 14 pin IC placement on such a bread board is shown below:

The upper and lower horizontal strips are normally served for power (+5V) and ground (0V) respectively. But it is not necessary to do so.



Never place any IC such that its opposite pins are within (connected to) the same Node on the same grid.

Procedure:

1. Make sure the trainer board is switched off while you are patching the circuit.
2. Make a neat schematic diagram clearly mentioning the IC numbers, PIN configurations and connections between different ICs.
3. Place the IC(s) such that the Notch is towards the left.
4. Provide the ground connection(s) by connecting the GND pin(s) of the IC(s) to 0 V on your trainer board power supply with the help of jumping wires. Make sure that all the ICs are properly grounded.
5. Provide the VDD or operating voltage to each IC by connecting its VDD (or VCC) terminal to +5V on your trainer board power supply.
6. Patch the circuit as per the schematic.
7. Connect the inputs of your circuit to the logic switches provided on your trainer board. Typically, there are 8 such switches provided. The low position of the switch indicates a 0-logic level (0V) and the high position a logic level of 1(+5V).
8. Connect the output of your circuit to the logic probe provided on the trainer board.
9. Now switch on the trainer board and give the input sequence to your circuit with the help of logic switches. It is a good practice to give the input sequence in ascending order like this:
   000, 001, 010, 011, 100, 101, 110, 111 (Here No. of inputs is 3). This pattern can be adopted for lesser or more No. of inputs.
10. Observe the output of your circuit against different inputs and record them in the truth table.
11. Compare with theoretical values and debug the circuit if needed.
12. Show your work for each lab task to your Lab Instructor.
13. Give your observations and conclusion.

Lab1: Familiarization of Basic Gates and Digital ICs

This Lab Activity has been designed to familiarize the beginning students with logic gates and IC chips, using breadboard and testing of gates and logic circuits.

Objectives:

- ✓ Familiarize the students with ICs, their categories, and different logic families.
  Identify ICs on the basis of series number as well as their functional behavior and pin numbers.
- ✓ Search data sheets of ICs from different sources and optimally use them in the design of digital circuits.
- ✓ Perform functional verification of basic logic gates by listing the truth tables and establishing IN/OUT relationship.
- ✓ Carry out best wiring practices in digital design.

Lab Instructions:

- ✓ This lab activity comprises three parts, namely Pre-lab, Lab tasks, and Post-lab viva session.
- ✓ The lab report will be uploaded on LMS three days before the scheduled lab date. The students will get a hard copy of lab report, complete the Pre-lab task before coming to the lab and deposit it with teacher/lab engineer for subsequent evaluation. Alternately each group to upload completed lab report on LMS for grading.
- ✓ The students failing to complete Pre-lab will not be allowed to attend lab session.
- ✓ The students will start lab tasks and demonstrate design steps separately for step-wise evaluation (teacher/lab engineer will sign each step after ascertaining functional verification). Any report submitted without teacher/lab engineer signatures will not be accepted.
- ✓ Remember that a neat logic diagram with pins numbered and nicely patched circuit will simplify troubleshooting/fault diagnostic process.
- ✓ After completion of lab, the students are expected to unwire the circuit and deposit back components to lab staff.
- ✓ The students will complete lab task within the prescribed time and submit complete report to the lab engineer before leaving the lab.
- ✓ There will be a viva session after demonstration for which students will be graded individually.

Pre-Lab Tasks: **(5 marks)**

1. Read the topic Integrated Circuits (2.9) from your course book and answer the following questions:

Digital ICs can be categorized according to the complexity of their circuits usually termed as *scale integration*. The following are the six major categories. Give their full names and range of gates available in each of them.

Complexity	Gates per Chip
SSI (Small Scale Integration)	Fewer than 12
MSI (Medium Scale Integration)	12 to 99
LSI (Large Scale Integration)	100 to 9999
VLSI (Very Large Scale Integration)	10,000 to 99,999
ULSI (Ultra Large Scale Integration)	100,000 to 999,999
GSI (Giga Scale Integration)	1,000,000 or more

2. Another categorization is with respect to the Logic Families of Digital ICs. The seven of these are listed below. Give their full name and give their utilization in terms of speed, power etc. (e.g., Low Power, High Speed).

RTL (Resistor-Transistor Logic):

RTL stands for Resistor-Transistor Logic. RTL is an early digital logic family that uses resistors as passive components and transistors as active components. It was popular in the 1960s but has largely been replaced by more advanced families.

Speed: Slow compared to modern technologies.

Power: Consumes more power compared to newer families.

Applications: Historically used in early digital computers.

DTL (Diode-Transistor Logic):

DTL stands for Diode-Transistor Logic. It uses diodes for AND logic and transistors for OR logic. It was popular in the 1960s but has been largely replaced by more efficient families.

Speed: Faster than RTL but slower than newer families.

Power: Consumes moderate power.

Applications: Used in early computing and control systems.

ECL (Emitter-Coupled Logic):

ECL stands for Emitter-Coupled Logic. It is a high-speed logic family known for its speed and precision. It uses transistors in a differential amplifier configuration for high-speed switching.

Speed: Very high-speed operation.

Power: Consumes more power than other families but is known for its high speed.

Applications: Common in high-speed applications like high-frequency communications and high-speed computing.

TTL (Transistor-Transistor Logic):

TTL stands for Transistor-Transistor Logic. It uses transistors for both logic operations and as amplifiers. It was one of the most widely used logic families and played a significant role in the development of digital electronics.

Speed: Moderate to high speed, depending on the sub-family.

Power: Consumes moderate power.

Applications: Common in early computing, microprocessors, and general digital electronics.

CMOS (Complementary Metal-Oxide-Semiconductor):

CMOS stands for Complementary Metal-Oxide-Semiconductor. It uses complementary pairs of MOS transistors for low power consumption and high noise margins. It's the most widely used logic family today.

Speed: Moderate speed but can be very low power.

Power: Very low power consumption when not switching states.

Applications: Widely used in modern integrated circuits including microprocessors, memory, and various digital and analog applications.

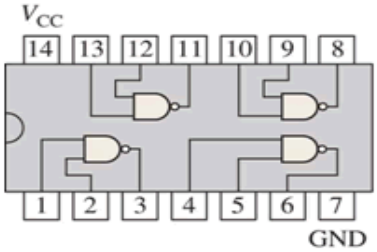
3. Differentiate b/w Fan in and Fan Out of an IC.

Answer: Fan-in corresponds to the number of inputs available in a gate whereas fan-out specifies the number of standard loads that the output of a typical gate can drive without impairing its normal operation. These standard loads are actually the amount of current needed by the input of another similar gate in the same family.

Fan-in	Fan-out
Fan-in refers to the maximum number of inputs that a gate or circuit can handle and still operate correctly. It indicates how many inputs can be connected to a gate without causing signal degradation or malfunction.	Fan-out refers to the maximum number of standard load inputs a gate's output can drive without degrading its performance. It represents the number of gates that can be connected to the output of a gate without causing a significant voltage drop or signal distortion. .
For example, a gate with a fan-in of 2 means it can effectively process signals from 2 input sources.	A gate with a high fan-out can drive more gates, meaning it has a stronger output

In summary, fan-in is about how many inputs a gate can handle, while fan-out is about how many gates a gate's output can drive. These characteristics are important for designing reliable and efficient digital circuits.

IC Pin Numbers:



TOP VIEW

Most of the ICs have a Notch (or sometimes a dot) to denote the start of the PIN numbering. Place the IC such that the Notch is on left side, then the lower left PIN is numbered 1, and the numbering continues in the anticlockwise direction.

Datasheet:

Information about any IC (its number of pins and gates inside it) can be found by simply searching by its name on internet. The document containing information about the IC is called its **datasheet**. Different manufacturers of these chips have this information on their sites.

4. Show the correct pin numbering and connection of gates inside these blank chips with the help of their datasheets.

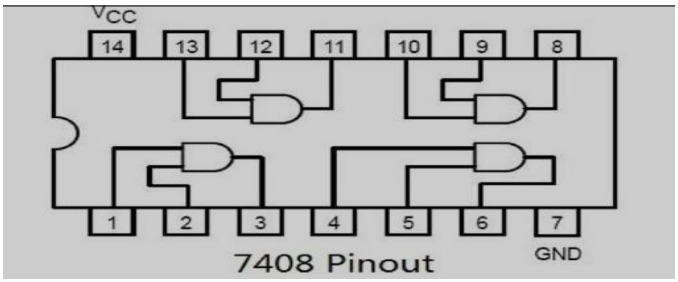


Figure1: Datasheet of AND Gate

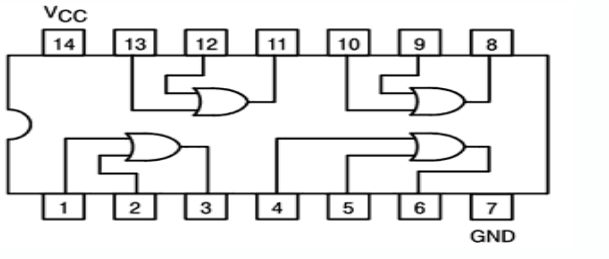


Figure 2: datasheet of OR Gate.

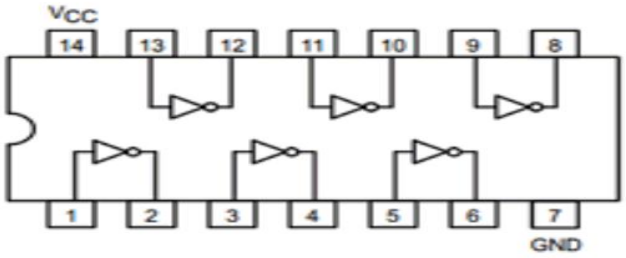


Figure3: Datasheet of NOT Gate

5. Mention the manufacturer whose datasheet you consulted.

Answer: Texas Instruments

Lab Task (5 Marks)

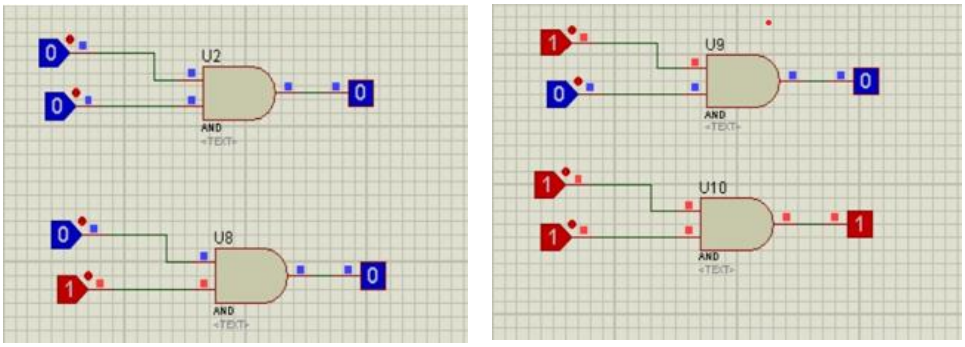
Verify the functioning of the following ICs:

7408

AND Truth Table

Sr. no.	Input A	Input B	Output (A.B)
1	0	0	0
2	0	1	0
3	1	0	0
4	1	1	1

Proteus Simulation



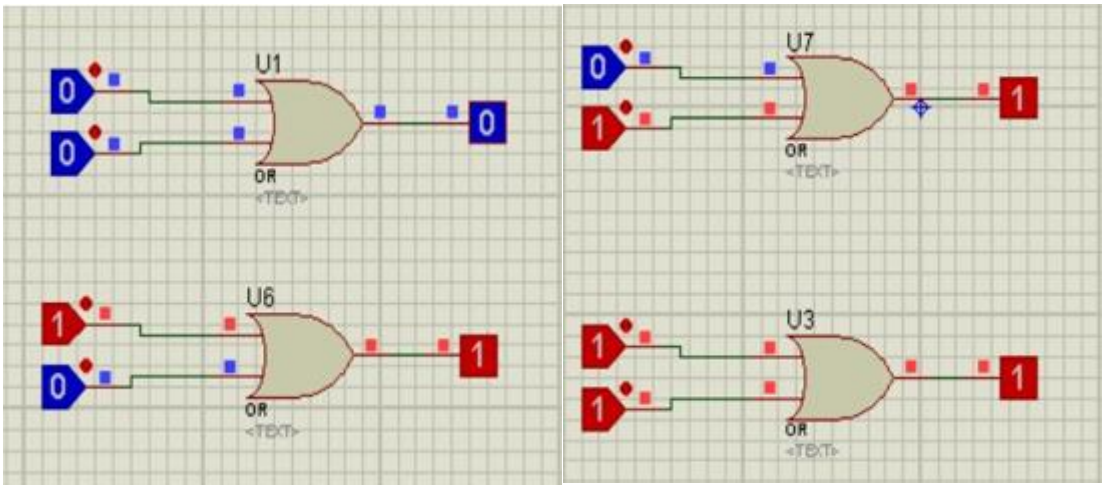
Hardware Output

7432

OR Truth Table

Sr. no.	Input A	Input B	Output (A + B)
1	0	0	0
2	0	1	1
3	1	0	1
4	1	1	1

Proteus Simulation



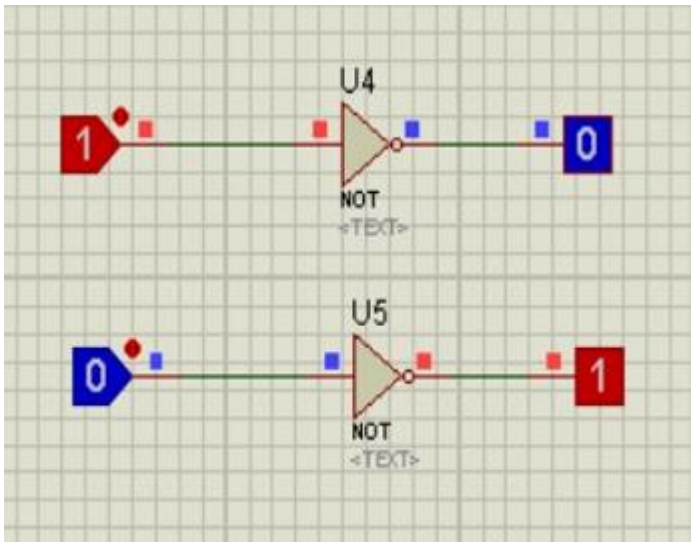
Hardware Output

7404

NOT Truth Table

Sr. no.	Input A	Output A'
1	0	1
2	1	0

Proteus Simulation



Hardware Output

Procedure

1. Make a **schematic layout diagram** in the space provided below, showing ICs pin numbers and their connections to form the logic circuit.
2. Plug in all ICs in bread board and power the ICs providing ground and VCC=5V to appropriate pins. The ground pin is to be connected first and then any other connections are made.
3. By looking at pin configuration apply input signals from a switch on logic lab. Connect the output to LED for display. The operation of circuit is verified and results to be shown to teacher or Lab Asst. For trouble shooting of circuit use the logic probe provided in the lab.
4. Make the truth tables in the space provided below:
5. Mention the full name of each IC provided to you with the help of its datasheet and explain the naming convention (You should be able to get this information from the internet).

Example: *Quad 2-Input AND Gates* *SN74 LS08P*
SN Standard Prefix of TEXAS INSTRUMENT
Quad refers to 4 AND gates
74 refers to commercial grade IC
LS means Low Power *Schottky*
P *Plastic Dual in-Line Package*
08 *refers to AND gate*

AND Gate SN74HC08N

SN Standard Prefix of TEXAS INSTRUMENT
74 refers to commercial grade IC
HC High-Speed Complementary Metal-Oxide-Semiconductor
08 *refers to AND gate*

N the package type or package designator

OR Gate SN74LS32N

SN Standard Prefix of TEXAS INSTRUMENT
74 refers to commercial grade IC
LS means Low Power *Schottky*
32 refers to OR Gate IC
N the package type or package designator

NOT Gate SN74LS04N

SN Standard Prefix of TEXAS INSTRUMENT
74 refers to commercial grade IC
LS means Low Power *Schottky*
04 refers to NOT Gate IC
N the package type or package designator

Fill in the blanks.

1. *The ICs in 7400 series are based on **TTL (transistor-transistor logic)** logic family.*
2. *The commercial grade IC is denoted by **74** prefix.*
3. *The military grade IC is denoted by **54** prefix.*

Observations/Comments:

This was our first DLD lab, so we did not know much about ICS etc. We observe that red light meant 1 and green light meant 0.

In addition, we learned;

- ICS are sensitive, and we should be careful with them.
- Inner circuit designs of ICS.
- A few tips e.g., always use ICS sideways, it helps with connecting wire.
- The AND gate outputs a high signal only when both of its inputs are high.
- The OR gate outputs a high signal when at least one of its inputs is high.
- The NOT gate, on the other hand, inverts the input signal.

In conclusion, it's likely that you gained hands-on experience with these basic logic gates and observed their behavior in different scenarios. This practical knowledge can be fundamental in understanding and designing more complex digital circuits. Additionally, we looked at their internal circuitry, complexity, and their respective pin sequences from the manufacturer datasheet. This was followed by verifying their truth table by simulation in PROTEUS software. Lastly, hardware simulation was used to verify our PROTEUS simulation and truth table by making use of the digital training system.