National University of Sciences and Technology (NUST)
School of Electrical Engineering and Computer Science

Department of Electrical Engineering

Faculty Member: Sir Arshad Nazir **Dated: 16th November 2023**

Semester: 3rd **Section: D**

Group No.: 10

EE-221: Digital Logic Design

Lab 09: Excess-3 to Gray Code Conversion using Nand Gates (Open Ended Lab)

		PLO4/CLO4	PLO4/CLO4	PLO5/CLO5	PLO8/CLO6	PLO9/CLO7	
Name	**Reg. No**	**Viva / Lab Performance**	**Analysis of data in Lab Report**	**Modern Tool Usage**	**Ethics and Safety**	**Individual and Team Work**	**Total marks Obtained**
		5 Marks	**5 Marks**	**5 Marks**	**5 Marks**	**5 Marks**	**25 Marks**
Arooj Fatima	423365						
Ahmad Nasir	409959						
Haseeb Umer	427442						
Irfa Farooq	412564						

Lab 09: Excess-3 to Gray Code Conversion using Nand Gates

This Open-ended Lab has been divided into two parts:

In first part you are required to **design** and **implement** an Excess-3 to gray code converter.

The next part is the Verilog Modeling and **Simulation** of the Circuit you implemented in you first part.

Objectives:

- ✓ Understand steps involved in design of combinational circuits.
- ✓ Understand binary codes for decimals and their hardware realization.
- ✓ Write code for combinational circuits using Verilog Gate Level Modeling
- ✓ Design a circuit in Verilog by calling different modules.

Lab Instructions

- ✓ This lab activity comprises three parts, namely Pre-lab, Lab tasks, and post-Lab Viva session.
- ✓ The lab report will be uploaded on LMS three days before the scheduled lab date. The students will get a hard copy of lab report, complete the Pre-lab task before coming to the lab and deposit it with teacher/lab engineer for necessary evaluation.
- ✓ The students will start lab tasks and demonstrate design steps separately for step-wise evaluation(course instructor/lab engineer will sign each step after ascertaining functional verification).
- ✓ Remember that a neat logic diagram with pins numbered coupled with nicely patched circuit will simplify trouble-shooting process.
- ✓ After the lab, students are expected to unwire the circuit and deposit back components before leaving.
- ✓ The students will complete lab task and submit complete report to Lab Engineer before leaving lab.
- ✓ There are related questions at the end of this activity. Give complete answers.

Pre-Lab Tasks: (To be done before coming to the lab)

1. In the lab you would be implementing an Excess-3 to gray code converter. Make a truth table for both the codes by filling in the following tables and simplify the expressions for W,X,Y,Z in terms of A,B,C,D.(Use backside of the page if necessary). Use unused combinations as don't care conditions. Hint, u can take help from http://engineeringproblemsandanswers.blogspot.com/2015/03/logic-circuits-1-digit-decimal-in-excess-3-to-gray-code-converter.html

(2Marks- **Individual. and Teamwork**)

Dec	Excess 3 code				Gray Code			
	A	B	C	D	W	X	Y	Z
	0	0	0	0	x	x	x	x
	0	0	0	1	x	x	x	x
	0	0	1	0	x	x	x	x
0	0	0	1	1	0	0	0	0
1	0	1	0	0	0	0	0	1
2	0	1	0	1	0	0	1	1
3	0	1	1	0	0	0	1	0
4	0	1	1	1	0	1	1	0
5	1	0	0	0	0	1	1	1
6	1	0	0	1	0	1	0	1
7	1	0	1	0	0	1	0	0
8	1	0	1	1	1	1	0	0
9	1	1	0	0	1	1	0	1
	1	1	0	1	x	x	x	x
	1	1	1	0	x	x	x	x
	1	1	1	1	x	x	x	x

HINT:

Our inputs and outputs are of 4-bit decimal values. You will have to make 4 K-Maps (Consider W as independent function of input variables A,B,C,D, Make K-Map and simplify it). Arrive at the simplest expression for each output. Show your k-mapping and equation simplification in your lab report. Don't copy and paste from this link, other-wise you will get zero.

W = A (B + CD)

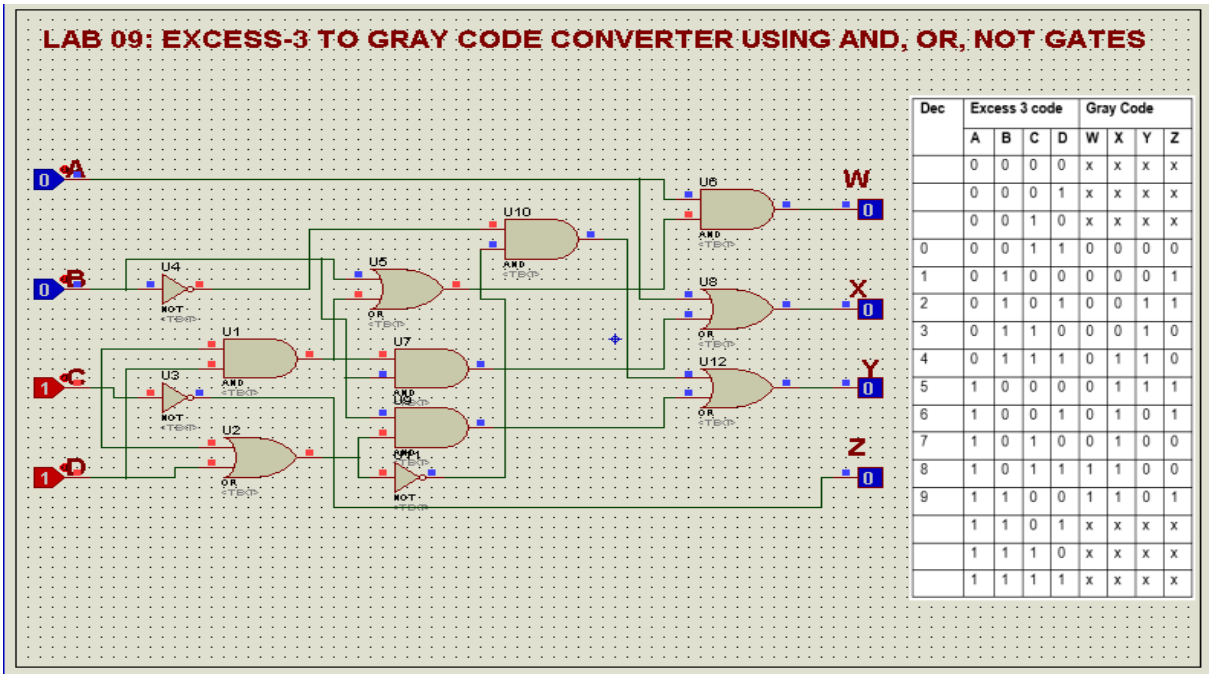
X = A + BCD

Y = B'C'D' + BD + BC

= B'(C + D)' + B(C + D)

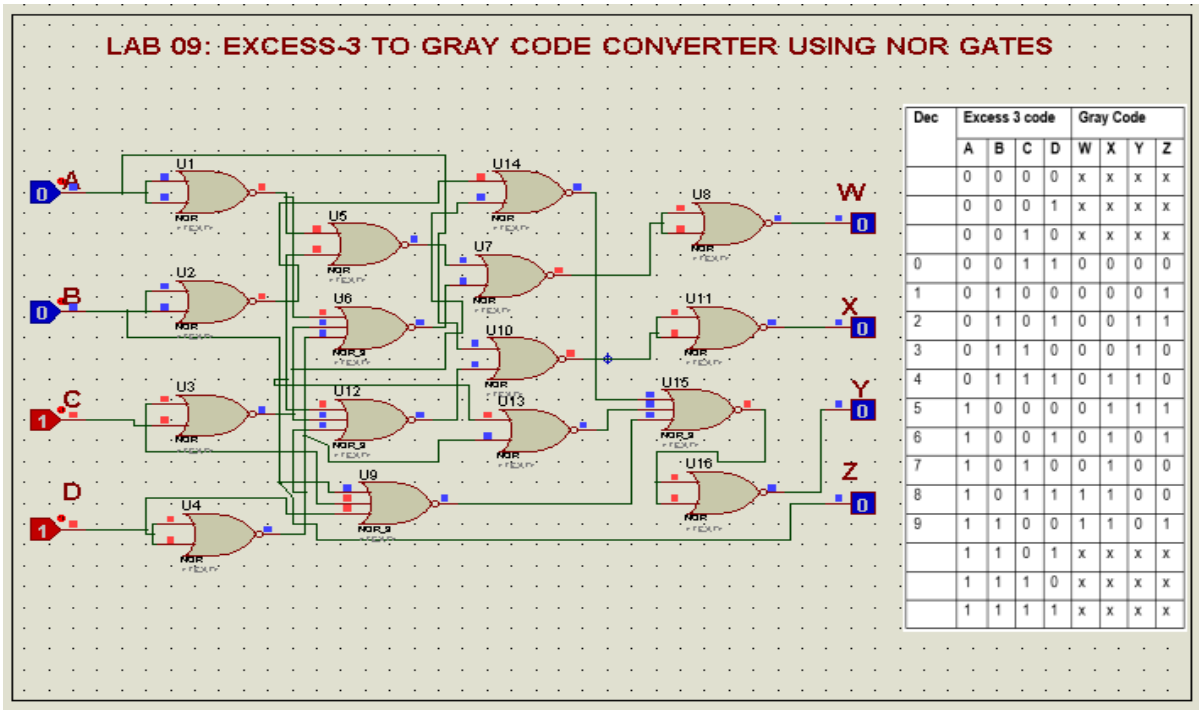
Z = C'

2. Draw the logic diagram for Excess-3 to gray code converter using AND, OR and NOT gates in the space provided below. You can use 2,3,4 input gates if required. (2 Marks- Modern tool usage)



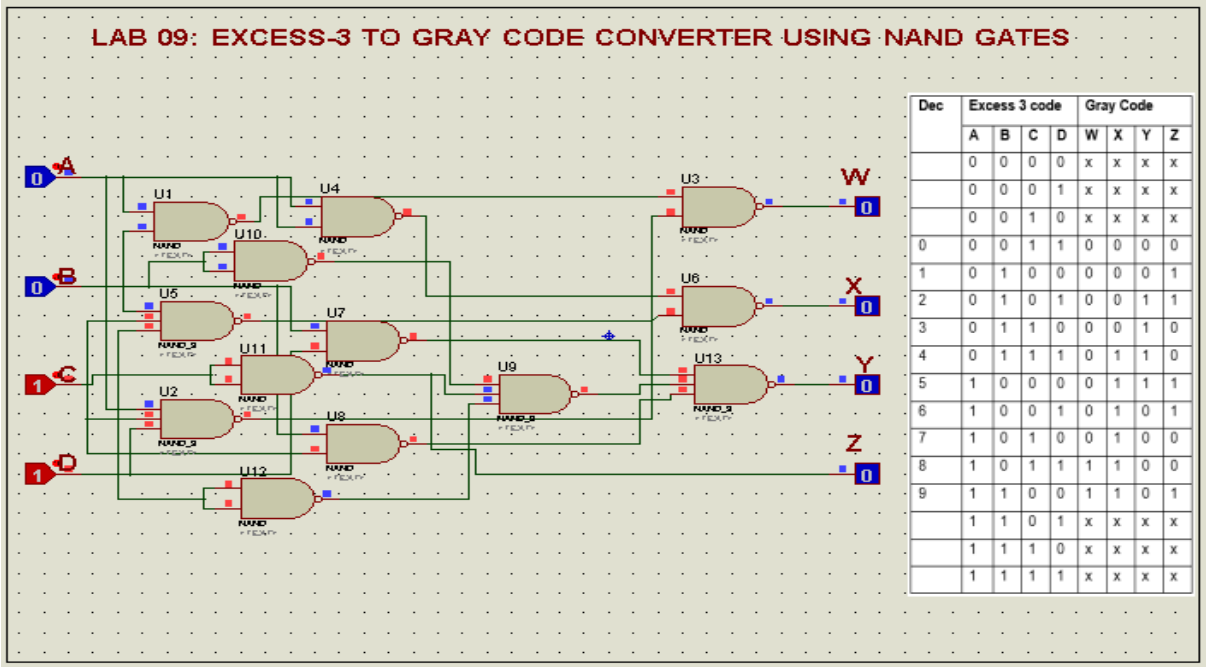
Dec	Excess 3 code				Gray Code			
	A	B	C	D	W	X	Y	Z
	0	0	0	0	x	x	x	x
	0	0	0	1	x	x	x	x
	0	0	1	0	x	x	x	x
0	0	0	1	1	0	0	0	0
1	0	1	0	0	0	0	0	1
2	0	1	0	1	0	0	1	1
3	0	1	1	0	0	0	1	0
4	0	1	1	1	0	1	1	0
5	1	0	0	0	0	1	1	1
6	1	0	0	1	0	1	0	1
7	1	0	1	0	0	1	0	0
8	1	0	1	1	1	1	0	0
9	1	1	0	0	1	1	0	1
	1	1	0	1	x	x	x	x
	1	1	1	0	x	x	x	x
	1	1	1	1	x	x	x	x

3. Draw the logic diagram for Excess-3 to gray code converter using only NOR gates in the space provided below, you can use 2,3,4 input NOR gates if required (3 Marks- **Individual. and Teamwork**)



Dec	Excess 3 code				Gray Code			
	A	B	C	D	W	X	Y	Z
	0	0	0	0	x	x	x	x
	0	0	0	1	x	x	x	x
	0	0	1	0	x	x	x	x
0	0	0	1	1	0	0	0	0
1	0	1	0	0	0	0	0	1
2	0	1	0	1	0	0	1	1
3	0	1	1	0	0	0	1	0
4	0	1	1	1	0	1	1	0
5	1	0	0	0	0	1	1	1
6	1	0	0	1	0	1	0	1
7	1	0	1	0	0	1	0	0
8	1	0	1	1	1	1	0	0
9	1	1	0	0	1	1	0	1
	1	1	0	1	x	x	x	x
	1	1	1	0	x	x	x	x
	1	1	1	1	x	x	x	x

4. Draw the logic diagram for Excess-3 to gray code converter using only NAND gates in the space provided below, you can use 2,3,4 input Nand gates if required (3 Marks- **Individual. and Teamwork**)



Dec	Excess 3 code				Gray Code			
	A	B	C	D	W	X	Y	Z
	0	0	0	0	x	x	x	x
	0	0	0	1	x	x	x	x
	0	0	1	0	x	x	x	x
0	0	0	1	1	0	0	0	0
1	0	1	0	0	0	0	0	1
2	0	1	0	1	0	0	1	1
3	0	1	1	0	0	0	1	0
4	0	1	1	1	0	1	1	0
5	1	0	0	0	0	1	1	1
6	1	0	0	1	0	1	0	1
7	1	0	1	0	0	1	0	0
8	1	0	1	1	1	1	0	0
9	1	1	0	0	1	1	0	1
	1	1	0	1	x	x	x	x
	1	1	1	0	x	x	x	x
	1	1	1	1	x	x	x	x

K-Maps for NAND Gate:

CD / AB	00	01	11	10
00	X	X	0	X
01	0	0	0	0
11	1	X	X	X
10	0	0	1	0

W = ((AB)'(ACD)')'

CD / AB	00	01	11	10
00	X	X	0	X
01	0	0	1	0
11	1	X	X	X
10	1	1	1	1

X = (A'(BCD)')'

CD / AB	00	01	11	10
00	X	X	0	X
01	0	1	1	1
11	0	X	X	X
10	1	0	0	0

Y = (B'C'D')'(BD)'(BC)')'

CD / AB	00	01	11	10
00	X	X	0	X
01	1	1	0	0
11	1	X	X	X
10	1	1	0	0

Z = C'

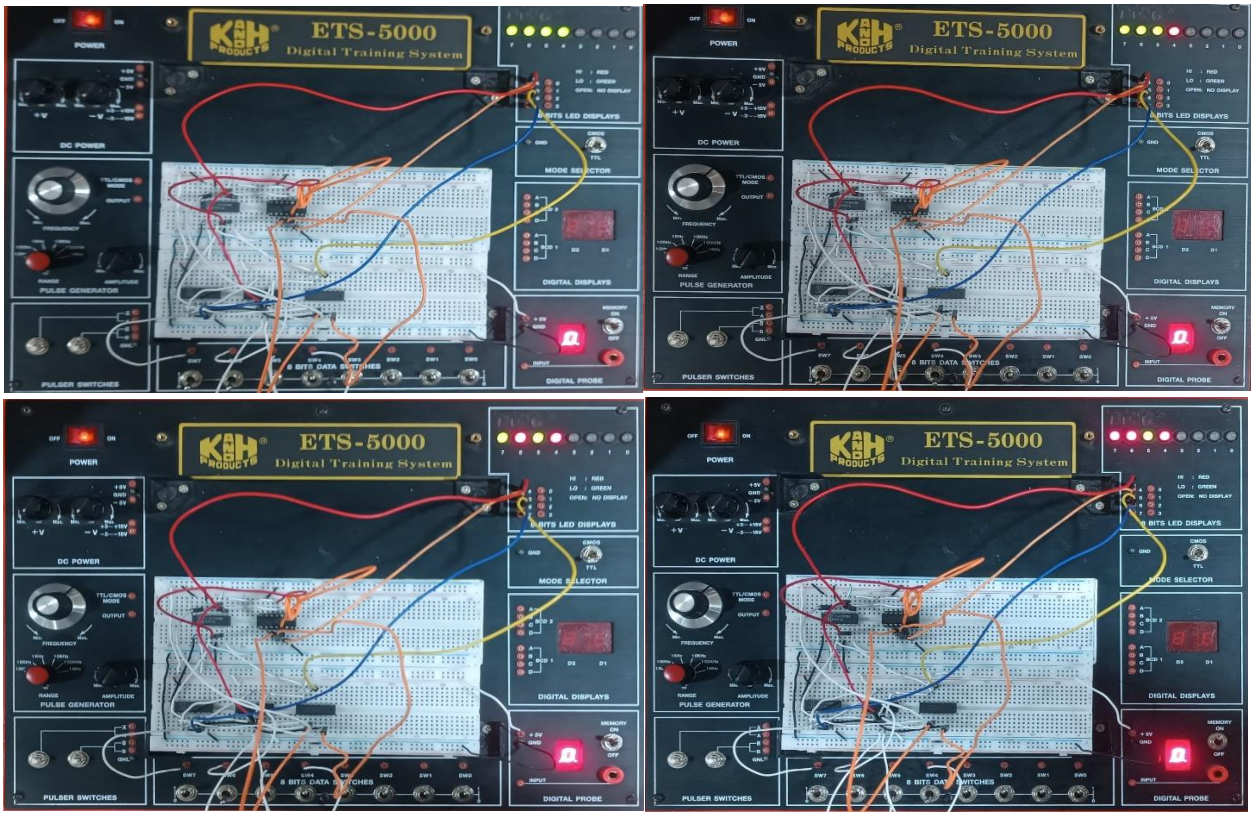
Lab Tasks: (To be completed in the lab)

Lab Task 1:

Implement Excess-3 to gray code converter using only NAND gates on hardware. Paste the complete circuit diagram, depicting hardware results. (5 Marks - Analysis)

Dec	Excess 3				Gray Code Hardware result			
	A	B	C	D	W	X	Y	Z
0	0	0	1	1	0	0	0	0
1	0	1	0	**0**	0	0	0	1
2	0	1	0	1	0	0	1	1
3	0	1	1	0	0	0	1	0
4	0	1	1	1	0	1	1	0
5	1	0	0	0	0	1	1	1
6	1	0	0	1	0	1	0	1
7	1	0	1	0	0	1	0	0
8	1	0	1	1	1	1	0	0
9	1	1	0	0	1	1	0	1

Hardware:



Lab Task2:

Design and simulate the circuit k-map equations you obtained in Pre-lab task 1 in Verilog **dataflow** modeling. Give the code and testbench and waveform in the space provided below.

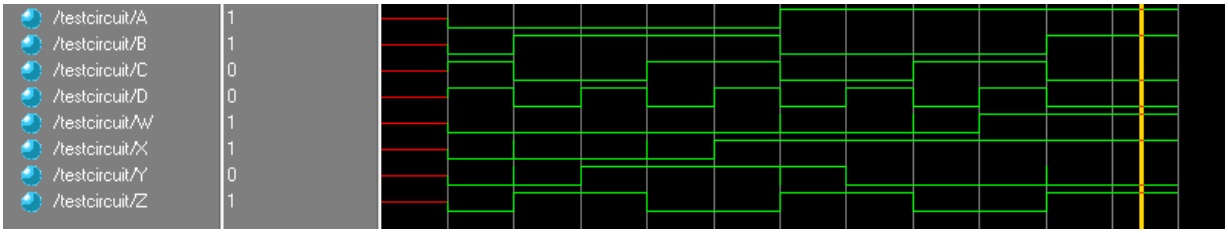
(3Marks – Modern tool usage)

Code:

```
module circuit ( w,x,y,z,a,b,c,d );
input a,b,c,d;
output w,x,y,z;
assign w = ~((~(a&b)) & (~(a&c&d)));
assign x = ~(~a & (~(b&c&d)));
assign y = ~((~(b&c)) & (~(b&d)) & (~(~b & ~c & ~d)));
assign z = ~c;
endmodule

module testcircuit;
reg A,B,C,D;
wire W,X,Y,Z;
circuit testcircuit ( W,X,Y,Z,A,B,C,D);
initial
begin
#100 A= 1'b0;B= 1'b0;C=1'b1;D=1'b1;
#100 A= 1'b0;B= 1'b1;C=1'b0;D=1'b0;
#100 A= 1'b0;B= 1'b1;C=1'b0;D=1'b1;
#100 A= 1'b0;B= 1'b1;C=1'b1;D=1'b0;
#100 A= 1'b0;B= 1'b1;C=1'b1;D=1'b1;
#100 A= 1'b1;B= 1'b0;C=1'b0;D=1'b0;
#100 A= 1'b1;B= 1'b0;C=1'b0;D=1'b1;
#100 A= 1'b1;B= 1'b0;C=1'b1;D=1'b0;
#100 A= 1'b1;B= 1'b0;C=1'b1;D=1'b1;
#100 A= 1'b1;B= 1'b1;C=1'b0;D=1'b0;
end
endmodule
```

Output Waveform:



Conclusion:

In this lab, we implemented an Excess-3 to Gray Code Convertor in three different ways:

1. Using Basic Logic Gates,

2. Using NAND Gates,

3. Using NOR Gates. Therefore, we implemented a Boolean Function using two non-degenerate forms.