National University of Sciences and Technology (NUST)
School of Electrical Engineering and Computer Science

Department of Electrical Engineering

Faculty Member: Engg. Arshad Nazir   **Dated:** December 14, 2023

Semester: 3rd   **Section:** BEE-14D

Group No.: 10

EE-221: Digital Logic Design

Assessment Rubrics for Lab 13 (Open Ended Lab): Design of a BCD to Seven Segment decoder circuit with 4-Digits multiplexed display using MSI ICs.

		PLO4/CLO4	PLO4/CLO4	PLO5/CLO5	PLO8/CLO6	PLO9/CLO7	
Name	**Reg. No**	Viva / Lab Performance 5 Marks	Analysis of data in Lab Report 5 Marks	Modern Tool Usage 5 Marks	Ethics and Safety 5 Marks	Individual and Teamwork 5 Marks	Total marks Obtained 25 Marks
Irfa Farooq	412564						
Arooj Fatima	423365						
Ahmad Nasir	409959						
Haseeb Umer	427442						

Lab13: Design of a BCD to Seven Segment decoder circuit with 4-Digits multiplexed display using MSI ICs.

The aim of this lab experiment is to enhance student's prototyping skills related to the digital circuits. In this lab they will get familiarized with use of different MSI ICs of their own choice available in the lab to design a **BCD-to-Seven-Segment Decoder** for multiplexed display and use the available ICs to **display last two digits of their CMS ID**. This lab requires some knowledge of combinational circuits like Multiplexers, Decoders/Demultiplexers, Encoders, Tristate gates, different type of logic gates, and multiple Numeric Read-out Displays.
(Different designs with the same functionality are acceptable.)

Objectives

- ✓ Design and verify combinational circuit design using different implementation models.
- ✓ Understand the function of Multiplexers, Decoders/Demultiplexers, Tristate gates, different logic gates and their application in digital design.
- ✓ Familiarization with BCD-to-Seven-Segment Decoder IC as a driver to drive Numeric Read-out.
- ✓ Transform any problem statement to truth table description and choose output functions that need Multiplexers implementation or other simplification techniques using logic gates.
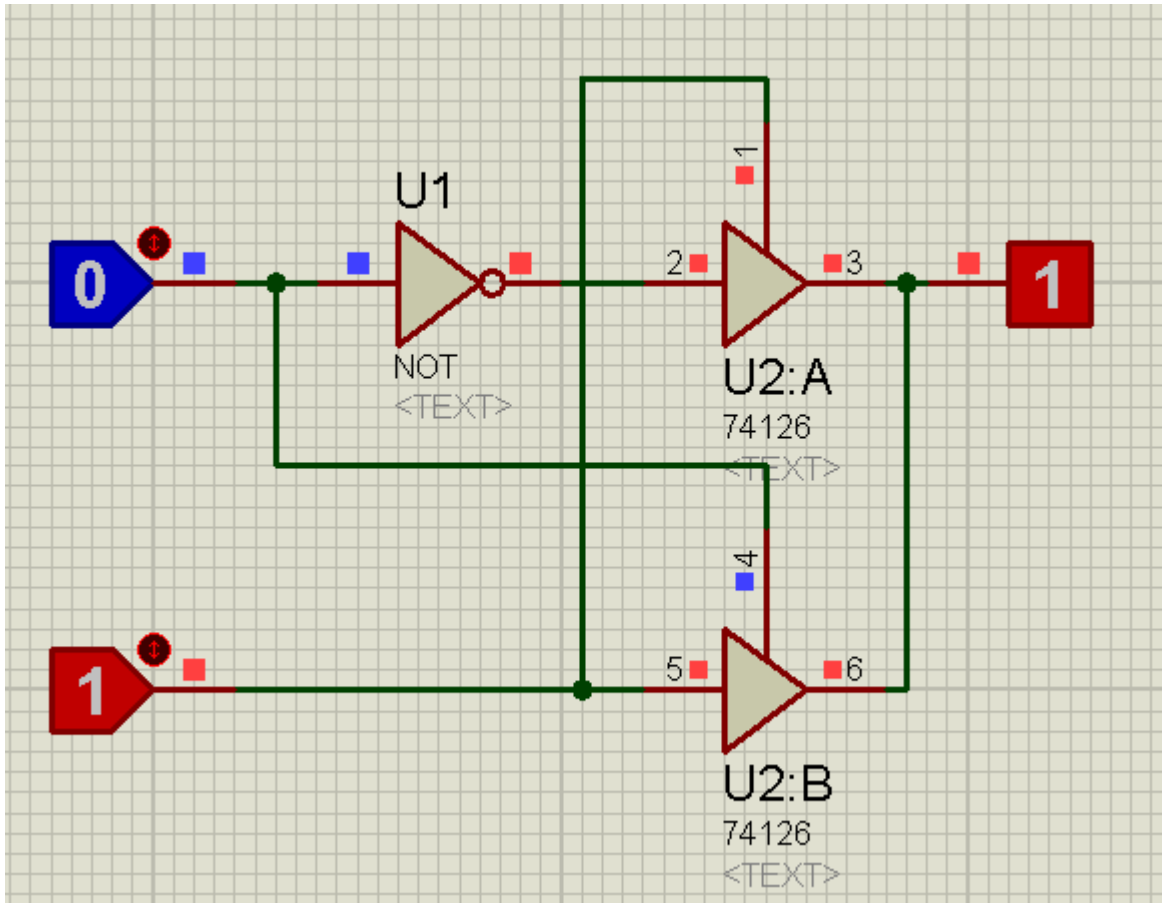
Lab Instructions

- ✓ This lab activity comprises three parts, namely Pre-lab, Lab tasks, and post-Lab Viva session.
- ✓ The lab report will be uploaded on LMS two to three weeks before scheduled lab date. The students will get hard copy of lab report, complete the Pre-lab task before coming to the lab and deposit it with teacher/lab engineer for necessary evaluation.
- ✓ The students will start lab task and demonstrate design steps separately for step-wise evaluation (course instructor/lab engineer will sign each step after ascertaining functional verification)
- ✓ Remember that a neat logic diagram with pins numbered coupled with nicely patched circuit will simplify trouble-shooting process.
- ✓ After the lab, students are expected to unwire the circuit and deposit back components before leaving.
- ✓ The students will complete lab task and submit complete report to Lab Engineer before leaving lab.
- ✓ There are related questions at the end of this activity. Give complete answers.

A. Pre-Lab Tasks

1. Draw the circuit that shows how to implement two input XOR function using two tristate buffers and one NOT gate.   **(3 marks)**
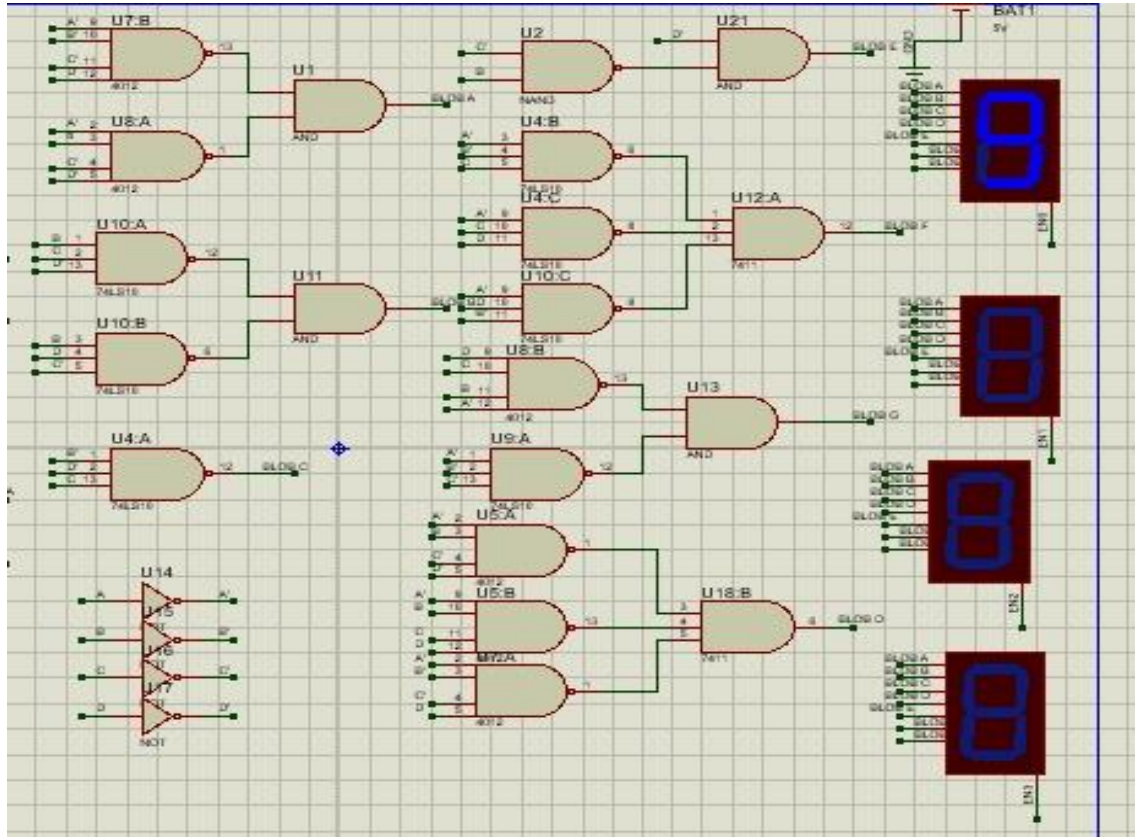

2. Fill in the following truth table for BCD-to-Seven-segment Decoder/Driver.   **(3 marks)**

Digit	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

3. Draw the Block/Logic diagram of BCD-to-Seven-segment Decoder/Driver using any kind of MSI ICs available in the lab. **(4 Marks)**
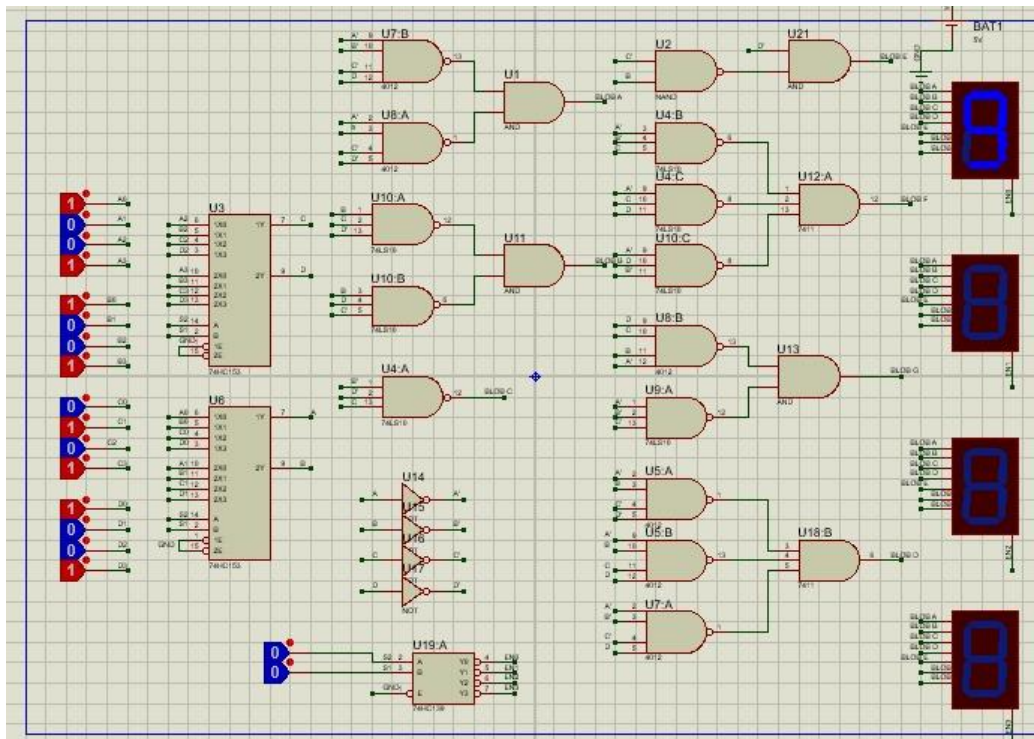
B. Lab Task

(Complete the design and simulation work before coming to the lab)

4. Design BCD-to-Seven-segment Decoder/Driver Circuit using any MSI ICs of your own choice and show it to your teacher/lab Engr. **(5 marks)**
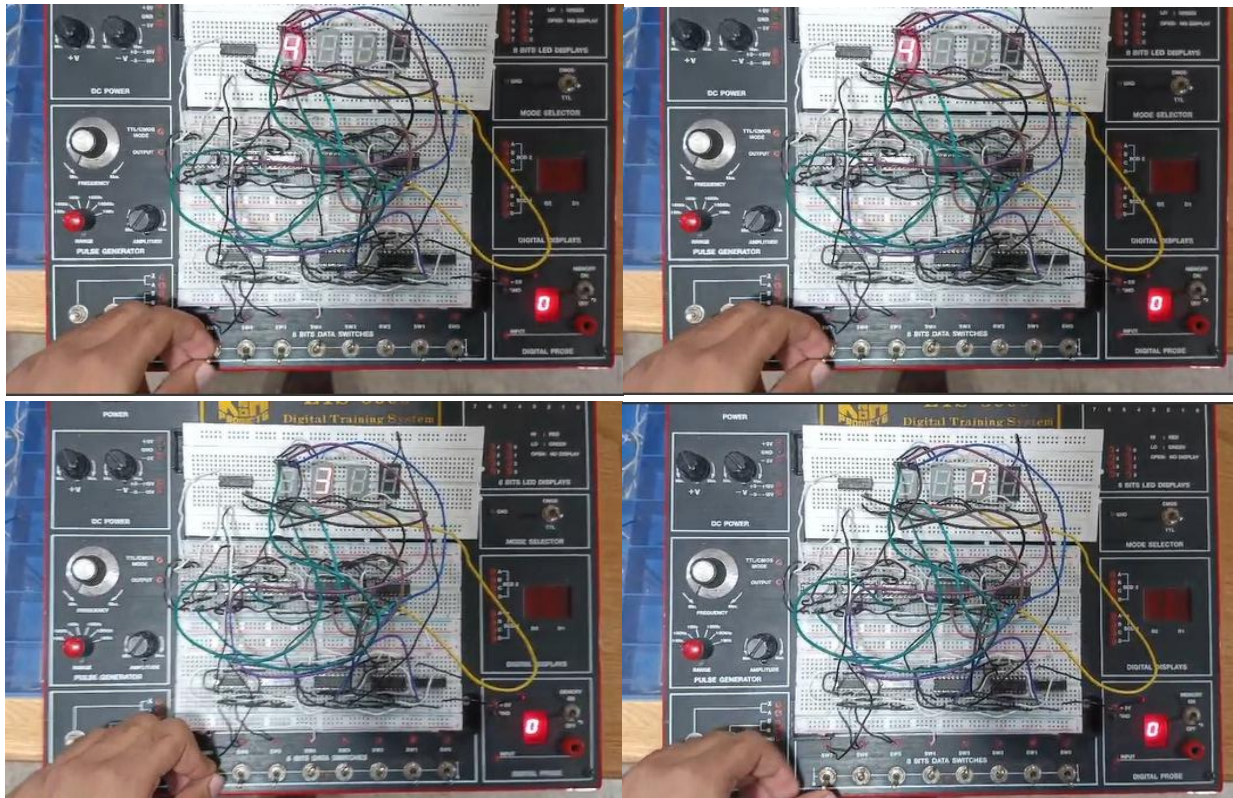
5. Show your complete circuit in working condition after completing the **Logic Diagram** with the ICs name and Configuration and implement it in hardware. **(10 Marks)**

ICs you may use in this lab.
1. All types of gates available in the lab
2. Decoder/Driver IC
3. Multiplexers, Decoders/DE multiplexers
4. Seven segment displays (Common anode or cathode)
5. Tristate buffer IC

Hardware Pictures:

Conclusion:

In this lad, we implemented two-level NAND AND implementation and designed a circuit to represent last four digit of our CMS. This allowed us to understand the working of 74153 MUX and 74139 decoder ICS along with NAND AND concepts.