National University of Sciences and Technology (NUST)
School of Electrical Engineering and Computer Science

Department of Electrical Engineering

Faculty Member: Sir. Arshad Nazir

Dated: 30th November 2023

Semester: 3rd

Section: D

Group No.: 10

EE-221: Digital Logic Design

Assessment Rubrics for Lab 11: Memory Elements: Latches and Flip-Flops

		PLO4/CLO4	PLO4/CLO4	PLO5/CLO5	PLO8/CLO6	PLO9/CLO7	
Name	**Reg. No**	**Viva / Lab Performance**	**Analysis of data in Lab Report**	**Modern Tool Usage**	**Ethics and Safety**	**Individual and Team Work**	**Total marks Obtained**
		5 Marks	**5 Marks**	**5 Marks**	**5 Marks**	**5 Marks**	**25 Marks**
Arooj Fatima	423356						
Ahmad Nasir	409959						
Haseeb Umer	427442						
Irfa Farooq	412564						

Lab11: Sequential Logic: Memory Elements: Latches and Flip-Flops

This Lab experiment has been designed to familiarize the students with use of Flip-Flops

Objectives

- ✓ Learn working of SR Latch and the way it can be constructed using NOR and NAND gates
- ✓ Modifying the SR Latch circuit to transparent latch (D-Latch)
- ✓ Design D type positive edge-triggered Flip-Flop using SR Latched

Lab Instructions

- ✓ This lab activity comprises three parts, namely Pre-lab, Lab tasks, and Post-Lab Viva session.
- ✓ The lab report will be uploaded on LMS three days before scheduled lab date. The students will get hard copy of lab report, complete the Pre-lab task before coming to the lab and deposit it with teacher/lab engineer for necessary evaluation.
- ✓ The students will start lab task and demonstrate design steps separately for step-wise evaluation (course instructor/lab engineer will sign each step after ascertaining functional verification)
- ✓ Remember that a neat logic diagram with pins numbered coupled with nicely patched circuit will simplify trouble-shooting process.
- ✓ After the lab, students are expected to unwire the circuit and deposit back components before leaving.
- ✓ The students will complete lab task and submit complete report to Lab Engineer before leaving lab.
- ✓ There are related questions at the end of this activity. Give complete answers.

A. Pre-Lab Tasks (5 marks – Individual and teamwork)

1. Differentiate between the Combinational and Sequential Circuit.

2. Differentiate between the Synchronous Sequential logic and Asynchronous Sequential logic.
3. Draw the logic diagram of SR Latch using NOR Gates. Also give its function table.
4. The SR Latch can also be constructed using NAND Gates. Differentiate between the two implementations of SR Latches using Logic Diagram and function table:
5. What are the set and reset conditions for SR and S´R´ Latches?
6. What is the undefined state for the Latches and how it occurs? How can you evaluate its behavior in this state?
7. How can we remove the problem of undefined state using D Latch? Give Logic Diagram of D Latch.
8. The essential elements of Sequential Circuits are memory elements. The two basic types of memory elements are Latches and Flip-Flops. What is the basic Difference between them?
9. Give the graphic symbols for SR, S'R' and D Latch

B. Lab Task (10 marks – Tool Usage and Analysis)

SR Latch:

10. Implement the SR Latch using a) NOR and b) NAND gates and show it to Lab Instructor. Give Logic Diagram, Function Table, and State Table for both designs. What is the difference between the two implementations?

D-Latch:

11. Implement the D-Latch and show it to your Lab Instructor. Give Logic Diagram and Function Table. What advantage does it have over SR Latch?

Flip-Flop:

12. Implement a D-type positive edge-triggered Flip-Flop using S.R. latches. What gates would you need for the implementation? Give Logic Diagram, Graphic Symbols and Characteristic Table. What change would be needed to design a negative edge triggered Flip-Flop?
13. Add CLEAR (Direct-reset) and PRESET (Direct-set) to the Flip-Flop. What are the functions of these inputs?
14. D Flip-Flop IC is 7474. Give its PIN Configuration, Function table and internal IC circuit. Draw its state diagram and compare working of IC to you design in 13