National University of Sciences and Technology (NUST)
School of Electrical Engineering and Computer Science

Department of Electrical Engineering

Faculty Member: Mr. Arshad Nazir **Dated: 23rd November 2023**

Semester: Fall 2023 **Section: BEE-14-D**

Group No.: 10

EE-221: Digital Logic Design

Lab 10: Magnitude Comparator

		PLO4/CLO4	PLO4/CLO4	PLO5/CLO5	PLO8/CLO6	PLO9/CLO7	
Name	**Reg. No**	**Viva / Lab Performance** **5 Marks**	**Analysis of data in Lab Report** **5 Marks**	**Modern Tool Usage** **5 Marks**	**Ethics and Safety** **5 Marks**	**Individual and Team Work** **5 Marks**	**Total marks Obtained** **25 Marks**
Arooj Fatima	423365						
Ahmad Nasir	409959						
Haseeb Umar	427442						
Irfa Farooq	412564						

Lab 10: Magnitude Comparator

This Lab Activity has been designed to familiarize students with design and working of combinational circuits using basic logic gates.

Objectives:

- ✓ Design and Implementation of 2-bit magnitude comparator using classical design method learned in the class.
- ✓ Design of a 4-bit magnitude comparator using a 4-bit adder IC and logic gates
- ✓ Verification of 4 bit comparator IC
- ✓ Dataflow modeling in Verilog HDL

Lab Instructions

- ✓ This lab activity comprises three parts, namely Pre-lab, Lab tasks, and Post-Lab Viva session.
- ✓ The lab report will be uploaded on LMS three days before scheduled lab date. The students will get hard copy of lab report, complete the Pre-lab task before coming to the lab and deposit it with teacher/lab engineer for necessary evaluation.
- ✓ The students will start lab task and demonstrate design steps separately for step-wise evaluation(course instructor/lab engineer will sign each step after ascertaining functional verification)
- ✓ Remember that a neat logic diagram with pins numbered coupled with nicely patched circuit will simplify trouble-shooting process.
- ✓ After the lab, students are expected to unwire the circuit and deposit back components before leaving.
- ✓ The students will complete lab task and submit complete report to Lab Engineer before leaving lab.
- ✓ There are related questions at the end of this activity. Give complete answers.

Pre-Lab Tasks:5 marks (5 marks Individual and team work- Evaluated in the start of the lab)

1. **What do you mean by a comparator circuit?**

   Answer: A comparator circuit is a combinational circuit that determines the relative magnitudes of two numbers. It compares two numbers A and B and determines whether one number is greater than, equal to or lesser than the other.

   Draw the truth table for a 1-bit magnitude comparator. The comparator has 2 inputs (A and B) and 3 outputs E, L and G for (A=B), (A<B) and (A>B) respectively.

A	B	A=B	A<B	A>B
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	0

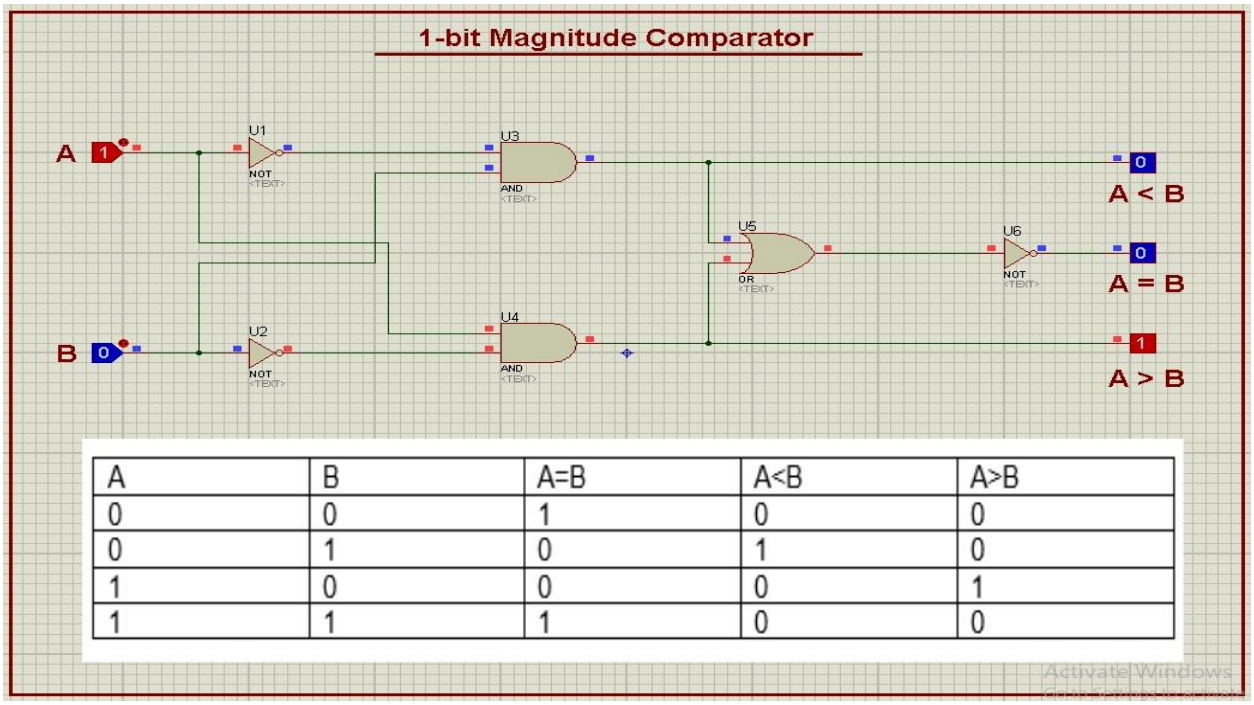
2. **Simplify the functions E, G and L and give their Logic diagrams.**

E= A'B' + AB

L= A'B

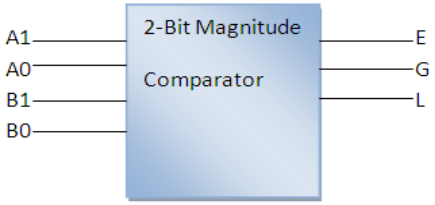
G=AB'

Proteus Schematic:



A	B	A=B	A<B	A>B
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	1	0	0

3. Design a 2-bit magnitude comparator. The Block diagram is shown below.



a) List the truth table.

Inputs				Outputs		
A1	A0	B1	B0	E (A=B)	G (A>B)	L (A<B)
0	0	0	0	1	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	1	0

1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	0	1	1	0	0	1
1	1	0	0	0	1	0
1	1	0	1	0	1	0
1	1	1	0	0	1	0
1	1	1	1	1	0	0

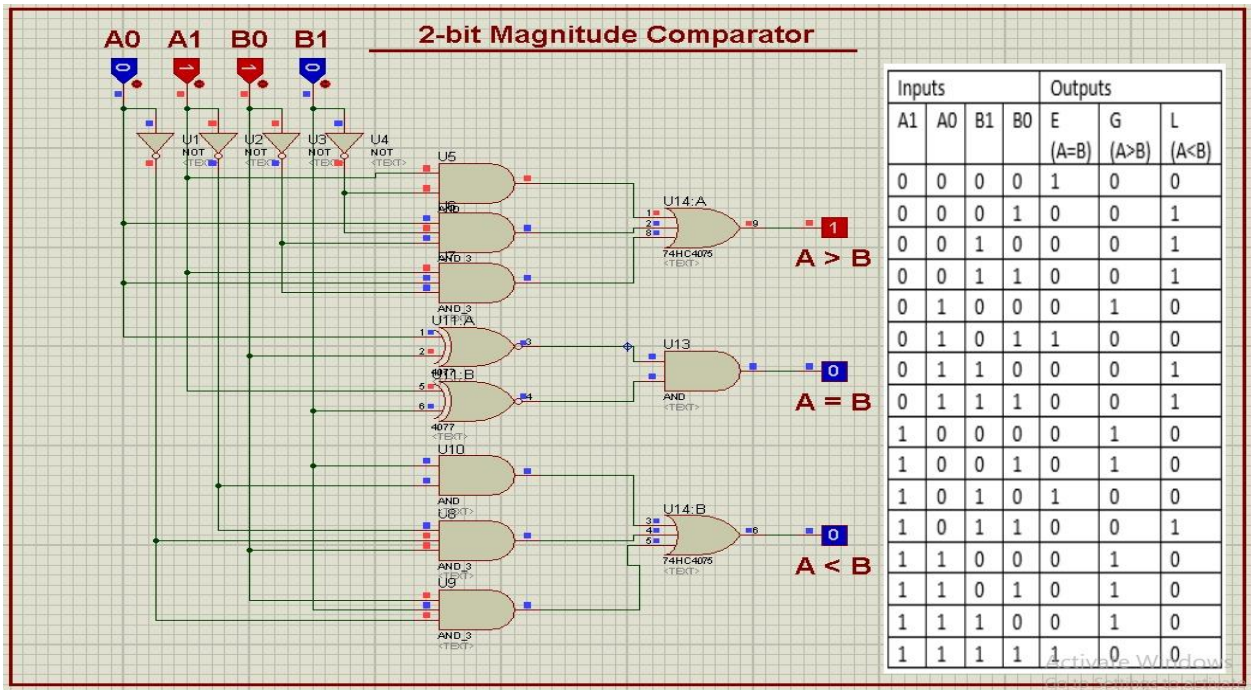
b) Simplify each of the functions E, G and L and give the logic diagram.

E= (A1'B1' + A1B1) + (A0B0 + A0'B0')

G= A1B1' + (A0B0 + A0'B0')(A0B0')

L= A1'B1 + (A0B0 + A0'B0')(A0'B0)

Logic Diagram:



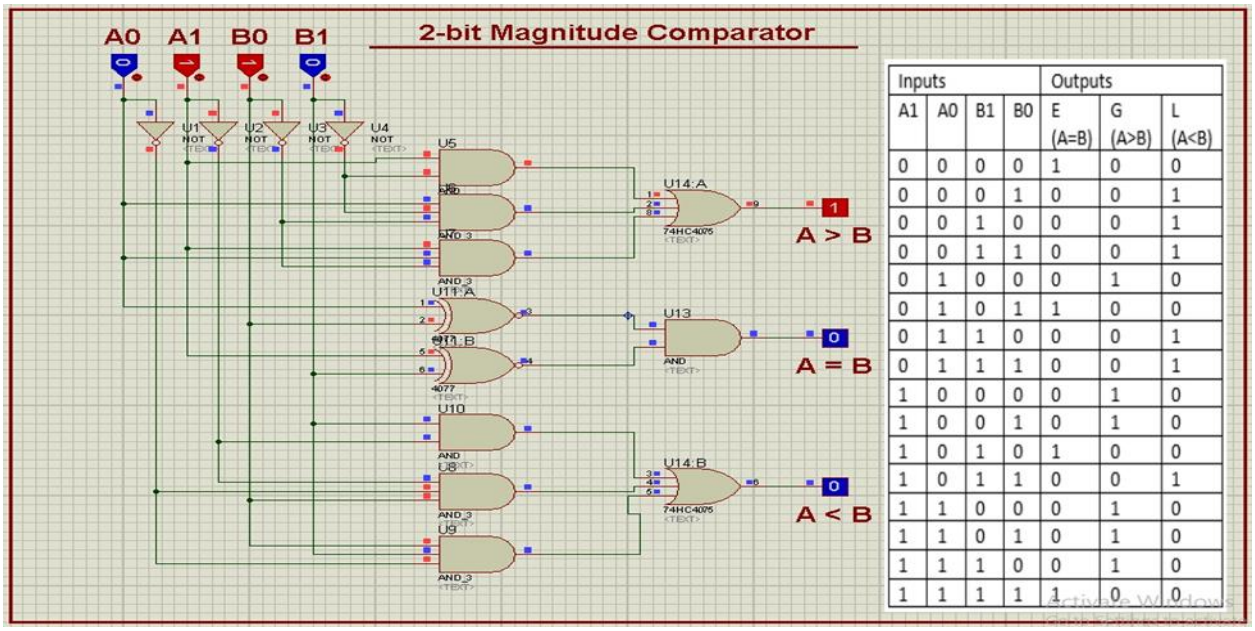
Inputs				Outputs		
A1	A0	B1	B0	E (A=B)	G (A>B)	L (A<B)
0	0	0	0	1	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	1	0
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	0	1	1	0	0	1
1	1	0	0	0	1	0
1	1	0	1	0	1	0
1	1	1	0	0	1	0
1	1	1	1	1	0	0

Lab Tasks: 10 marks

4. Implement the 2-bit Comparator circuit you arrived in your Pre-lab Task. Give the Complete circuit schematic diagram here again. (4 marks- Analysis)

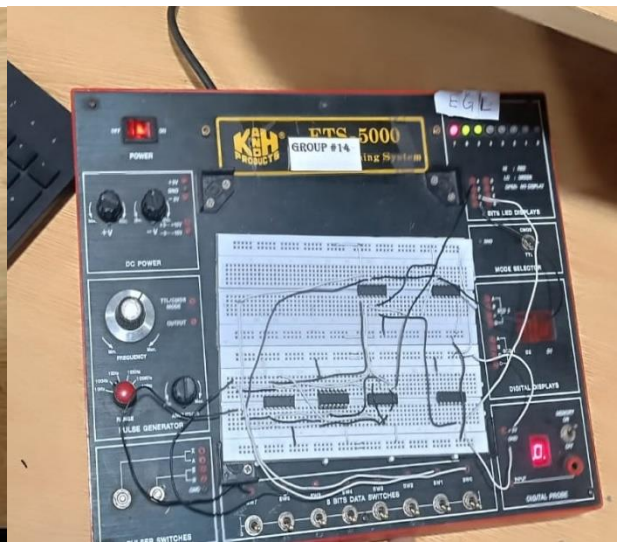
You can use following gates: NOT, AND, OR, XOR, NAND, NOR

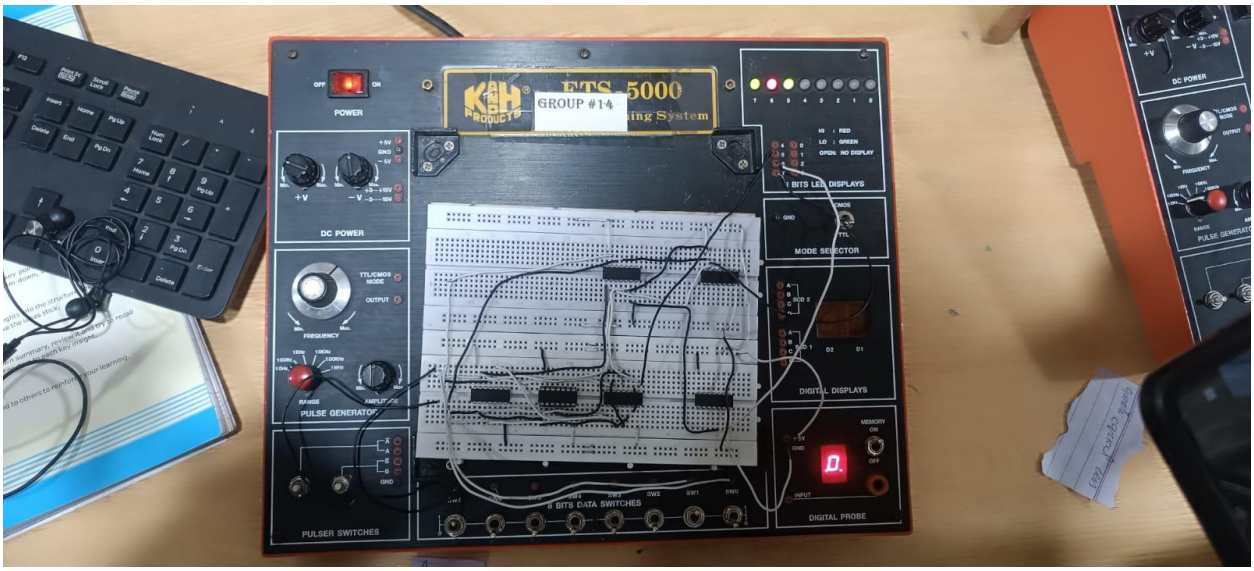
Proteus Schematic:



Inputs				Outputs		
A1	A0	B1	B0	E (A=B)	G (A>B)	L (A<B)
0	0	0	0	1	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	1	0	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	1	0
1	0	0	1	0	1	0
1	0	1	0	1	0	0
1	0	1	1	0	0	1
1	1	0	0	0	1	0
1	1	0	1	0	1	0
1	1	1	0	0	1	0
1	1	1	1	1	0	0

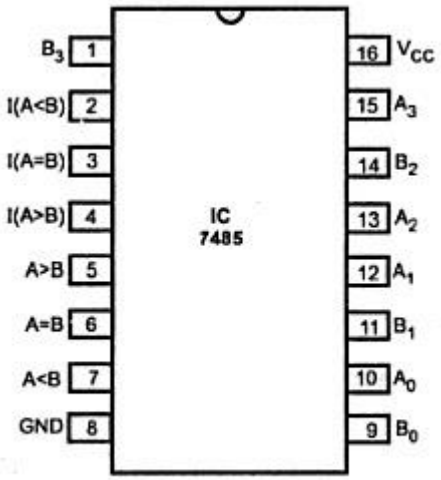
Hardware Implementation:





5. Get the 4-bit magnitude comparator IC (7485) from the lab. Give its function table, Pin Layout and show its implemented hardware. Does your results match with task4 results? If not, state its reason. (3 marks = 1-mark Analysis, 2 marks Modern tool usage)

Pin Layout:



(a) Pin diagram (IC 7485)

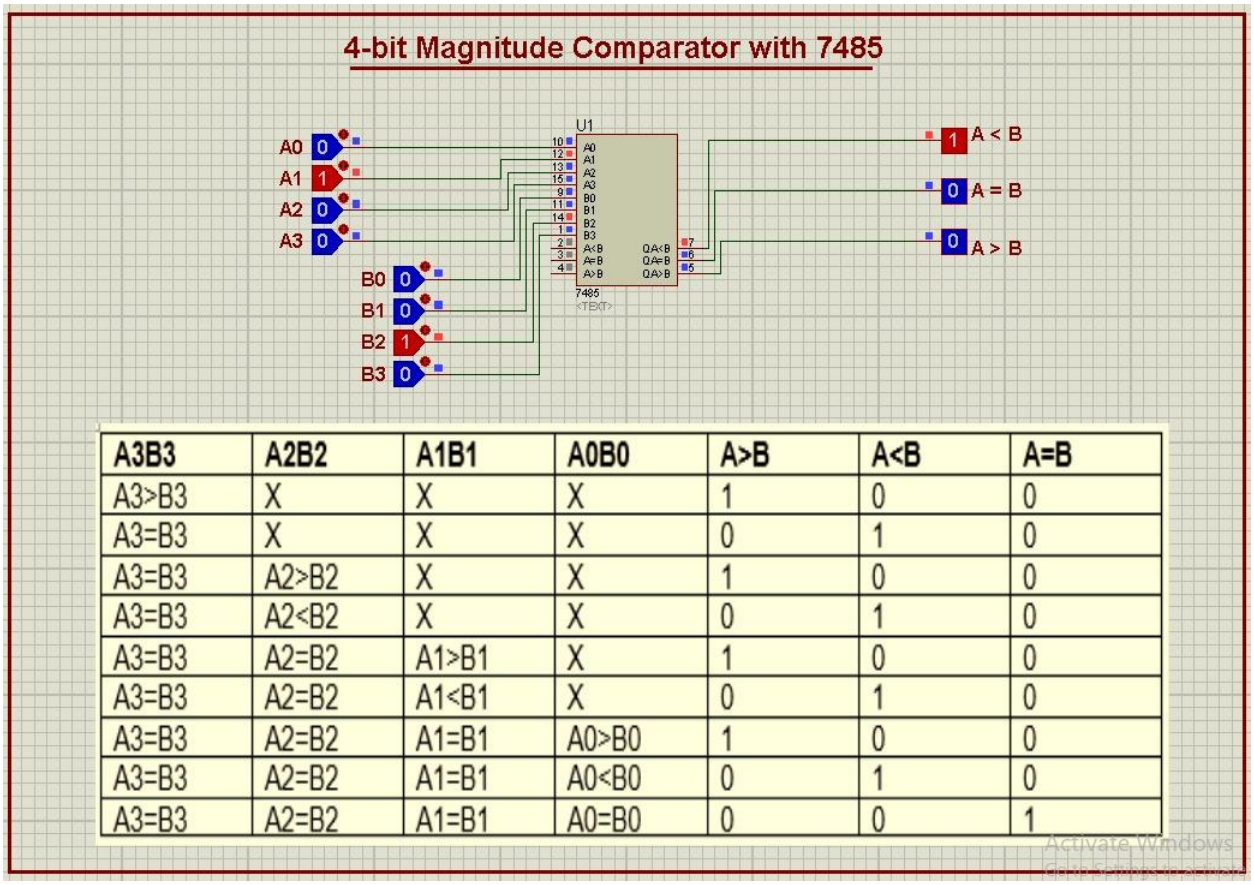
Function Table:

A3B3	A2B2	A1B1	A0B0	A>B	A<B	A=B
A3>B3	X	X	X	1	0	0
A3<B3	X	X	X	0	1	0
A3=B3	A2>B2	X	X	1	0	0
A3=B3	A2<B2	X	X	0	1	0
A3=B3	A2=B2	A1>B1	X	1	0	0
A3=B3	A2=B2	A1<B1	X	0	1	0
A3=B3	A2=B2	A1=B1	A0>B0	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1

Analysis:

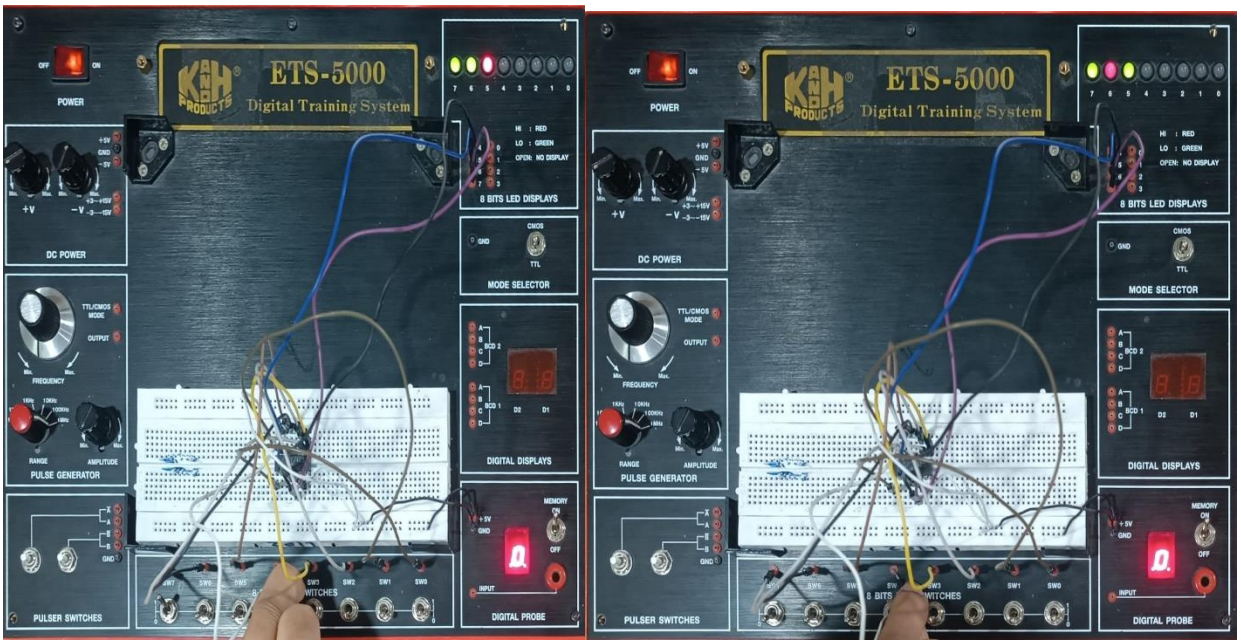
The results for the 7485 IC match with our function table and Proteus Schematic. It gives the correct output for all three conditions i.e. A=B, A>B and A<B.

Proteus Schematic:



A3B3	A2B2	A1B1	A0B0	A>B	A<B	A=B
A3>B3	X	X	X	1	0	0
A3=B3	X	X	X	0	1	0
A3=B3	A2>B2	X	X	1	0	0
A3=B3	A2<B2	X	X	0	1	0
A3=B3	A2=B2	A1>B1	X	1	0	0
A3=B3	A2=B2	A1<B1	X	0	1	0
A3=B3	A2=B2	A1=B1	A0>B0	1	0	0
A3=B3	A2=B2	A1=B1	A0<B0	0	1	0
A3=B3	A2=B2	A1=B1	A0=B0	0	0	1

Hardware Implementation:



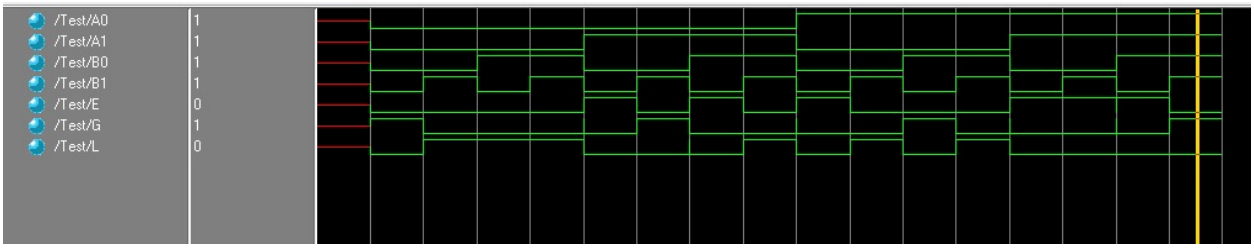
6. Write Verilog code of 2-bit comparator using dataflow modeling. (3 marks - Modern tool usage)

```
module Lab_10 (e, g, l, a0, a1, b0, b1);
output e, g, l;
input a0, a1, b0, b1;
assign e = (a1 & ~b1)|(a0 & ~b1 & ~b0)|(a1 & a0 & ~b0);
assign g = ~(a0 ^ b0) & ~(a1 ^ b1);
assign l = (~a1 & b1) | (~a0 & b0 & b1) | (~a1 & ~a0 & b0);
endmodule

module Test;
wire E, G, L;
reg A0, A1, B0, B1;
Lab_10 T1(E, G, L, A0, A1, B0, B1);

initial
begin
        #100 A0=1'b0; A1=1'b0; B0=1'b0; B1=1'b0;
        #100 A0=1'b0; A1=1'b0; B0=1'b0; B1=1'b1;
        #100 A0=1'b0; A1=1'b0; B0=1'b1; B1=1'b0;
        #100 A0=1'b0; A1=1'b0; B0=1'b1; B1=1'b1;
        #100 A0=1'b0; A1=1'b1; B0=1'b0; B1=1'b0;
        #100 A0=1'b0; A1=1'b1; B0=1'b0; B1=1'b1;
        #100 A0=1'b0; A1=1'b1; B0=1'b1; B1=1'b0;
        #100 A0=1'b0; A1=1'b1; B0=1'b1; B1=1'b1;
        #100 A0=1'b1; A1=1'b0; B0=1'b0; B1=1'b0;
        #100 A0=1'b1; A1=1'b0; B0=1'b0; B1=1'b1;
        #100 A0=1'b1; A1=1'b0; B0=1'b1; B1=1'b0;
        #100 A0=1'b1; A1=1'b0; B0=1'b1; B1=1'b1;
        #100 A0=1'b1; A1=1'b1; B0=1'b0; B1=1'b0;
        #100 A0=1'b1; A1=1'b1; B0=1'b0; B1=1'b1;
        #100 A0=1'b1; A1=1'b1; B0=1'b1; B1=1'b0;
        #100 A0=1'b1; A1=1'b1; B0=1'b1; B1=1'b1;
end
endmodule
```

Output Waveform:



Conclusion:

In this lab, we implemented 1-bit and 2-bit magnitude comparator circuits using logic gates. In addition, the circuitry was implemented on Proteus prior to hardware patching. Verilog Coding for 2-bit magnitude comparator revealed the same results as our hardware and the derived truth table. Lastly, we also drew the function table for a 4-bit magnitude comparator and tested its IC i.e.,7485, which matched the truth table. Consequently, all hardware was verified using Proteus Schematics.