DIGITAL ELECTRONICS

NUMBER SYSTEM

1. *Positional number system* : The number called as digits which has both face and place value is called positional number system.
   Ex : $(742)_{10} \longrightarrow 7_1\ 4_1\ 2$ are called digit and 10 is called as base (or) radix
2. For any number system having base 'r' will have r number of digits.
   Ex : decimal number system of base 10 have 10 digits from 0 to 9
   Octal number system of base 8 have 8 digits from 0 to 7
   Hexadecimal system has a radix of 16. The digits use are 0 to 9, A, B, C, D, E, F
3. Conversion of a decimal number is repeatedly divided by the base 'r', and the remainder after each division is used to indicate the coefficient of the number to be formed. This is continued until nothing remains. This is valid for whole numbers only.
   Ex : $(16)_{10} \longrightarrow (10000)_2$

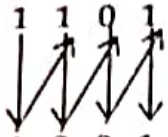
2	16
2	8 – 0
2	4 – 0
2	2 – 0
2	1 – 0
	0 – 1

4. The conversion of decimal fraction may be accomplished by repeated multiplication with base 'r' where r may be 2 or 8 or 16
   Ex : $(.25)_{10} \longrightarrow (.01)_2$
   $0.25 \times 2 = 0.5 \longrightarrow 0$
   $0.5 \times 2 = 1.0 \longrightarrow 1$
   hence to get any number to change it from decimal system to binary or octal or hexadecimal, we divide the integer part and multiply the decimal part.
5. Hexadecimal number system can be converted into binary by representing each hexadecimal number with 4 bit binary equivalent
   Ex : $(23)_{16} \longleftrightarrow (\overline{0010}\ \overline{0011})_2$
6. Octal number can be converted into binary by representing each octal number with 3 bit binary equivalent
   Ex : $(14)_8 \longleftrightarrow (\overline{001}\ \overline{100})_2$
7. Hexadecimal to octal number is obtained by using intermediate binary code.
8. Any weighted number system can be converted into decimal system is a follows :
   $X_3\ x_2\ x_1\ x_0\ .\ x^I\ x^{II}\ x^{III}$ can be converted into decimal by multipling each digit with r^0, r^1, r^2 ..... From integer LSB to MSB and r^{-1}, r^{-2} ..... by decimal fraction and adding.
   $(x_3)r^2 + (x_1)r^1 + (x_0)r^0\ .\ (x^I)r^{-1} + (x^{II})r^{-2} + (x^{III})r^{-3}$
   Ex : $(1011.11)_2 \longrightarrow 1x2^3 + 0x2^2 + 1x2^1 + 1x2^0\ .\ 1x2^{-1} + 1x2^{-2} = (11.75)_{10}$
9. Representation of negative numbers :
   (a) sign magnitude from
   (b) one's complement form
   (c) two's complement from

10. If the number is negative the left most bit is one
11. In sign magnitude method the MSB is used to represent sign (0 for + ve and 1 for -ve) and the remaining digits represent the magnitude in straight binary form
    Ex : $(8)_{10} \longrightarrow (01000)_2$
    $(-8)_{10} \longrightarrow (11000)_2$
12. In 1's complement representation +ve numbers are represented exactly in the same way as in sign magnitude. Whereas negative numbers are represented by subtracting equivalent +ve number from 2^{n-1} where 'n' is the no. of bits.
13. Any binary number can be converted into 1's complement from by replacing 0's into 1's and 1's into zeros.
14. In 2's complement representation +ve nos. are represented exactly in the same way as in sign magnitude. But in the -ve nos. the magnitude is represented in 2's component.
15. Any binary number can be converted into 2's complement form by representing first the number in 1's complement form and adding 1 to the LSB.
16. The right most bit of a binary no. is known as LSB and left most bit of a binary no. is known as MSB.
17. In a weighted number system the value of a digit depends on its position.
    Ex : binary, octal, decimal & hexadecimal etc.
18. A group of 4 bits is defined as a nibble.
19. A group of 8 bits is defined as a byte.
20. ASCII (American Standard Code for Information Interchange) code is 7 bit code ASCII code is alphanumeric code.
21. Excess 3 code is a self complement code.
22. Examples of un weighted codes are Gray code. Excess 3 code.
23. Gray code is a reselected code or unit distance code. In gray code successive numbers differ in only one bit. Hence to avoid "race" between bits gray code is used.
24. Binary to gray conversion :
    (i) Binary number $B_8\ B_4\ B_2\ B_1$
    $G_8=B_8$ $G_4=B_8 \oplus B_4$ $G_2=B_4 \oplus B_2$ $G_1=B_2 \oplus B_1$
    Hence gray number is $G_8\ G_4\ G_2\ G_1$
    (ii) (a) First gray digit is same as first digit in mSB
    (b) Add each pair of adjustant bit to get next gray digit discold any carry that occur

    Ex : 1 0 0 1 (Binary) 1 1 0 1 (Gray code)
25. Gray to binary conversion
    (i) Gray number is $G_8\ G_4\ G_2\ G_1$
    $B_8 = G_8$: $B_4 = G_8 \oplus G_4$
    $B_2 = G_8 \oplus G_4 \oplus G_2$; $B_1 = B_2 \oplus G_1$
    (ii) a) first binary bit is same as MSB of gray code
    b) add diagonally to get the next binary digit

Gray code 1 1 0 1



Binary code 1 0 0 1

26. The direct representation of decimal numbers can be accomplished by using a binary coded decimal (BCD) representation in which each decimal digits have four binary digits.

2 7

Ex : 27 → | 0010 | 0111 |

Parity bit is used to detect the errors in the binary bits. Hence I extra bit is added to ASCII code for parity checking.

27. In even parity method, the value of the parity bit is chosen so that the total number of 1s in code group is even number, including parity bit.
Ex: 1001101 represent in even parity as 01001101
1010100 represent in even parity as 11010100

28. In add parity method, the value of the parity bit chosen such that the total number is 1s in code group including parity bit is add.
Ex : 1001101 represent in odd parity as 11001101
1010100 represent in odd parity as 01010100

29. A group of digits and other symbols is known as string. Replacing a longer string by a shorter one is known as chunking.

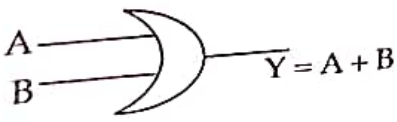
30. Excess 3 code is nothing but it is equivalent to the number in binary adding 11 to the binary number.

LOGIC GATES

1. Not gate : The output of a NOT gate takes on the 1 state if only if the input does not take the 1 state
This is also known as inverter.

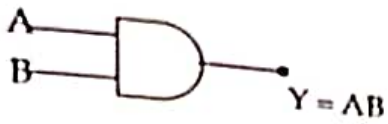
Truth Table	
A	Y
0	1
1	0

2. OR Gate : An OR gate has two or more inputs and a single output. The output of an OR gate is 1 state when one or more inputs assume the 1 state for OR gate 1 is the disable input.



Truth Table		
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

3. AND Gate : An AND gate has output 1 when all the inputs are 1. When any one of the input is zero output is zero. Hence is the disabled input to the AND gate. Disabled input means the gate can only depends on this input irrespect of other input



Truth Table		
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

4. NAND Gate : The output of NAND gate assumes '0' state if and only of all the inputs assumes the "1" state.

Truth Table		
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

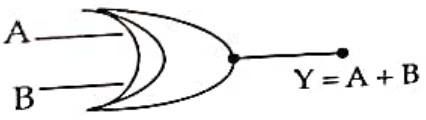
For NAND gate zero is disabled input

5. NOR Gate : A NOR gate has two or more inputs and a single output. The output of a NOR assumes '0' state if one or more input assumes the '1' state.

Truth Table		
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

6. EX – OR Gate : The output of a two input Ex – OR gate assumes '1' state if one and only one input assumes 1 state.

Boolean expression for Ex – OR gate is $Y = A \oplus B = AB + AB$.



Truth Table		
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

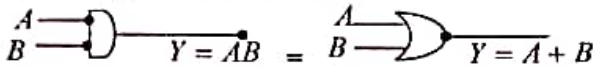
Ex – OR gate have output 1 when the input are different.

Commercially available Ex – OR gate has only two inputs.

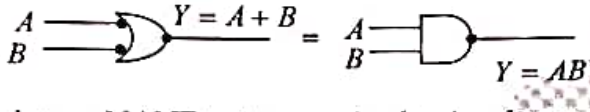
Ex – OR gate is used to compare the binary bits.

7. Unlike AND and OR gates, the inverter (NOT) gate cannot be constructed from diodes because an active circuit element is required to provide the power required in the inversion process.

8. In positive logic high voltage level is logic 1 and low voltage level is logic zero.
9. In negative logic high voltage level is logic zero and low voltage level is logical.
10. A negative OR gate is the same circuit as a positive AND gate and a negative AND is equivalent to positive OR gate.
11. AND gate also called coincidence gate.
12. OR gate is also called mixing gate.
13. NAND and NOR gates are called universal gates because using this gates we can realize any type of gate.
14. Bubbled AND gate is equivalent to NOR gate.



15. Bubbled OR gate is equivalent to NAND gate



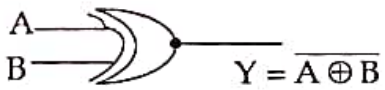
16. Number of minimum NAND gates required to implement other gates is follows.

Gate	No. of NAND gate required
NOT	1
AND	2
OR	3
EX – OR	4
EX – NOR	5

17. Number of minimum NOR gate required to implement other gates is as follows.

Gate	No. of NAND gate required
NOT	1
AND	3
OR	2
EX – OR	5
EX – NOR	4

18. AND gate is a combination of series switches.
19. OR gates is a combination of parallel switches
20. EX-NOR gate: in EX-NOR gate when both inputs are equal output is 1 and when inputs are different output is zero.



A	B	Y
0	0	1
0	1	0

1	0	0
1	1	1

21. Only Ex-OR gate has two inputs remaining gates have to or more inputs.
22. NOT gate can also be represented as

23. Enabled input means gate is working but output depends on remaining inputs also.
24.

IC. NO	Gate
7400	Quad 2 input NAND gate
7402	Quad 2 input NOR gate
7404	Hex inverter (NOT gate)
7408	Quad 2 input AND gate
7432	Quad 2 input OR gate
7486	Quad 2 input EX – OR gate

Quad means 4 gates available in a single IC chip.

25. NAND – NAND is equivalent to AND - OR
26. NOR – NOR is equivalent to OR - AND
27. AND – NOR is equivalent to NAND - AND
28. OR – NAND is equivalent to NOR - OR

BOOLEAN ALGEBRA

1. Boolean algebra is used to simplify the expressions. The advantage of simplification is reduced hardware i.e. less number of gates are required.
2. There are three methods to simplify Boolean expressions
   (a) Boolean algebra method
   (b) Karnaugh map method
   (c) Tabulation method
3. Boolean algebra theorems :

(i)	$A + 0 = A$	$A.1 = A \longrightarrow$ (i) (b)
(ii)	$A + 1 = 1$	$A.0 = 0 \longrightarrow$ (ii) (b)
(iii)	$A + A = A$	$A.A = A \longrightarrow$ (iii) (b)
(iv)	$A + \overline{A} = 1$	$A.\overline{A} = 0 \longrightarrow$ (iv) (b)

4. (i.a) is dual of (I.b) :
   (ii. a) is dual of (ii, b)
   (iii. a) is dual of (iii, b)
   (iv. a) is dual of (iv, b)
5. Duals can be written as follows.
   Given any equation in one column, the corresponding equation in the other column can be written by (I) interchange + and sings and (ii) interchange 0 and 1.
   The theorems which are related to one another by this double interchange is called duals.
   Ex : $A + AB = A \longrightarrow$ Dual is $A(A+B)$

6. $X = X$
7. $X + Y = Y + X$
8. $X.Y = Y.X$
9. $X + (Y + Z) = (X + Y) + Z$
10. $X + XZ = X(1+Z) = X$
11. $X(Y+Z) = XY + XZ$
12. $X(X+Y) = X$
13. $(X+Y)(X+Z) = X+YZ$
14. $X+\overline{X}Y = X+Y$
15. $XY + YZ + \overline{Y}Z = XY + Z$
16. Demorgain's theorems :
    $\overline{X+Y} = \overline{X}.\overline{Y}$ complement of a sum is equal to product of individual complement.
    $\overline{XY} = \overline{X} + \overline{Y}$ complement of product is equal to sum of individual complements.
17. Sum of products expression : A SOP expression is a product terms or several product terms are logically added.

Ex : $A\overline{B}C + A\overline{B}\overline{C} + ABC + \overline{A}BCD + ABCD$

18. Product of sum expression : A POS expression is a sum terms or several sum logically multiplied.
    Ex : $(A+B+\overline{C})(A+\overline{B}+C)(A+B+C)$
19. In sum of proudct form each individual term is referred to as a min term.
20. In product of sum form each individual terms is referred to as a max term.
21. Karnaugh – map method is used to simplify when the no. of terms in any expression is more.
22. When ever we see a pair of horizontally (or) vertically adjacent 1s we can eliminate the variable that goes from complemented to un complemented form (or) vice versa.
23. A quad is a group of four 1s that are horizontally (or) vertically adjacent.
24. A quad means two variables drop out of Boolean equation.
25. An octet is a group of eight 1's. Octet eliminates three variables and their complements.
26. Tabulation method is used to simplify Boolean expressions when there are more than 5 variables.

LOGIC FAMILIES

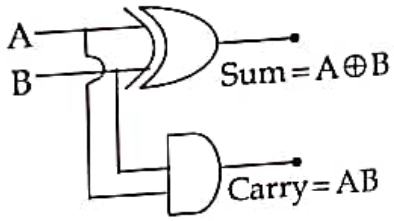
1. An integrated circuit consists of a single crystal silicon chip contains both active and passive elements and their inter connections.
2. According to level of complexity IC may be classified as SSI, MSI. LSI. VLSI.
3. SSI (Small Scale Integration) contains 1 to 12 gates
   MSI (Medium Scale Integration) contains 13 to 99 gates
   LSI (Large Scale Integration) contains 100 to 10000 gates.
   VLSI (Very Large Scale Integration) contains more than 10000 gates.
4. In Bipolar IC's NPN is prepared than PNP because NPN is more faster than PNP and NPN transistor requires +Ve power supply.
5. Bipolar families are more faster thanMOSFET (FET) families.

6. Bipolar occupies more space than FET in an IC. Hence MOSFET's are more prepared than BJT.
7. CMOS families require less power for its operation than any family.
8. The no. of gates driven by a single gate is referred to as the fanout of that gate.
9. The no. of input gates connected to logic circuit is referred to a fan in of that logic circuit.
10. Noise margin of a logic circuit is the maximum noise voltage added to the input of a digital circuit that does not cause an un wanted change in the binary state of the output.
11. Fan out is limited by the output of the driving gate is at the logic 1 level.
12. For maximum fan out. The output impedance of logic circuit is low for both logic '0' and logic '1' level.
13. In RTL (Resistor transistor logic) gates the basic gate is NOR.
14. Fan out of RTL gate is 5.
15. DTL gates perform NAND logic.
16. Propagation delay time in DTL gates are of the order of 30 –80 nano seconds.
17. To increase noise margin in DTL gate we use HTL gate.
18. HTL gate is high thresold logic which is modified version of DTL logic. In which zener diode is connected to increases noise margin.
19. To increase fan out of DTL gate we replace diode by transistor.
20. Emitter coupled logic (ECL) is also known as current mode logic (CML), current steeling logic, and non saturation logic.
21. ECL is the fastest logic family.
22. ECL offers complementary outputs, OR gates and NOR gate.
23. Typical propagation delay of ECL gate is 1 nano second.
24. Typical noise margin of ECL is 0.33V
25. TTL gates basic gate is NAND.
26. The advantage of active pull up (to tempole) over passive pull up :
    a) Increased speed of operation
    b) Reduced power dissipation
    c) Low output impedance
27. CMOS power dissipation is minimum than all other families.
28. Highest fan out is possible with CMOS logic because high input impedance
29. Typical fan out of CMOS logic is 50.
30. Negative supply is preferred in ECL to reduce the effect of noise present in the supply line.
31. Temperature range of 74 – series IC's are 0 to 70^0C.
32. Temperature range of 54 – series IC's are – 55^0c to 125^0c.
33. In the tristate logic in addition to two low output impedance output 0 & 1, there is third state known as high impedance.
34. Disadvantage of open collector or gates is their slow switching speed.

35. Higher suriching sped is possible in schottky transistor over normal transistor because the transistor is prevented form entering into saturation.
36. N – channel MOS devices are preferred over P channel MOS devices for digital circuit because higher mobility of electrons than holes.
37. In open collector wired operations is possible because of high output impedance.

COMBINATIONAL LOGIC CIRCUITS

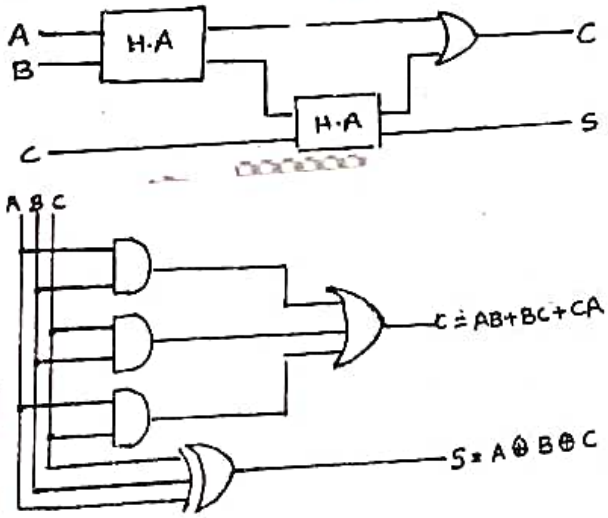
1. A two bit adder is called a half adder. Half adder has two inputs and two outputs.



Truth Table

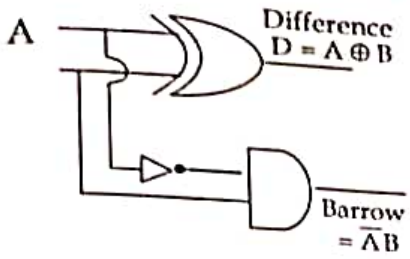
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

2. A gate structure which performs an addition of three bits is called a full adder.
3. Full adder consists of two half adder and 1 OR gate.
4. Full adder consists of 3 AND gates, 1 OR gate, 1 EX-OR gate.



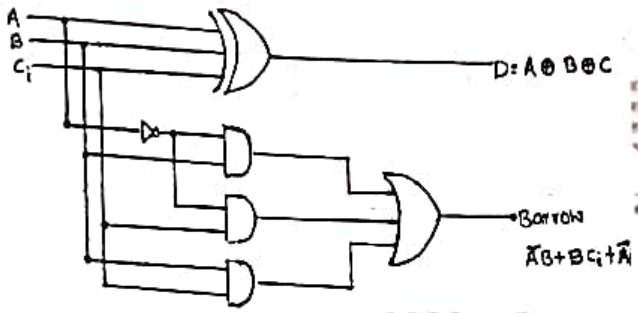
5. For a serial adder only one full adder is sufficient.
6. Serial adder is slowest adder. It requires N + 1 clock pulses to add. N bits.
7. Parallel adder require N full adder (or) N–1 full adder and one half adder, for N bit addition.
8. Parallel adder requires only clock pulse for its operation.
9. Parallel adder requires only clock pulse for its operation
10. For 4 bit addition 3 full address and 1 half adder is required.
11. Half subtractor : two bit subtractor is called half subtractor. It has two inputs and two outputs.

A is minuend, B is the subtrahend, D A – B the difference and C is the borrow



Truth Table			
A	B	D	C
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

12. Full subtractor accepts as inputs the minuend 'A' the subtrahend 'B' and a barrow from a previous order C.



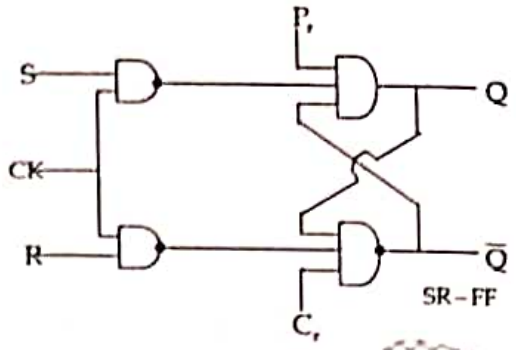
13. To realize a full subtractor two half subtractor and one OR gate is required.
14. Demultiplexer is a logic circuit that accepts one data output and distributes it over several outputs.
15. Multiplexer is a logic circuit that gates are out of several inputs to a single output.
16. Multiplexer can be used to realize any Boolean expression hence multiplexer is a universal logic circuit.
17. A 'n' variable Boolean expressions can be realized by using 2" 1 multiplexer.
18. Multiplexer and demultiplexer required control inputs.
19. Decoder is a logic circuit that decodes from binary to octal decimal. Hexa decimal.
20. Encoder has a number of inputs only one of which is one state and an n-bit code is generated depending upon which of the inputs is excited.
21. Two's complement is used to perform subtraction using adder instead of subtractor.
22. Encoder and decoder has no control inputs.
23. The ALU issued to perform arithmetic and logical operations
24. Combinational circuits cannot have memory elements.

SEQUENTIAL LOGIC CIRCUITS

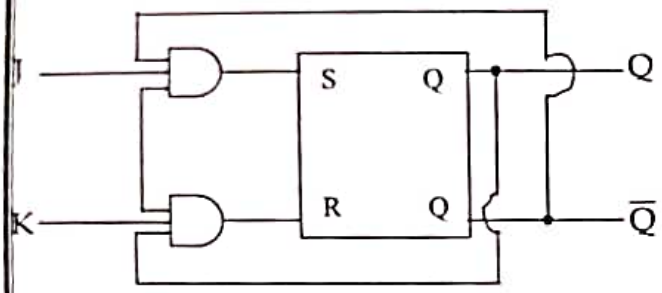
1. Sequential logic circuit output depends not only on the present inputs but also on the previous outputs.
2. Flips flop has two stable states.
3. A pair of cross coupled NOR gates is called a latch. R – S flip flop is known as latch.
4. The fundamental most important characteristic of a flip flop is that it has a "memory".
5. Flip flop is also called Binary (or) Bistable multivibrator.
6. Flip flop may store one bit of information.

7. A clocked R – S latch is called S – R flip flop.
8. In R – S flip flop S = 1, R = 1, is forbidden.

Sn	Rn	Qn + 1
0	0	Qn
1	0	1
0	1	0
1	1	forbidden



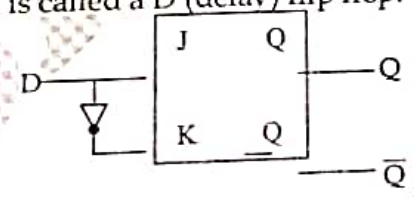
9. K – K flip flop removes the ambiguity of S – R flip flop.



Clock	J	K	
0	X	X	XC
1	0	0	NC
1	1	0	1
1	0	1	0
1	1	1	Toggle

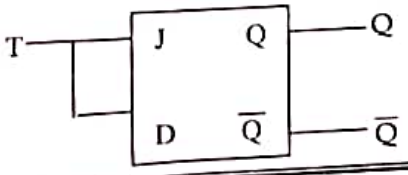
10. A J – K flip flop has feed back output to input. Because of this feed ack J – K flip flop toggles for both high inputs.
11. In J – K flip flop race around condition is occur.
12. Race around condition can be eliminated by keeping clock pulse width less than propagation delay time (or) by increasing propagation delay time.
13. Master slave flip flop s used to eliminate the race around condition J – K flip flop by increasing propagation delay time.
14. Race around condition can be eliminated by edge triggering.
15. Master slave is a cascading of 2 J – K flip flops
16. If a j – K flip flop is modified by the addition of an inverter so that K is the complement of J, the flip flop is called a D (delay) flip flop.

D	Qn + 1
0	0
1	1



17. D flip flop provides one clock pulse delay.
18. T flip flop can be constructed by shorting J and K inputs of J – K flip flop. It acts as a toggle switch.

D	Qn + 1
0	Qn
1	$\overline{Q}$n



19. D flip flop can be converted into T using Ex OR gate and vice versa.
20. N flip flop can store n bits referred to as a register.
21. Toggle flip flop is used in binary counting
22. Toggle flip flop is also suffered from race around condition.
23. Advantage of edge trigging is two successive events can be carried out in a single clock pulse.
24. Application of shift registers :
    (a) serial to parallel conversion
    (b) serial to serial conversion
    (c) parallel in, serial out
    (d) Parallel in, parallel out
    (e) right shift, left shift
    (f) sequence generator
25. Only preset is sufficient, clock is not required for parallel out data where as clock is required for serial out.
26. Ripple counter is a asynchronous counter.
27. Synchronous counter have same clock pulse for all flip flops.
28. For asynchronous counter different clock pulses for different flip flops.
29. Synchronous counter are faster than asynchronous counter.
30. A counter which can be made to counter in either the forward or reverse direction is calledan up down counter.
31. N bit shift register ring counter is a divided by 'n' unit scalar.
32. N bit twisted ring counter is a $2^n : 1$ scalar
33. Twisted ring counter is a $2^n : 1$ scalar
34. The no. of flip flops (n) required to constant MOD 'N' can be obtained from the formula
    $$2^{n-1} < N \leq 2^n$$
35. A decade counter requires 4 flip flops.
36. Parallel carry type counters are faster than serial carry type.
37. The main disadvantage of parallel carry synchronous counters is larger fan in of the gates.
38. Application of counters :
    (i) Measurement of frequency
    (ii) Measurement of time
    (iii) Measurement of distance
    (iv) In digital clocks.
39. A decade counter is mod 10 ripple counter.
40. Shift left operation multiplice a binary number by 2 and a shift right operation divides a binary number by 2.
41. A counter divides the clock frequency by its modules.
42. A ring counter is a shift left register with its output fed back to input.

MEMORIES

1. Static storage device is one in which the information does not change position.
   Ex : flip flop, register, magnetic tape.
2. A dynamic storage device is one in which the information stored is continually changing position.
   Ex : CCD.

3. Memories are used in digital systems to store information such as instructions, data & results.
4. A memory is said to be volatile if the contents of memory get erased as soon as the power goes off. Ex : RAM
5. A memory is said to be non volatile if the contents of memory are not effected by power failure.
   Ex : ROM, PROM, EPROM, EAROM
6. RAM – Random Access Memory
7. ROM – Read only memory
8. PROM – Programmable Read Only Memory.
9. EPROM – Erasable programmable read only memory.
10. EEPROM – Electrically Erasable programmable Read only memory.
11. EAPROM – Electrically alterable programmable read only memory.
12. Dynamic RAMS require refreshing.
13. Secondary memories are slower than main memories.
14. Static MOS memories are slower than the bipolar memories.
15. MOS memories consumes less power than bipolar memories
16. RAM is both read and write memory.
17. A memory with 'n' address lines an dm data lines has a memory capacity of $2^n \times m$ bits.
18. A memory has staring address 4000 and final address 7FFF. The no of location in it is.
    7FFF – 4000 + 1 = 3 FFF + 1 = 4000
19. In EPROM the data can be erased by ultra violet light.
20. PROM is a ready only memory that can be programmed only once.
21. A memory of size M × N bits can store n words of n bits each.
22. EPROM is fabricated using MOS technology.

A/D, D/A CONVERTERS

1. A digital to analog converter (DAC) converts digital signal into corresponding analog signal.
2. An analog to digital converter converts analog voltages in to corresponding digital code.
3. A/D, D/A converter are used in digital communication and Digital modulation.
4. Heart of D/A converter is op amp. It acts as summer in D/A converter.
5. Resolution is the ratio of ILSB increment to the maximum output of a D/A converter.
6. Resolution = $1/2^n - 1$ where n is the input bits.
7. Resolution volts = $V/2^n - 1$ where V is the maximum voltage.
8. The accuracy of a converter is a measure of the difference between the actual analog output voltage and what the output should be in the ideal case.
9. There are two types of D/A converter.
   (i) weighted register D/A
   (ii) R – 2R ladder D/A
10. D/A converter is usually considered as a decoder.
11. A/D converter is usually considered as a encoder
12. The advantage of R – 2R ladder circuit over weight register D/A is (I) better linearity (II) only two values of resistance are needed.
13. Monotonicity means checking that the output voltage increases regularly as the input digital increases.
14. Flash type is the fastest A/D converter.
15. A/D converts are :
    (i) Counter type

(ii) Continuous conversion
(iii) Ramp type (or) single slope conversion type
(iv) Successive aproximation type (SAR)
(v) Dual slope integration type
(vi) Simultaneous (or) parallel compalation type (or) flash converter

16. Counter type A/D converter require $2^n - 1$ clock pulses for n bit conversion.
17. SAR type the conversion time required in A/D converter is n clock pulses for n bit conversion.
18. SAR takes uniform conversion.
19. Ram p type is a slower type converter.
20. Dual slope integration type have high conversion time. It require 2^{N-1} clock pulse for N bit convert.
21. Dual slope integration type have highest accuracy. Hence it is more accurate.
22. Parallel comparation (or) flash converter require $2^n - 1$ comparators for n bit conversion.
23. A ring counter is used in successive application conversion.

OBJECTIVE TYPE QUESTIONS

NUMBER SYSTEM EXERCISE :

1. The radix for binary system is
   a) 0 b) 1 c) 2 d) 10
2. The radix (base) for Hexadecimal system is
   a) 1 b) 16 c) 6 d) 8
3. Binary equivalent of $(64)_{10}$ is
   a) 1000 b) 100000
   c) 101010 d) 1000000
4. Decimal equivalent of Binary number 10101 is
   a) 21 b) 13 c) 19 d) 23
5. Octal equivalent of decimal number 15.5 is
   a) 20.2 b) 17.4 c) 16.3 d) 20.4
6. A group of 8 bits is known as
   a) A nibble b) A byte c) A bit d) Quad
7. Two's complement of the binary number 10010100 is
   a) 10011010 b) 10101100
   c) 11011000 d) 01101100
8. $(121)_x = 100_8$; x =
   a) 5 b) 6 c) 7 d) 9
9. If the number is negative the left most bit is
   a) 1 b) 0 c) 4 d) 3
10. The 2's complement of 1010 is
    a) 1010 b) 1011 c) 0110 d) none
11. Which code is self complement code
    a) Gray code b) ASCII code
    c) BCD code d) Excess 3 code
12. In which code only one bit differ in successive numbers
    a) Gray code b) BCD code
    c) 2421 code d) EBCDI code
13. Gray equivalent of binary number 1101 is
    a) 1010 b) 1011 c) 1110 d) 1101
14. Binary equivalent of gray code 101011 is
    a) 110010 b) 111010
    c) 101011 d) none
15. In the following which is even parity
    a) 101100 b) 100011
    c) 101011 d) 0101100
16. Decimal equivalent of FA. CE
    a) 250.78 b) 220.3
    c) 270.5 d) 260.45
17. What is the octal equivalent of decimal 0.6 ?
    a) 0.46314631 b) 0.2327272
    c) 0.3333333 d) 0.46464646

18. The maximum positive and negative numbers which can be represented in two complement form using n bits are respectively
a) + (2^{n-1}), $-(2^{n-1}-1)$ b) + $(2^{n-1}-1)$, 2^{n-1}
c) + 1^{n-1}, -2^{n-1} d) + 1^{n-1}, $-(2^{n-1}+1)$

19. Following which is alphanumeric code
a) Excess 3 code b) ASCII code
c) EBCDIC d) none

20. The minimum number of bits required to represent positive numbers in the range 1 to 31 using 2s complement representation is
a) 5 b) 6 c) 8 d) 10

21. The code used in computer cards is
a) Gray code b) natural BCD code
c) 12 bit Helloreth code d) ASCII code

22. Excess 3 code (XS3 code) for 9 is
a) 1001 b) 1010 c) 1110 d) 1100

23. The number 7 expressed in 2421 code
a) 0100 b) 1010 c) 1100 d) 1101

24. Two's complement of –6 is
a) 1100 b) 1011 c) 1010 d) 1001

25. 1's complement of +5 is
a) 1010 b) 1011 c) 1101 d) 1111

26. The hexadecimal equivalent of the binary number 11101101111010 is
a) EDE8 b) 65572 c) FB7A d) 3B7A

27. To detect one bit error in digital systems we use
a) Gray code b) Excess 3 code
c) Parity Bit d) Hallirath code

28. Following which is unweighted code
a) Gray code b) BCD code
c) 8421 code d) ASCII code

29. One's complement of a binary number can be found by
a) changing all zero's to ones
b) changing all ones to zero
c) changing all ones to zeros and all zeros to ones
d) none of these

BOOLEAN ALGEBRA & LOGIC GATES :

1. In Boolean Algebra A+A+A+A+....+A is the same as
a) nA b) A^n c) zero d) A

2. In Boolean algebra 1+A+B+C is equal to
a) A b) 1 c) 1 + A d) 1 + 3A

3. The Boolean expression for AND Gate is
a) A + B = Y b) A.B = Y
c) A = B d) A – B = Y

4. A – B is the Boolean expression for
a) XNOR b) XOR
c) AND Gate d) NOR Gate

5. The output of a gate is low when atleast one of its input is low. It is true for
a) AND b) OR c) NAND d) NOR

6. The output of a 2 input gate is 1 if and only if its inputs are zero. It is true for
a) OR b) EXOR
c) EXNOR d) NOR

7. The output of a 2 input gate is 1 if and only if its inputs are equal. It is true for
a) EXOR b) AND
c) NAND d) EXNOR

8. The most suitable gate for comparing two bits is
a) AND b) OR c) EX-OR d) OR

9. The output of a gate is High when atleast one of its input is low it is true for
a) EXOR b) NAND
c) NOR d) OR

10. The output of a gate is low if and only if all its inputs are High it is true for
a) EX-OR b) NAND
c) NOR d) OR

11. The output of a gate 1 if and only if its input are unequal. It is true for
a) OR b) EX-OR
c) EX-NOR d) NOR

12. The output of a 2 input gate is '0' if and only if its inputs are unequal. It is true for
a) EX-NOR b) AND
c) NAND d) NOR

13. A gate is disabled when its disable input is at logic 0. The gate is
a) AND b) NOR
c) OR d) None of these

14. Of the following which are the universal gates
a) NAND, NOT b) NOR, NAND
c) NOR. OR d) NAND, AND

15. $\overline{A.B.C}$ is equal to
a) $\overline{A} + \overline{B} + \overline{C}$ b) $\overline{A.B.C}$
c) A + b + C d) A. B. C

16. A gate is enabled when its inhibit input is at logic. The gate is
a) OR b) NAND c) NOR d) None

17. The dual of a Boolean theorem is obtained by
a) interchanging all 0's and one's only
b) changing all 1's to zeros only
c) interchanging all 0's and 1's and + and. Signs.
d) changing all 0's to one's only

18. Dual of A + BC is
a) A(B+C) b) AB + BC
c) A + (B + C) d) AC + B

19. To check the parity of a digital word, it is preferable to use
a) NOR Gate b) NAND gate
c) EX-OR gate d) OR gate

20. The simplification $XY + YZ + \overline{Y}Z$
a) XY + Z b) X + Y + Z
c) XZ + Y d) XY + YZ

21. Positive logic AND is equivalent to
a) Positive NAND b) Negative OR
c) Negative NOR d) Positive NOR

22. X + 0 = X is the dual of
a) X . X = X b) X . 0 = X
c) X . 1 = X d) X = X

23. In sum of product form (SOP) each individual term is called as
a) Max. term b) Bit
c) Quad d) Min. term

24. To simplify more than 6 variable preferable method as
a) Boolean algebra method
b) Karnaush – map method
c) Tabulation method
d) None of these

25. The minimum no. of NAND Gates required to implement EX-OR gate is
a) 1 b) 3 c) 4 d) 5

26. In product of sum form (POS) each individual term is called as
a) max. term b) min. term
c) byte d) octet

27. Minimum no. of NOR gates required to implement EX-NOR gate is
a) 1 b) 2 c) 4 d) 5

28. Bubbled OR gate is equivalent to
a) NOR b) NAND
c) AND d) EX-OR

29. AND – NOR is equivalent to
a) OR b) NAND – AND
c) AND d) NAND

30. NAND Gates are pre-tested than other gates because they have
a) high power consumption
b) low noise
c) low power consumption
d) low cost

31. 7432 is a
a) Quad 2 input OR gate
b) Quad 2 input AND gate
c) Quad 2 input NAND gate
d) Quad 2 input NOR gate

32. Which is identical to the action of two series switches
a) AND b) NAND c) NOR d) OR

33. An OR Gate has 6 inputs. How many input words are there on its truth table ?
a) 6 b) 36 c) 64 d) 64,000,000

34. In a karnaga map a quad eliminates how many variables ?
a) Two b) Three c) Four d) 1

35. Positive logic in a logic circuit is one in which
a) logic 0 and 1 are represent in +ve voltage respectively
b) logic 0 and 1 are represent in –ve and +ve voltage respectively
c) logic 0 voltage level is higher than logic 1 voltage level
d) logic 0 voltage level is higher than logic 1 voltage level

36. The Boolean expression $Y = \overline{AB} + \overline{AC} + BC$ when simplified becomes
a) $\overline{A}$ b) B c) $\overline{B}$ d) $\overline{C}$

37. A NAND logic with +ve logic acts as
a) NOR Gate with +ve logic
b) AND Gate with +ve logic
c) OR with –ve logic
d) AND with –ve logic

38. Minimum no. of NOR Gates required to implement EX-OR Gate is
a) 3 b) 4 c) 5 d) 6

39. The minimum no. of pins required in an IC with two 4 inputs gates is
a) 12 b) 14 c) 16 d) 18

40. The disabled input to the NAND gate is
a) 0 b) 1
c) Both 0 & 1 d) None

41. The SOP form of logical expression is most suitable for designing logic circuit using only
a) NOR Gates b) NAND Gates
c) AND Gates d) EX-OR Gates

42. The POS form of logical expression is most suitable for designs logic circuits using only
a) EX-OR Gates b) AND Gates
c) NAND Gates d) NOR Gates

43. The code used for labelling the cells of k - map is
a) Natural BCD b) Hexadecimal
c) Gray Code d) Octal

44. The max term corresponding to decimal number 15 is
a) ABCD b) $\overline{ABCD}$
c) A+B+C+D d) $\overline{A}+\overline{B}+\overline{C}+\overline{D}$

45. The min term corresponds to the decimal number 13 is
a) A+B+C+D b) ABCD
c) $\overline{ABCD}$ d) $\overline{A}+\overline{B}+\overline{C}+\overline{D}$

LOGIC FAMILIES

1. The basic gate of RTL family is
a) NAND b) AND
c) NOR d) OR

2. NPN transistors are preserred over p-n-p transistor for digital circuits because
a) then require +ve power supply
b) then consume less power
c) of the requirement of positive logic system
d) the mobility of electrons is higher than the mobility of holes hence speed of operation is high

3. In general the proposation delay time of MOS devices
a) Is of the same order as bipolar devices
b) Is less than those of bipolar devices
c) Is more than those of bipolar devices
d) May be more or less than those of bipolar devices

4. The logic family with highest noise margin is
a) TTL b) DTL c) HTL d) CMOS

5. A schottky transistor when used as a switch, switches between
a) cutoff and between
b) cutoff and active region
c) active and satulation region
d) inactive region

6. The speed at whichschottky TTL can be operate is
a) lower than that of standard TTL
b) higher than that of standard TTL
c) same as that of standard TTL
d) none of the above

7. The figure of merit of a logic family is given by
a) Gain x band width
b) Propagation delay time x power dissipation
c) Tanout x propagation
d) Noise margin x power dissipation

8. Following which is non saturated bipolar logic
a) DTL b) TTL c) HTL d) ECL

9. TTL circuits with active pull up are preferred because of their suitability for
a) wired AND operation
b) bus operated system
c) less power dissipation and higher speed of operation
d) higher noise margin

10. Tristate logic has
a) three output states : 0,1 and high impedance
b) only two output states 0 and 1
c) only high output impedance
d) logic 0 output when tristated

11. CMOS logic circuit consists of
a) only p channel MOS devices
b) MOS devices and capacitors
c) Only n channel MOS devices
d) both p channel and n channel devices

12. In ECL negative power supply issued because of
a) increase in speed of operation
b) reduction in noise at the output
c) saving in power
d) low noise immunity

13. MOS devices are used for VLSI because of
a) their higher noise immunity
b) availability of n channel and p channel devices
c) lower silicon chip area required
d) higher speed of operation

14. The logic family with highest speed (or lowest propagation delay time) is

a) CMOS b) NMOS c) TTL d) ECL

15. The logic family which has minimum power dissipation than all other families is
a) DTL b) TTL c) ECL d) CMOS

16. Complementary out puts are available in
a) ECL b) HTL c) DTL d) CMOS

17. Tristate logic is used for
a) increasing the fan out
b) improving figure of merit
c) improving figure of merit
d) bus oriented system

18. The most popular logic family for SSI and MSI digital ICs is
a) TTL b) DTL c) CMOS d) ECL

19. The logic family which has highest fan out
a) DTL b) TTL c) CMOS d) HTL

20. MOS families have speed of operation
a) higher than Bipolar
b) slower than Bipolar
c) same as Bipolar d) none

21. HTL is a modified form of
a) TTL b) DTL c) ECL d) CMOS

22. For higher fan out
a) the output impedance is high
b) high input impedance
c) the output impedance is low at both logic 0 and logic 1 level
d) the output impedance is low at both logic 0 level and low at logic 1 level

23. In which logic family current mode logic issued
a) DTL b) TTL c) HTL d) ECL

24. For standard TTL the fan out is
a) 10 b) 6 c) 50 d) 20

25. Which logic family is the resistor free
a) DTl b) HTL c) ECL d) CMOS

26. Basic gate in CMOS is
a) NAND b) NOR c) NOT d) EX.OR

27. The standard propataiton delay time of TTL IC's is
a) 10ns b) 10s c) 10ms d) 6ms

28. Which logic family has high noise immunity
a) DTL b) TTL c) HTL d) ECL

29. Which logic family is best useful in industrial environment
a) DTL b) TTL c) CMOS d) HTL

30. The basis gate in TTL CC families is
a) NOT b) AND c) NAND d) NOR

COMBINATIONAL LOGIC CIRCUITS :

1. In a combinational circuit the output at any time depends on
a) only on the past inputs
b) only on the past outputs
c) only on the input present at that instant of time
d) on past inputs and as well as present inputs

2. A combinational circuit
a) never contains memory elements
b) always contains memory elements
c) may sometimes contains memory elements d) none

3. The gates required to build a half adder are
a) 1 EXOR gate and 1 OR gate
b) 1 EXOR gate and a NOR gate
c) 4 NAND gates
d) 1 EXOR gate and a AND gate

4. In a half adder if the two inputs are '1' then
a) sum is 1, carry is 1
b) sum is 1, carry is 0
c) sum is 0, carry is 1
d) sum is 0, carry is 0

5. A logic circuit that can adds three bits at a time is known as a
a) full adder b) half adder
c) ALU d) CPU

6. A logic circuit that adds two binary numbers is known as
a) full adder b) half adder

c) binary adder
d)arithmetic logic unit

7. To add two four bit binary words at a time we need ——— full adders ——— half adders
a) 2,1 b) 1,3 c) 3,4 4) 4,3

8. The ALU performs ——— operations
a) brancing b) loop
c) arithmetic and logic d) all of these

9. To construct a full adder we require
a) two half adder, and 1 EX-OR gate
b) two half adder and 1 OR gate
c) 3 half adder and 1 OR gate
d) 3 half adder and 1 AND gate

10. For n bit serial adder we require full adder
a) 1 b) 2 c) n d) n – 1

11. For n bit serial adder operation we require
a) 1 clock pulse b) n clock pulse
c) n + 1 clock pulse d) none

12. For n bit parallel adder we require
a) n full adder, 1 half adder
b) 1 full adder
c) n – 1 full adder , 1 half adder
d) n half adder

13. For 4 bit parallel adder we require
a) 1 clock pulse b) two clock pulse
c) 4 clock pulse d) 5 clock pulse

14. Serial adder is
a) slower than parallel adder
b) faster than parallel adder
c) same speed with parallel adder
d) none of the above

15. For a half substractor we require
a) 2 EX OR and 1 AND gate
b) 1 EX OR, 1 OR, 1 NOT gate
c) 1 NAND, 1 OR, 1 NOT gate
d) 1 EX OR , 1 AND, 1 NOT gate

16. For full subtractor we require
a) two half subtracter and one AND gate
b) Two half subtracter and one OR gate
c) Two half subtracter and one NAND gate
d) Two half subtracter and two OR gates

17. Universal logic circuit is
a) multiplexer b) demultiplexer
c) full adder d) encoder

18. Multiplexer is a logic circuit it gives
a) several inputs several ouputs
b) one input several outputs
c) one input one output
d) several inputs one output

19. Demultiplexer is a logic ckt that
a) it accept one input and distributes it over several outputs
b) it accept one input and distributes it over one input
c) it accept several input and one output d) none

20. In digital systems subtraction is performed
a) using half adder
b) using half subtractors
c) using adders with one's complement representation & negative number
d) None

21. Full adder consists of
a) 3 AND gates 2 OR gates
b) 3 AND gates 1 OR gate 1 EXOR gate
c) 3 AND gates 1 OR gate
d) 3 AND gates 1 EXOR gate

22. To compare magnitude of bits were
a) EXOR gate b) NOR gate
c) NAND gate d) AND gate

23. Decoder converts
a) decimal to binary
b) decimal to octal
c) octal to binary
d) binary to decimal number

24. Encoder converts
a) binary to octal
b) binary to decimal
c) decimal to binary d) none

25. Which is called as data selector
a) multiplexer b) decoder

c) demultiplexer d) encoder

26. Which is called as Data distributor
a) multiplexer b) decoder
c) demultiplexer d) encoder

27. Sum output of an half adder is obtained using
a) AND gate b) EXOR gate
c) NOR D) NAND

28. Binary multiplication is done using
a) two 's complement
b) one's complement
c) shift and add
d) successive subtraction

29. To multiply a binary number by 32, it is enough if the number is shifted to the left by ———— places
a) 2 b) 3 c) 4 d) 5

30. Binary division can be down using
a) shift and add
b) successive subtraction
c) two ' s complement
d) addition

SEQUENTIAL LOGIC CIRCUITS :

1. In a sequential circuit the output at any instant of time depend
a) only on the inputs present at that instant of time
b) only on the past outputs
c) on the past outputs and the inputs present at that instant of time
d) only on the past inputs

2. The basic memory element in a digital circuit
a) consists of NAND gate
b) consists of a NOR gate
c) is a flip-flop
d) is a shift register

3. A flip-flop has two out puts which are
a) always zero b) always one
c) always complementary
d) in one of the above states

4. A flip-flop is used to store
a) one bit of information
b) two bits of information
c) one nibble of information
d) one byte of information

5. In S-R flip-flop, forbiddion occur at
a) S = 1 : R = 0 b) S = R = 0
c) S = 0 , R = 1 d) S = R = 1

6. When J = K = 1 then the output of j=K flip-flop is
a) Qn b) Qn+1
c) toggle d) forbidden

7. Race around condition occur in J-K flip-flop due to
a) the clock time period less than propagation delay time
b) the clock time period greater than propagation delay time
c) due to triggering d) none

8. Master slave flip-flop is used to
a) increase its clocking rate
b) reduce race around condition
c) eliminate race around condition
d) improve its reliability

9. Flip-flops can be used to make
a) latches b)Bounce elimination witches
c) registers d) All of these

10. D flip –flop may be constructed by the addition of _____ to the J-K flip
a) an inverter b) an AND gate
c) OR gate d) EXOR gate

11. A J-K master slave flip-flop can be converted in to T flip-flop by making
a) J=k b) K = J c) CIK = 0 d) None

12. T flip-flop can be converted into during a
a) OR b) AND c) EX-OR d) NOT

13. The main difference between the RS flip-flop and D flip-flop
a) D flip-flop does not require clock
b) D flip-flop has two inputs
c) D flip-flop has only one input
d) None

14. A twisted ring counter (Johnson counter) consists of five flip-flop will have
    a) 6 states b) 12 states
    c) 10 states d) 16 states
15. A normal ring counter having five flip-flops will have
    a) 5 states b) 10 states
    b) 32 states d) infinite states
16. The maximum possible number of states in a ripple counter consisting of four flip-flop is
    a) 4 b) 8 c) 10 d) 16
17. The number of flip-flops in a decode counter is
    a) 2 b) 8 c) 10 d) 16
18. Ripple counter is a
    a) syncronous counter
    b) asyncronous counter
    c) both (a) and (b) d) none
19. For a syncronous counter
    a) clock pulses are same for each flip-flop
    b) different clock pulse for different flip-flops
    c) both (a) and (b) d) none
20. In mod K counter the no.of flip-flops required are
    a) $K > 2^N$ b) $K < 2^{N-1}$
    c) $2^N > K > 2^{N-1}$ d) None
21. Parallel carry type synchronous counter are
    a) faster than serial carry
    b) slower than serial carry
    c) have same speed d) none
22. In a Johnson counter the input to a first flip-flop as
    a) output of second flip-flop
    b) output of first flip-flop
    c) $\overline{Q}$ of last flip-flop
    d) Q of last flip-flop
23. For n bit register _____ flip-flops are required
    a) 2^n b) n c) 2^{n-1} d) n –1
24. A shift left operation
    a) divide the binary number by 2
    b) add-2 to the binary number
    c) multiply the binary number by 2
    d) subtract 2 from the binary number
25. The maximum count of a counter is given by
    a) n b) 2^{n-1} c) n –1 d) $2^n - 1$
26. Decade counter divides the input clock free at o/p is
    a) by 5 b) by 10 c) by 2 d) by 16
27. Synchronous counter are
    a) faster than asynchronous counter (ripple counter)
    b) slower than ripple counter
    c) have same speed of operation with ripple counter d) none
28. Preset and clear are known as
    a) synchronous inputs
    b) control inputs
    c) asynchronous inputs d) none
29. A counter is a register capable of counting
    a) bits b) bytes
    c) clock pulses d) words
30. A mod 32 counter needs _____ flip-flop
    a) 2 b) 3 c) 4 d) 5
31. If the input frequency to a decade counter is 1000 Hz. The output frequency is
    a) 50Hz b) 100Hz c) 200Hz d) 300Hz
32. A shift right operation
    a) divide the binary number by 2
    b) multiply binary number by 2
    c) add 2 to the binary number
    d) subtract 2 from binary number
33. When the output of one flip-flop drives another then the counter is called as
    a) ring counter b) ripple counter
    c) decade counter
    d) synchronous counter

MEMORIES :

1. In a micro processor the program stored in
   a) RAM b) ROM
   c) Bistable Latch d) none
2. Memories are used in digital system to store
   a) instructions b) data
   c) intermediate and final results
   d) all of the above
3. A shift register is a
   a) random access memory
   b) sequentially accessed memory
   c) read only memory
   d) content addressable memory
4. A memory in which the contents get erased when power failure occurs is
   a) RAM b) EAROM
   c) PROM d) ROM
5. A static RAM is fabricated using
   a) only bipolar technology
   b) only the mos technology
   c) either bipolar or mos technology
   d) none
6. A PROM
   a) masic programmed
   b) is erasable by UV radiation
   c) can be programmed only once
   d) can be programmed any no. of times
7. An EPROM
   a) non erasable b) volatile
   c) programmable and erasable
   d) erasable but not programmable
8. Read and write memories is same as
   a) ROM b) PROM
   c) EAROM d) RAM
9. A memory has 16 bit address bus. The number of locations in this memory are
   a) 16 b) 32 c) 1024 d) 65536
10. A memory in which the present contents must be erased before new information can be stored is
    a) ROM b) PROM
    c) EAROM d) RAM
11. A dynamic RAM can be fabricated using
    a) mos technology b) TTL
    b) ECL d) bipolar
12. In the following the volative memory is
    a) ROM b) EPROM
    c) RAM d) EAROM
13. Which memories are periodically refreshing
    a) ROM b) dynamic RAM
    c) static RAM d) PROM
14. Secondary memories are
    a) slower than main memories
    b) faster than main memories
    c) have same speed with main memory
    d) none
15. Which memories consume less power
    a) bipolar b) mos memories
    c) both d) none
16. Bipolar memories are
    a) faster than static mos memories
    b) slower than mos memories
    c) have same speed d) none
17. A memory with n address lines has _____ locations
    a) 2^{n-1} b) n c) $2^n + 1$ d) 2^n
18. A memory with n address lines and m date lines has a memory capacity of _____ bits
    a) 2^n b) $n \times m$ c) $2^n \times m$ d) m
19. The memory capacity of a chip with 12 address lines and 8 date lines is
    a) 2KB b) 4KB c) 8KB d) 12 KB
20. Memory unit which uses only combinational logic gates in its simplification
    a) ROM b) RAM c) Core d) Disc
21. Which of the following got equal access time for all locations of the memory

a) floppy disk b) RAM
c) hard disk d) Rom

22. Which of the following issued for storing variable quantitive
a) EPROM b) ROM c) PROM d) RAM

23. The time required to locate and read a word for memory is
a) read cycle time
b) write release time
c) access time
d) data hold time

24. EPROM
a) ultra voilet light erasable and electrically programmable
b) infrared light erasable and magnetically programmable
c) electrostatically erasable and magnetically programmable
d) magnetically erasable and electrically programmable

25. On detection of an error, a part of the memory can be erased in
a) EPROM b) PROM
c) EROM d) EAROM

A/D, D/A CONVERTERS:

1. A D/A converter (DAC) converts
a) analog signal into digital
b) binary to octal
c) digital signal into corresponding analog signal
d) octal to hexa decimal

2. D/A converter usually considered as
a) encoder b) decoder
c) multiplier d) adder

3. Resolution is defined as the ratio of
a) LSB to maximum output
b) MSB to LSB
c) LSB to MSB–1 d) None

4. In weighted registers D/S convertion operational amplified used as
a) integrator b) differentiator
c) multiplier d) summer

5. Disadvantage of weighted register D/A converter are
a) low accuracy, large register values
b) high accuracy, large register values
c) high accuracy, low register values
d) low accuracy, low register values

6. The advantage of R-2R ladder is
a) only one value of register value is used
b) only two value of register value is used
c) only 4 values of register value used
d) only 5 values of register values are used

7. For n bit DIA converter the resolution is given by
a) 2^{n-1} b) $2^n - 1$ c) $n - 1$ d) $1/2^{n-1}$

8. An A/D converter (ADC) converts
a) digital to analog
b) analog to digital
c) binary to BCD d) none

9. In an R-2R adder D/A converter, the input resistance is
a) not same for all digital inputs
b) R for each input
c) 2R for each input
d) 3R for each input

10. The A/D converter which has the highest speed of conversion is
a) dual slop A/D converter
b) successive approximation A/D converter
c) flash type A/D converter
d) ramp type A/D converter

11. An A/D converter having an analog range of –5v to +5v and 8 bit digital output has resolution of
a) 20 volts b) 40 volts
c) 20mv d) 40mv

12. In successive approximation ADC _____ counter is used

a) ripple counter b) mod 10 counter
c) ring counter d) none

13. The maximum no.of clock pulses required for conversion using N bit counter type ADC is
a) 2^N b) 2^{N-1} c) N d) N – 1

14. The maximum no.of clock pulses required for N bit conversion in successive approximation ADC is
a) 2^N b) N c) 2^{N-1} d) N – 1

15. The max. no. of clock pulsed required for N bit flash type (parallel comparator)
a) 2^N b) N c) 1 d) 0

16. The max. no. of clock pulses required for N bit dual slope ADC is
a) 2^N b) 2^{N+} c) 2^{N+1} d) 1

17. _____ ADC is more accurate
a) dual slope
b) successive approximation
c) flash type d) potentiometric

18. Disadvantage of parallel comparator (or) flash type DAC is
a) need of higher clock pulse
b) need of high power supply
c) low accuracy
d) need of more comparators

19. In flash type DAC no.of comparators required for n bit conversion is
a) n b) n – 1 c) 2^{n-1} d) $2^n - 1$

20. The minimum number of resistors required in 4 bit D/A network of weighted register type is
a) 4 b) 8 c) 15 d) 16

ANSWERS

NUMBER SYSTEM :

1)c 2) b 3) d 4) a 5) b 6) b
7)d 8) c 9) a 10) c 11) d 12) a
13) b 14) a 15) c 16) a 17) a 18) b
19) b 20) b 21) c 22) d 23) d 24) c
25) a 26) d 27) c 28) a 29) c

BOOLEAN ALGEBRA & LOGIC GATES :

1). d 2). b 3). b 4). d 5). a 6). d
7). d 8). c 9). b 10). b 11). b 12) a
13) a 14) . b 15). a 16). a 17). c
18). a 19). c 20). a 21). b 22). c
23). d 24). c 25). c 26). a 27). c
28). b 29). b 30). c 31). a 32). a
33). c 34). a 35). c 36). d 37). a
38). c 39). b 40). a 41). b 42). d
43). c 44). d 45). b

LOGIC FAMILIES :

1). c 2). d 3). c 4). c 5). b 6). b
7). b 8). d 9). c 10). a 11). d 2). b
13). c 14) . d 15). d 16). a 17). d
18). a 19). c 20). b 21). b 22). c
23). d 24). a 25). d 26). a 27). a
28). c 29). d 30). c

COMBINATIONAL CIRCUITS :

1). c 2). a 3). d 4). c 5). a 6). d
7). a 8). c 9). b 10). a 11). c 12). c
13). a 14) . a 15). d 16). b 17). d
18). d 19). a 20). c 21). b 22). a
23). d 24). c 25). a 26). c 27). b
28). c 29). d 30). b

SEQUENTIAL LOGIC CIRCUITS :

1). c 2). c 3). c 4). a 5). d 6). c
7). b 8). c 9). d 10). a 11). c 12) c
13). c 14) . c 15). b 16). d 17). c 18) b

19). b 20). c 21). a 22). c 23). b 24) c
25). d 26). b 27) a 28). c 29). c
30). d 31). b 32). a 33). b

MEMORIES :

1). a 2). d 3). b 4). a 5). c 6). c
7). c 8). d 9). d 10). c 11). a 12) c
13). b 14). a 15). b 16). a 17). d
18). c 19). b 20). a 21). a 22). a
23). c 24). a 25). d

A/D, D/A CONVERTERS :

1). c 2). b 3). a 4). d 5). a 6). b
7). d 8). b 9). d 10). c 11). d 12) c
13). a 14). b 15). c 16). c 17). a
18) d 19).d 20).a