

## MICROPROCESSOR

1. A computer designed using the micro processor is called a micro computer. It includes memory, input, output, microprocessor .
2. A CPU built into a single LSI or VLSI chip is called a micro processor.
3. The term LSI (Large Scale Integration) refers to IC's containing components usually transistors, in the range of 1000 to 10,000.
4. Instructions and Data fed to the CPU of a digital computer must be in terms of 0s and 1s.
  - a]A binary digit is known as a bit.
  - b]A group of 8-bits is called a byte.
  - c]A group of 4-bits is called Nibble.
5. Each computer has a fixed set of instructions in the form of binary patterns called a machine language.
6. The binary instructions are given, abbreviated names, called mnemonic's, which form the assembly language. Mnemonic is a combination of letters to suggest the operation of an instruction.
7. The number of bits that a digital computer can process in parallel at a time is called its word length. It is a measure of computing power of a computer. A 4-bit micro computer has a word-length of 4 bits.
8. Most of 8-bit microprocessors use LSI technology and clock frequency lies in the range of 1 MHz to 6 MHz.
9. 16-bit microprocessors have more powerful instructions set than that of 8-bit microprocessors.  
They use VLSI technology. These are designed to work in multiprocessor environment and use high-level languages.
10. Low level language: A medium of communication that is machine dependent or specific to a given computer. The machine and the assembly language of a computer are considered low-level languages. Programs written in these languages are not transferable to different types of machines.
11. High level language : A medium of communication that is independent of a given computer.  
Programs are written in English-like words, and they can be executed on a machine using a translator (compiler or Interpreter).
12. Compiler : A program that translates English -like words of a high level language into the machine language of a computer. A compiler reads a given program, called a source code, in its entirety and then translates the program into the machine language, which is called

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an object code.

**13. Interpreter :** A program that translates the English-like statements of a high-level language into the machine language of a computer. An interpreter translates one statement at a time from source code to an object code.

**14. Assembler :** A computer program that translates an assembly language program from mnemonics to the binary machine code of a computer.

**15.** The first microprocessor was introduced in 1971 by Intel Corporation, U.S.A. It was a micro processor, the Intel 4004.

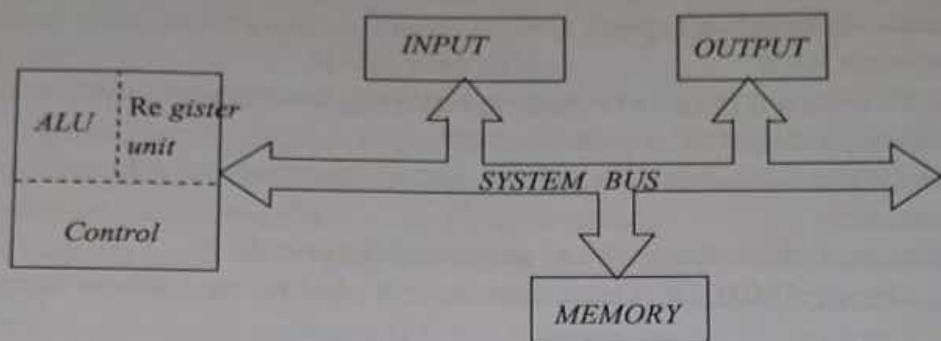
**16.** The Intel 4004 and 8008 both used PMOS technology. Intel 8080 use NMOS technology.

Micropocessor Remarks	Year of Introducing	Word length	Memory addressing capacity	Pins	Clock
4004	1971	4-bit	1KB	16	750KHz First Micro processor
8008	1972	8-bit	16KB	18	800KHz First 8-bit Microprocessor
8085	1976	8-bit	64KB	40	3-6MHz Popular, widely used
8086	1978	16-bit	1MB	40	5-10MHz First 16-bit μP
80386DX	1985	32-bit	4GB real, 64TB virtual	132	20-33MHz First 32-bit
i860	1989	64-bit	4GB	168	40MHz 64-bit RISC Processor
68000	1979	16/32-bit	16MB	64	10-25MHz Popular & widely used

**GENERATION OF DIGITAL COMPUTER**

1. The digital computers using electronic valves are known as first generation computers.
2. The digital computers using transistors instead of electronic valves as CPU components are known as second generation computers.
3. Third generation uses IC's instead of transistors.
4. Computers employing microprocessors are fourth generation computers.
5. Fifth generation computers are in research and development stage.
6. **Applications of Microprocessors:** Industry, instrumentation, transportation, military equipment like tanks, radars etc., banks, business organizations, communication, automatic control of generators voltage, fuel control of furnaces, consumers and commercial applications etc.,

**BLOCK DIAGRAM OF A MICRO COMPUTER**



1. The physical devices and circuitry of a computer are called hardware.
2. A sequence of instructions to perform a particular task is called program.
3. The microprocessor is a semiconductor device consisting of electronic logic circuits manufactured by using either a Large Scale Integration [LSI] or Very Large Scale Integration [VLSI]. It is divided into 3 segments:
  - a] Arithmetic /Logic unit [ALU]
  - b] Register unit
  - c] Control unit
4. Arithmetic Logic unit [ALU]: The function of ALU is to perform arithmetic operations such as addition, subtraction, and logical operations such as AND, OR and EXCLUSIVE OR.
5. Timing and control unit : This unit controls the entire operations of a computer. It generates timing signals necessary for input and output devices.
6. Accumulator and general purpose Registers : The accumulator is a register which contains one of the operands and stores results of most arithmetic and logical operation. General purpose registers are used for temporary storage of data and intermediate results while computer is making execution of a program. Special purpose registers are used by micro processor itself. They are not accessible to programmers.
7. Memory : Memory is a storage device. It stores program, data, results etc. There are two kinds of memories
  - a] Semiconductor which are faster, smaller, lighter and consume less power are used as the main memory of computer.
  - b] Magnetic memories are slow but they are cheaper than semi conductor memories.

These are used as secondary memories of a computer for bulk storage.
8. Semiconductor memories are mainly
  - a] Random Access Memory [RAM]
  - b] Read Only Memory [ROM]
9. Random Access Memory [RAM]: It is a Read and Write memory i.e., R/W memory. Information can be read or written into it. It has random access property. It is volatile in

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10. In RAM again we have two types

- a] Static RAM
- b] Dynamic RAM

nature i.e., its power contents are lost when power supply is switched off.

Static RAM does not require refreshing but it consumes more power as compared to Dynamic RAM.

Dynamic RAM requires regular refreshing for maintaining its contents.

- \* In RAM again we have two types
    - a] Static RAM
    - b] Dynamic RAM
  - \* Static RAM does not require refreshing but it consumes more power and are more expensive. It is faster than Dynamic RAM.
  - \* Dynamic RAM consumes less power and it requires refreshing for every 2 ms. Memory is required.

**• Dynamic RAM** consumes less power and is faster than SRAM. It is used for main memory.

**11. Read Only Memory [ROM]:** It is non-volatile. It has a random access property. User cannot write into a ROM, it is not accessible. It is also called as Programmable Read Only Memory.

- a]PROM - Programmable Read Only Memory.
  - b]E PROM - Erasable Programmable Read Only Memory.
  - c]E<sup>2</sup>PROM - Electrically Erasable PROM
    - computer receives data and instructions through

12. Input: The computer receives data and instructions through input devices. An input device converts instructions, input data and signals into proper binary form suitable for a digital computer. Examples of input devices are keyboard, mouse, scanner, etc.

The output section transfers data from the microprocessor to output devices.

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14. System Bus : System Bus is a communication path between the microprocessor and the output devices. It is nothing but a group of wires that carries bits.

**14. System Bus :** System Bus is a communication path between the components. It is nothing but a group of wires that carries bits.

15 Intel 8085 is an 8-bit, NMOS microprocessor. It is a 40 pin I.C.

15. Intel 8085 is an 8 bit microprocessor which requires a single +5 d.c. supply for its operation. Its clock speed is about 3.5 MHz. The time for the clock cycle of the Intel 8085 is 200ns.

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It consists of three main sections, an arithmetic and logic unit, a timing control unit and

**16. Arithmetic and Logic Unit :** ALU performs following arithmetic and logical operations.

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a] Addition	b] Subtraction	c] Logical AND
d] Logical OR	e] Logical Exclusive	f] Complement (Logical NOT)
f] Increment (add 1)	g] Decrement (Sub 1)	h] Left Shift (add i/p to

Ptself)

**17. Timing and Control Unit**: It generates timing and control signals which are necessary for

the execution of instructions. It controls data flow b/w CPU & Peripherals. It provides Status, Control and timing signals which are required for the operation of memory and I/o

devices. It controls the entire operations of the microprocessor and peripherals connected to it.

**18. Registers :** Registers are used by the microprocessor for temporary storage and manipulation of data and instructions. Intel 8085 microprocessor has the following registers.

- a]One 8-bit accumulator i.e. register A
- b]Six 8-bit general purpose registers. These are B, C, D, E, H and L
- c]One 16-bit Stack pointer, Sp
- d]One 16-bit Program counter, PC
- e]Instruction register
- f]Status register
- g]Temporary register

**19. Accumulator** is a 8-bit microprocessor in Intel 8080/8085. This is used during the execution

of program for temporary storage. The final result of arithmetic or logical operation is placed in the accumulator. Machine code of Accumulator is 111.

**20.** There are six 8-bit general purpose Registers called B, C, D, E, H and L. To handle 16-bit data two 8-bit registers can be combined. The combination of two 8-bit registers is called a

register pair. The valid register pairs of Intel 8085 are B-C, D-E and H-L. The H-L pair is used to address memories.

**21. Stack Pointer (SP)** holds the address of the Stack top. Stack is a sequence of memory location defined by the programmer. It is used to save the content of a register during the execution of a program. The last memory location of the occupied portion of the stack is called Stack top.

**22. Program Counter (Pcl)** contains the address of the next instruction. The CPU fetches an instruction from the memory, executes it and increments the content of the PC. Thus in the

next instruction cycle it will fetch the next instruction of the program. Instructions are executed sequentially unless an instruction changes the content of the PC.

**23.** There is a set of five flip-flops which act as Status flags. Each of these flip-flop holds 1-bit flag that indicates certain condition which arises during arithmetic and logic operations.

The

following status flags have been provided in Intel 8085.

- a]Carry (CS)
- b]Zero (Z)
- c]Sign (S)
- d]Parity (P)
- e]Auxiliary Carry (AC)

**24. Carry (CS) :** The Carry Status flags holds carry out of the most significant bit resulting from

the execution of an arithmetic operation. If there is a carry from addition or a borrow from

subtraction or comparison the Carry flag CS is set to 1; otherwise 0.

**25. Zero (Z) :** The Zero status flag Z is set to 1 if the result of an arithmetic or logical operation

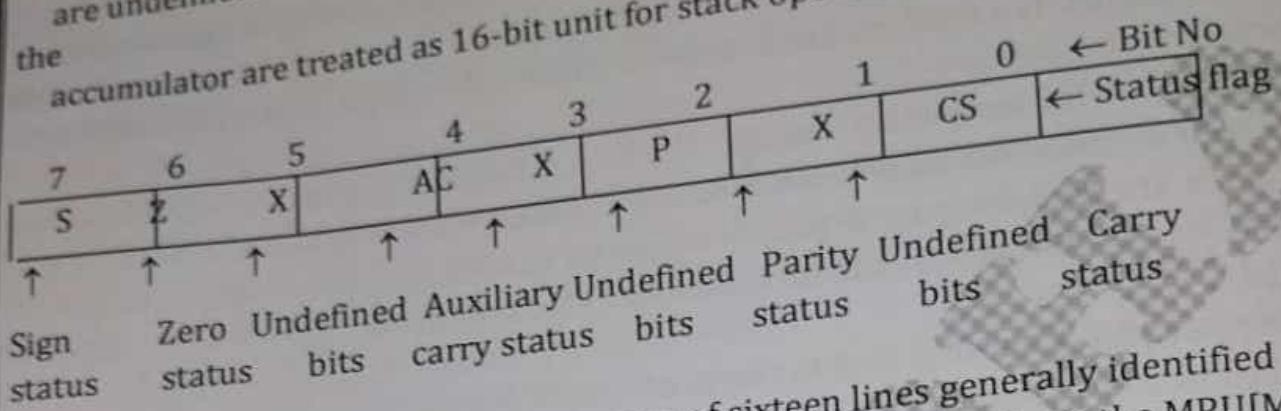
is Zero. For non Zero-result it is set to 0.

**26. Sign (S) :** The sign status flag is set to 1 if the most significant bit of the result of an arithmetic or logical operation is 1, otherwise 0.

**27. Parity (P) :** The Parity status flag is set to 1 when the result of the operation contains even

number of 1's. It is set to Zero when there is odd number of 1's.

28. Auxiliary Carry (AC): The Auxiliary carry status flag holds carry out of bit 3 to 4 resulting from the execution of an arithmetic operation.
29. Program Status Word (PSW): Five bits indicate the five status flags and three bits indicate undefined. The combination of these 8-bits is called Program Status Word. PSW and the accumulator are treated as 16-bit unit for stack operation.



30. Address bus: The address bus is a group of sixteen lines generally identified as A<sub>0</sub> to A<sub>15</sub>. The address bus is unidirectional. Bits flow in one direction from the MPU [Micro Processor Unit] to peripheral devices. The 8085 MPU with its sixteen address lines is capable of addressing  $2^{16} \geq 64$  K memory locations.

31. Data bus: The data bus is a group of eight lines used for data flow. These lines are bidirectional-data flow in both directions b/w the MPU and peripheral devices. In 8-bit MPU the largest number that can appear on the data bus is 1111 1111 ( $255_{10}$ ). It determines the wordlength and the register size of microprocessor.

32. Control bus: Control bus is also bi-directional. Single lines that are generated by the MPU to provide timing of various operations.

33. Pinout of 8085 microprocessor mainly classified into six groups

- a] Address bus
- b] Data bus
- c] Control and status signals
- d] Power supply and frequency signals
- e] Interrupts and peripherals initiated signals &
- f] Serial I/o ports.

34. Address bus: The 8085 has eight signal lines A<sub>8</sub>-A<sub>15</sub>, which are unidirectional and used as

the high order address bus.

35. Multiplexed address/data bus: The signal lines AD<sub>7</sub> to AD<sub>0</sub> are bi-directional. They serve a

dual purpose. They are used as the low-order address bus as well as the data bus. In executing an instruction, during the earlier part of the cycle, these lines are used as the low-order address bus. During the later part of the cycle, these lines are used as the data bus. This is known as multiplexing the bus.

36. Control and Status Signals: This group of signals includes two control signals (RD and WR),

three status signals (IO/r, S<sub>1</sub> and S<sub>0</sub>) to identify the nature of the operation. One special ALE.

**ALE:** It is an address latch enable signal. It goes high during first clock cycle of a machine cycle and enables the lower 8 bits of the address to be latched either into the memory or external latch.

**RD:** It is a signal to control READ operation. When it goes low the selected memory or I/o device is read.

**WR:** It is a signal to control WRITE operation. When it goes low, the data on the data bus is written into the selected memory or I/o location.

**IO/M :** This is a status signal which distinguishes whether the address is for memory or I/o. When it goes high the address on the address bus is for I/o devices. When it goes low, the address on the address is for the memory.

**S<sub>0</sub> and S<sub>1</sub>:** These are status signals sent by microprocessor to distinguish the various types of operation.

S <sub>1</sub>	S <sub>0</sub>	Operations
0	0	Halt
0	1	Write
1	0	Read
1	1	Fetch

Power Supply and Clock frequency:  
Vcc : +5v supply  
Vss : ground reference

**X<sub>1</sub>, X<sub>2</sub> :** These are terminals to be connected to an external crystal oscillator which drives an internal circuitry of the microprocessor to produce a suitable clock for the operation of microprocessor.

**CLK:** It is a clock output for user, which can be used for other digital Ics. Its frequency is same at which processor operates.

#### Interrupts and Externally initiated operations :

**READY :** It is used by the microprocessor to sense whether a peripheral is ready to transfer data or not. If READY is high the peripheral is ready . If it is low, the microprocessor waits till it goes high.

**HOLD :** It indicates that another device is requesting the use of the address and data bus. When HOLD is acknowledged, address bus, data bus, RD, WR and IO/M are tristated.

**HLDA :** It is a signal for HOLD acknowledgment. It indicates that the HOLD request has been received. After the removal of HOLD request HLDA goes low.

**INTR :** It is an interrupt request signal. When it goes low the Program Counter does not increment its count.

**INTA :** It is an interrupt acknowledgment sent by the microprocessor after INTR is received.

RST 7.5, RST 6.5, RST 5.5 and TRAP:

These are the Interrupts.

Line  
TRAP

Location from which next instruction is picked up  
0024

RST 7.5	003C
RST 6.5	0034
RST 5.5	002C

\* RST 7.5, 6.5 & RST 5.5 are the restart interrupts. The order of priority of interrupts is as follows.

TRAP (Highest priority)

RST 6.5

RST 5.5

INTR (lowest priority)

\*TRAP is non maskable interrupt. It is unaffected by any mask or interrupt enable.

**RESETIN** : It sets the Program Counter to zero. It also resets interrupt enable and HLDA, flip-flops. It does not effect any other flag or register except Instruction register. The CPU is held in reset condition as long as RESET is applied.

**RESET OUT** : It indicates that the CPU is being reset.

Serial I/o Ports :

**SID** : It is data line for Serial i/p. the data on this line is loaded not the 7<sup>th</sup> bit of the accumulator is outputted on SOD line when SIM instruction is executed.

Instruction : Each Instruction contains two parts.

1. Operation Code      2. Operand Code

The first part of the instruction which specifies the task to be performed by the computer is

called OP code. The second part of the instruction is the data to be operated on, and is called

Operand.

Instruction word size : According to word size the Intel 8085 instructions are classified into the following three types.

1. One word or 1-byte instruction

2. Two word or 2-byte instruction

3. Three word or 3-byte instruction

One-byte instruction : One byte instruction includes the OP code and Operand in the same byte.

Eg.	Task	OP code	Operand	Binary Code	Hex Code
	Copy the contents of the accumulator to the register C	MOV	C,A	0100 1111	4FH
	Complement (Invert) accumulator	CMA		0010 1111	2FH
	Add the contents of register B to the contents of the accumulator	ADD	B	1000 0000	80H

Two-byte instruction : In a 2-byte instruction the first byte specifies the OP code and the second byte specifies the Operand.

Task	OP code	Operand	Binary Code	Hex Code
Load an 8-bit data byte in the accumulator	MVI	A, data	0D11 1110	3E First byte
32 in the accumulator	MVI	A, 32H	0011 1110 0011 0010 32 H	Second byte Load 3E I-byte II-byte

Three-byte instructions : In a three-byte instruction the first byte specifies the OP code, and the following two bytes specify the 16-bit address. The second byte is low-order address and the third byte is high-order address.

Eg. Task	OP code	Operand	Binary Code	Hex Code
Transform the program sequence to the memory location 2085 H	IMP	2085 H	1100 0011 1000 0101 0010 0000	C3 First byte 85 Second byte 20 Third byte

Instruction Cycle : It is defined as the time required to complete the execution of an instruction. It consists of fetch cycle and execute cycle.

Machine Cycle : It is defined as the time required to complete the operation of accessing either memory or I/O.

T-state : It is defined as one subdivision of the operation performed in one clock period. These subdivisions are internal states synchronized with the system clock.

Execute Cycle : The necessary steps which are carried out to get data, if any, from the memory and to perform the specific operation specified in an instruction, constitute an execute cycle.

Fetch Cycle : The necessary steps which are carried out to fetch an OP code from the memory constitute a fetch cycle.

Timing Diagram : The necessary steps which are carried out in a machine cycle can be represented graphically. Such a graphical representation is called timing diagram.

### INSTRUCTION SET OF INTEL 8085

An instruction is a command given to the computer to perform a specified operation on given data. There are 5 types of instructions.

- 1. Data transfer group
- 2. Arithmetic group
- 3. Logical group
- 4. Branch Control group
- 5. I/o and Machine Control group

Data transfer group : Instruction transfer data from one register to another register, from memory to register, register to memory .

Eg. MOV, MVI, LXI, LDA, STA etc.

Arithmetic group : Instructions of this group perform arithmetic operation such as addition, subtraction, increment or decrement of the content of a register or memory.

Eg. ADD, SUB, INR, DAD etc.

Logical group : The instructions under this group perform logical operation such as AND, OR, Compare, Rotate etc. Eg. ANA, XRA, ORA, CMP, RAL etc.

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Branch Control group: This group includes the instructions for conditional and unconditional jump, subroutine call and return, and restart.  
Eg. JMP, JC, JZ, CALL CZ, RST etc.

I/O and Machine Control group : This group includes the instructions for input / output ports, stack and Machine Control.

Addressing modes:

Each instruction requires certain data on which it has to operate. There are various techniques on which it has to operate. These techniques are called addressing modes. Intel 8085 uses the following addressing modes.

1. Direct addressing

3. Register Indirect addressing

2. Register addressing

4. Immediate addressing.

Direct addressing: In this mode of addressing the address of the operand is given in the instruction itself. Eg. STA 2400 H

Register Indirect addressing: In this mode of addressing the address of the operand is specified by a register pair. Eg. (1) MOV A, M (2) ADD M

Implicit addressing: Instructions which operate on the content of the accumulator. Such instructions do not require the address of the operand.

Eg. CMA, RAL, RAR etc.

INSTRUCTION	STATES	FLAGS	ADDRESSING	MACHINE CYCLE	REMARKS
MOV r <sub>1</sub> ,r <sub>2</sub>	4	none	register	1	Content of register r <sub>2</sub> is moved to register r <sub>1</sub> .
Move the contents of register to register MOV r <sub>1</sub> M	7	none	register	2	The content of memory location whose address is H-L pair is moved to register r.
(Move the content of memory to register) MOVM1 r	7	none	Indirect	2	Content of register r is moved to memory location addressed by HL pair.
(Move the content of r to memory ) MVI r, data	7	none	register	2	data is moved to register r.
(Move Immediate data to register ) MVI M, data	10	none	Immediate	2	data is moved to memory location whose address is H-L pair.
(Move Immediate data to memory) LXI rp, data	10	none	Immediate/ register Indirect	3	The instruction loads 16-bit data immediate to register pair rp.
(Load register pair Immediate )					

LDA addr (Load accumulator direct)	13	none	direct	4	The content of the memory location whose address is specified by the 2 <sup>nd</sup> and 3 <sup>rd</sup> bytes of the instruction is loaded into the accumulator.
STA addr stored (Store accumulator direct)	13	none	direct	4	The content of the A is
LHLD addr (Load H-L pair direct)	16	none	direct	5	in the memory . Load H-L pair direct.
SHLD addr (Store H-L pair direct)	16	none	direct	5	Store H-L pair direct.
LDAX rp (Load accumulator indirect)	7	none	Register indirect	2	The content of the memory location whose address is in register rp is loaded into the accumulator.
STAX rp accumulator (Store accumulator indirect)	7	none	Register indirect	2	The content of the
XCHG	4	none	register	1	is stored in the memory location, whose address is in the rp.
Add r (add register to accumulator)	4	all	register	1	The contents of H-L pair are exchanged with contents of D-E pair.
Add M (add memory to A)	7	all	register indirect	2	The content of register r is added to the content of the accumulator and the sum is placed in the accumulator
Adc r (add r with carry to A)	4	all	register	1	
Adc M (add M with carry to A)	7	all	register indirect	2	
ADI data (add immediate data to A)	7	all	immediate	2	
ACI data (add with C immediate data to A)	7	all	immediate	2	
DAD rp (Add register pair to H-L pair)	10	CS	register	3	

SUB rP (Subtract register from accumulator)	4	all	register	1
SUB M (Subtract memory from accumulator)	7	all	register	2
SBB r (Subtract register from A with borrow)	4	all	register	1
SBB m (Subtract memory from A with borrow)	7	all	Register indirect	2
SUI data (Subtract immediate data from accumulator)	7	all	immediate	2
SBI data (Subtract immediate data from A with borrow)	7	all	immediate	2
INR r (Increment register content)	4	all except carry flag	register	1
INR m (Increment memory content)	10	all except carry flag	register	3
DCR r (Decrement register content)	4	all except carry flag	register	1
DCR m (Decrement memory content)	10	all except carry flag	register	3
INX rp (Increment register pair)	6	none	register	1
DCX rp (Decrement register pair)	6	none	register	1
DAA (Decimal adjust accumulator)	4	all	register	1
ANA r (AND register with A)	4	all	register	1
ANA M (AND memory with A)	7	all	register indirect	2
ANI data (AND immediate data with A)	7	all	immediate	2

ORA r	4	all	register	1
(OR register with A)				
ORA M	7	all	register indirect	2
(OR memory with A )				
ORI data	7	all	immediate	2
(OR immediate data with accumulator)				
XRA r	4	all	register	1
(Exclusive -OR memory with A)				
XRA M	7	all	register indirect	2
(Exclusive -OR memory with A)				
XRI DATA	7	all	immediate	2
(Exclusive -OR immediate data with A)				
CMA	4	none	implicit	1
(Complement the accumulator)				
CMC	4	CS		1
(Complement the carry status)				
STC	4	CS		1
(Set carry status)				
CMP r	4	all	register	1
(Compare register with accumulator)				
CMP m	7	all	register indirect	2
(Compare memory with A)				
CPI data	7	all	immediate	2
(Compare immediate data with accumulator)				
RLC	4	CS	implicit	1
(Rotate accumulator left)				
RRC	4	CS	implicit	1
(Rotate accumulator right)				
RAL	4	CS	implicit	1
(Rotate accumulator left through carry)				
RAR	4	CS	implicit	1
(Rotate A Right through carry)				
JMP	10	none	immediate	3

Conditional jump add r					
JZ add r	7/10	none	immediate	2/3	
JNZ add r	7/10	none	immediate	2/3	
JC add r	7/10	none	immediate	2/3	
JNC add r	7/10	none	immediate	2/3	
JP add r	7/10	none	immediate	2/3	
JM add r	7/10	none	immediate	2/3	
JPE add r	7/10	none	immediate	2/3	
JPO add r	7/10	none	immediate	2/3	

Stack I/o and Machine Control group.IN Port-address : (Input to accumulator from I/o port)

States : 10, Flags : none, Addressing : direct, Machine cycles : 3

OUT Port-address : (Output from accumulator to I/o port)

States : 10, Flags : none, Addressing : direct, Machine cycles : 3

PUSH : (Push the content of register pair to stack)

The contents of register pair (rp) is pushed into the stack.

States : 12, Flags : none, Addressing : registered indirect, Machine cycles : 3

 $[[SP] - 1] \leftarrow [rh]$  $[[SP] - 2] \leftarrow [rl]$  $[SP] \leftarrow [SP] - 2$ POP : The content of the register pair, which was saved earlier is moved from the stack to the register pair. $[rl] \leftarrow [[SP]]$  $[rh] \leftarrow [[SP] + 1]$  $[SP] \leftarrow [SP] + 2$ HLT : States : 5, Flags : none, Machine cycles : 1

The execution of the instruction HLT stops the microprocessor. The registers and status flags remain unaffected.

XTHL : [Exchange Stack-top with H-L] $[L] \leftrightarrow [[SP]]$  $[H] \leftrightarrow [[SP] + 1]$ 

States : 16, Flags : none, Addressing : Register direct, Machine cycles : 5

SPHL : [Move the contents of H-L pair to SP]

The contents of H-L pair are transferred to the SP register.

States : 6, Flags : none, Addressing : register, Machine cycles : 1

EI : [Enable Interrupt]

States : 4, Flags : none, Machine cycles : 1

When the instruction is executed the interrupt system is enabled.

DI : [Disable Interrupts]

When this instruction is executed interrupts are disabled.

States : 4, Flags : none, Machine cycles : 1

SIM : [Set Interrupt Masks]

States : 4, Flags : none, Machine cycles : 1

RIM : [Read Interrupt Mask]

States : 4, Flags : none, Machine cycles : 1

NOP : [No operation]

States : 4, Flags : none, Machine cycles : 1

No operation is performed when this instruction is executed

CALL : CALL instruction is used to call a subroutine. The address of the next instruction is saved in the stack. The contents of stack pointer is decremented by 2 to indicated the new stack top. Thus the program jumps to subroutines starting at address.

$[SP - 1] \leftarrow PCH$

$[SP - 2] \leftarrow PCL$

$SP \leftarrow SP - 2$

$PC \leftarrow \text{Address}$

There are some conditional call instructions i.e.

CC addr Call Subroutine if carry status CS = 1

CNC addr Call Subroutine if carry status CS = 0

CC addr Call Subroutine if result is Zero Z = 1

CNZ addr Call Subroutine if result is not Zero Z = 0

CP addr Call Subroutine if the result is plus, the sign status S = 0

CM addr Call Subroutine if the result is minus, the sign status S = 1

CPR addr Call Subroutine if even parity, the parity status P = 1

CPO addr Call Subroutine if even parity, the parity status P = 0

States : 9/18, Flags : none, Addressing : immediate, register indirect,  
Machine cycles : 2/5

RET : [Return from subroutine]

$[PCL] \leftarrow [[SP]]$

$[PCH] \leftarrow [[SP] + 1]$

$[SP] \leftarrow [SP] + 2$

States : 10, Flags : none, Addressing : register indirect, Machine cycles : 3

There are some conditional return instructions i.e.,

Eg. RC, RNC, RZ, RNZ, RP, RM, RPE, RPO

## INTEL 8086 MICROPROCESSOR

- ❖ It is a first 16 – bit microprocessor of INTEL series.
- ❖ It is a 40 pin IC. It requires +5V single power supply
- ❖ It consists of 16 data lines and 20 address lines.
- ❖ The addressing capacity of a 8086 is 1 M Bytes of memory locations
- ❖ The low order of 16 address lines are multiplexed with data lines.
- ❖ It can operate in two modes of operations Minimum mode and maximum mode
- ❖ The standard 8086 can operate with a maximum mode and maximum mode
- ❖ The 8086 processor is not having on – chip clock generation facility.
- ❖ The clock input signal is generated by the 8284 clock generator/driver chip.
- ❖ It consists of about 117 instructions with nearly about 300 Op codes
- ❖ It contains about 29 000 transistors internally.
- ❖ It is manufactured by using HMOS technology.
- ❖ The range of addresses generated by 8086 processor is 00000 H to FFFFF H
- ❖ The extended memory capability made multi programming feasible and several multiprogramming features have been incorporated into the 8086 processor design.
- ❖ An interesting feature of 8086 is that it prefetches up to 6 instruction bytes from memory and queues them in order to speed up instruction execution
- ❖ It is having multiprocessing capability
- ❖ The memory in the 8086 – based microcomputer is organized as bytes.
- ❖ Memory segmentation is used in 8086 processor
- ❖ An 8086 word in memory consists of any two consecutive bytes
- ❖ The 8086 always accesses a 16 – bit word to or from memory
- ❖ If the first byte of the word is at an even address, the 8086 can read the entire word in one operation
- ❖ If the byte of the word is at an odd address, the 8086 will read the first byte in one operation, and the second byte in another operation
- ❖ The second member of the 8086 family is the 8088 processor
- ❖ 8088 is fully software compatible with its processor, 8086. The basic difference between these two devices is that the way the processors communicate with the outside world.
- ❖ The 8086 is having external 16 – bit path whereas 8088 consists of only 8 – bit data path
- ❖ The 8086 is having 6 – byte instruction queue whereas the 8088 is having only 4 – byte instruction queue.
- ❖ The reason for the smaller queue in 8088 is that it can fetch only one byte at a time and the longer fetch times means that the processor cannot fully utilize a 6 – byte queue
- ❖ The 8088 is also manufactured using High performance Metal Oxide Semiconductor (HMOS) technology.
- ❖ The 8088 can also work in two different modes maximum and minimum modes.
- ❖ The internal architecture of 8086 is divided into two basic units, Bus interfacing Unit (BIU) and Execution Unit (EU).
- ❖ The registers of 8086 can be classified into three groups, segment group, and pointer and index group.
- ❖ The data group consists of AX, BX, CX and DX registers. All these registers are of 16-bit

- ❖ The segment group consists of four 16 – bit segment registers. They are Code Segment (CS) register, Data Segment (DS) register, Extra Segment (ES) register and Stack Segment (SS) register.
- ❖ The pointer and index group five 16 – bit registers. They are Stack pointer (SP) , Base Pointer (BP) Source Index (SI) . Destination Index (DI) and instruction Pointer (IO).
- ❖ The PSW of 8086 processor is nothing but the contents of flags register
- ❖ The flags register of 8086 processor consists of flags. Six conditions flags. Sign flag(S) Zero flag (Z) Auxiliary carry (Ac) flag. Parity flag (P) and Overflow flag (OF) Three control flags. Direction flag (DF) interrupt flag (IF) and Trap flag (TF)
- ❖ The BIU of 8086 sends out addresses, fetches instructions from memory reads data from ports and memory, and writes data to ports and memory. In other words the BIU handles all transfers of data and addresses on the buses for the execution unit.
- ❖ The EU of the 8086 tells the BIU where to fetch instructions or data from. Decodes instructions. And executes instructions.
- ❖ The segment registers always holds the most significant 16-bits of the starting address of the segment i.e . offset of the segment
- ❖ The 8086's 1 – megabyte memory is divided into segments the maximum size of the segment is always 64K bytes
- ❖ The 20 – bit physical address of the memory is generated by the BIU.
- ❖ The length of the 8086 microprocessor will vary from one byte to six bytes.
- ❖ The starting address of the segment must be always divisible by  $10^{16}$ .
- ❖ The instruction set of 8086 can be classified as Data transfer, Arithmetic instructions. Bit manipulation instructions , string instruction program control transfer instructions and Processor control instruction.
- ❖ The data transfer instructions can be general purpose byte or word transfer, simple input and output port transfer instructions, special address transfer instruction, and flag transfer instructions.
- ❖ Arithmetic instructions can be addition, subtraction, multiplication and division.
- ❖ Bit manipulation instructions can be addition subtraction , multiplication and division.
- ❖ Program control transfer instructions can be unconditional iteration control ( loop instructions). Interrupt instructions and high level language instructions
- ❖ Processor control instructions can be flag instructions, external hardware synchronization instructions and no operation instruction
- ❖ The basic addressing modes available in 8086 microprocessor are immediate addressing mode, Direct addressing mode, Register relative addressing mode , Based indexed addressing mode, Relative Based indexed addressing mode, intrasegment Direct, Intrasegment Indirect , and intrasegment Indirect addressing modes
- ❖ The 8086 processor can perform operation on bytes, words (16-bit ), and double words (32-bit)
- ❖ Assembler directive or Pseudo – instruction it is not a machine instruction but rather an instruction to the assembler giving information about some phase of the translation .
- ❖ Example : DB define data byte . Dw define data word DD define double word. EGERMENT END ASSUME etc.
- ❖ Multiplication and Division instructions are not present in 8085 microprocessor, whereas in 8086 multiplication and division instructions are present

- ❖ ECET(CSE-I)

  - ❖ Minimum mode: The minimum mode of operation is used for a small system with a single processor. A system in which 8086 generated all the necessary bus control signals directly.
  - ❖ Maximum mode: The maximum mode is for medium – size to large systems, which often includes two or more processors
  - ❖ The pin MN/MX decides the operating mode of the 8086 processor.
  - ❖ An 8086 interrupt can come from any one of three different sources.
  - ❖ External signal applied to NMI or INTR
  - ❖ Execution of interrupt instruction INT it is referred to as software interrupt.
  - ❖ The third source of interrupt is from some condition produced in the 8086 by the execution to the instruction. Example is the divide by zero interrupt .
  - ❖ The SP and BP (base pointer) registers are used to access data in the stack segment.
  - ❖ The two index registers, SI (source index) and DI (destination index) are used in indexed addressing
  - ❖ Instruction Pointer (IP) always holds the 16-bit address of the next code byte with I the code segment
  - ❖ The TF (Trap flag) is used for single step operation through a program.
  - ❖ The IF (interrupt flag) is used to allow /prohibit the interruption of a program
  - ❖ The DF (Direction flag) is use with sting instructions
  - ❖ In general the 20-bit physical address of the memory location is given by (Segment register)  $\times 10_{16} +$  (Instruction pointer )  
Example : let the contents of code segment register =  $2345_{16}$   
The contents of instruction pointer =  $1585_{16}$   
Physical address of the memory location =  $2345_{16} \times 10_{16} + 1585_{16}$   
 $= 2345_{16} + 1585_{16} = 24AD5_{16}$

## EXERCISE

- Identify 16-bit microprocessor from the following :  
(1) 8085      (2) 80386      (3) 8086      (4) 80486
  - The addressing capacity of 8086 is  
(1) 64 K      (2) 128K      (3) 16 MB      (4) 1MB
  - The clock frequency of a standard 8086 microprocessor is  
(1) 3MHz      (2) 4MHz      (3) 5 MHz      (4) 6 MHz
  - The bit capacity of 8086 microprocessor is  
(1) 8-bit      (2) 16-bit      (3) 32-bit      (4) 20-bit
  - The number of address lines present in 8086 microprocessor  
(1) 16      (2) 20      (3) 24      (4) 32
  - On-chip clock generation facility not available in the following processor :  
(1) 8086      (2) 80286      (3) 68000      (4) All above
  - 8086 is manufactured by using \_\_\_\_\_ technology  
(1) NMOS      (2) PMOS      (3) HMOS      (4) None
  - Total number of pins available in 8086 microprocessor  
(1) 40      (2) 68      (3) 168      (4) 273
  - Identify the modes of operations of 8086 from the following :  
(1) Simple mode and supervisory mode      (2) Minimum mode and maximum mode  
(3) Small mode and big mode      (4) Virtual mode and cache mode

10. Number of hardware interrupts present in 8086 processor  
 1) 5                    2) 4                    3) 2                    4) none
11. 8086 is  
 1) 8/26 – bit processor                    2) Fully software compatible with 8086  
 3) Having 4-byte instruction queue                    4) All the above
12. The instruction length of 8086 vary from  
 1) One to three bytes    2) One to four bytes    3) One to five bytes    4) One to six bytes
13. Identify correct statement from the following  
 1) 8086 can work in two modes                    2) Multiprogramming is feasible in 8086  
 3) Multiprocessing capability is present in 8086                    4) All the above
14. What is the length of instruction queue of 8086 microprocessor  
 1) 4 bytes                    2) 6 bytes                    3) 8 bytes                    4) None of these
15. The address bus width of 8086 processor is 20 – bit , so the instruction pointer (program counter ) register length is \_\_\_\_\_  
 1) 16-bit                    2) 20-bit                    3) 8-bit                    4) 32-bit
16. Total number of flags available in 8086  
 1) 8                    2) 16                    3) 9                    4) 12
17. Different groups of registers present in 8086 processor are:  
 1) Address registers, data registers and control registers  
 2) Stack group, pointer group and address registers  
 3) Data group, stack group and mode register group  
 4) Data group, pointer group and segment group
18. The function of Bus interface unit of 8086 processor is  
 1) Generates 20-bit physical address of the memory  
 2) Responsible for reading instructions from memory  
 3) Responsible for arranging the instructions in the instruction queue    4) All above
19. The range of addresses generated by 8086 is  
 1) 0000H to FFFF H    2) 00000 H to FFFFF H    3) 000 H to FFF H    4) None
20. The maximum size of the segment of 8086 processor is  
 1) 1 KB                    2) 512 KB                    3) 64 KB                    4) 1 MB
21. The starting address of the segment must be always  
 1) Divisible by  $10^{10}$                     2) divisible by  $10^{16}$                     3) Divisible by  $5^{10}$                     4) None
22. The segment register of 8086 always holds:  
 1) 20-bit starting address of the segment                    2) Least significant 16-bits of the starting address of the segment                    3) Ending address of the segment                    4) None
23. The instruction queue present in BIU of 8086 works on \_\_\_\_\_ principle  
 1) FIFO                    2) LIFO                    3) FILO                    4) All the above
24. Overlapping of instruction fetch with execution in 8086 processor causes.  
 1) Increased speed                    2) Reduced speed                    3) No change                    4) None
25. SS register of 8086 always points to \_\_\_\_\_  
 1) Current data segment    2) Current code segment    3) Current stack segment    4)None

ANSWERS

1-3	2-4	3-3	4-2	5-2	6-4	7-3
8-1	9-2	10-3	11-4	12-4	13-4	14-2

15-1	16-3	17-4	18-4	19-2	20-3	21-2
22-2	23-1	24-1	25-3			

PRELIMINARY FEATURES OF 68,000 , 80286 AND 80386THE 68000 MICROPROCESSOR:

- ❖ TMC 68000 is the Motorola's first 16-bit microprocessor.
- ❖ It is designed using HMOS technology and it requires +5V power supply.
- ❖ It can operate with a maximum internal clock frequency of 25 MHz.
- ❖ The 68000 processor does not have on - chip clock generation facility.
- ❖ It is available in 64 pin DIP
- ❖ All the internal registers of 68000 processor are of 32 – bit wide and its ALU is 16 – bit wide.
- ❖ It can operate in two different modes . Supervisor mode and user mode.
- ❖ The super visor mode is also called operating system mode
- ❖ The 68000 processor consists of 24 address lines. Hence its addressing capacity is 16 M bytes.
- ❖ It consists of 16 data lines and address and data lines are not multiplexed
- ❖ The 68000 can operate on five different data types. BCD, bytes, 16- bit words, and 32 – bit long words.
- ❖ It consists of about 56 basic instruction types . It supports 14 addressing modes and contains about 1000 Op codes.
- ❖ The 68000 processor does not support I/O mapped I/O and hence the instruction set does not include IN and OUT instructions
- ❖ This microprocessor includes eight 32-bit registers (D0 – D7) and nine 32 – bit address registers (A0 – A7 plus A7)
- ❖ Since the 68000 processor uses 24 – bit addresses, it discards the uppermost 8 bits ( bits 24 to 31 ), while using the address register to hold memory addresses.
- ❖ Depending on the mode of operation the 68000 uses A7 and A7 as the user or supervisor stack pointer (USP or SSP) respectively.
- ❖ The 68000 status register is composed of two bytes : a user byte and system byte.
- ❖ The user byte includes typical condition codes such as C,V,N,Z and X
- ❖ The contents of the system byte include a 3 – bit interrupt mask, a supervisory flag, and a trace flag.
- ❖ The byte addressing of 68000 includes both odd and even addresses; the word addressing includes only even addresses in increments of 2(0,2,4,6,.....) ; and long word addressing contains even addresses in increments of 4 (0,4,8,12.....).
- ❖ All 68000 instructions occupy one to five words, and they always start on the word boundary and even addresses byte.
- ❖ In the 68000 the first operand of two – operand instruction is the source and the second operand is the destination where as in the case of 8086 . the first operand is the destination and the second operand is the source.
- ❖ INTEL 80286 MICROPROCESSOR:
- ❖ The 80286 can be as much as 2.5 times faster than the 8086 operated at the same clock speed.

- ❖ The intel 80186 and 80286 are also 16 – bit microprocessors, which are extended versions of the 8086 microprocessor.
- ❖ These microprocessors use the concepts of prefetched pipeline structure, parallel processing, and memory management.
- ❖ The 80186 is available in two speeds an 8 MHz and a 10 MHz .
- ❖ It has multiplexed address and data bus.
- ❖ The 80286 microprocessor is available in 68 pin package.
- ❖ The 80286 eliminates the multiplexing of the address and data buses.
- ❖ It consists of 24 address lines, so it can address 16 M bytes of memory locations directly.
- ❖ It support a memory management unit through which it can address 1G bytes of memory . This is called virtual memory.
- ❖ The 80286 microprocessor was mainly designed for multi-user systems .
- ❖ The 80286 microprocessor consists of nearly about 1,30,000 transistors.
- ❖ This processor works in two modes; Real mode and Protected Virtual Address Mode (PVAM)
- ❖ The block diagram of 80286 consists of four separate processing units.
- ❖ a) Bus unit      b) instruction unit    c) execution unit    d) address unit
- ❖ The bus unit performs all memory and I/O read and write operations.
- ❖ The instruction unit fully decodes up to three prefetched instructions and holds them in a queue from where the execution unit can access.
- ❖ The execution unit sequentially executes instructions it receives from the instruction unit.
- ❖ The address unit computes the physical addresses that will be sent out to memory or I/O by the bus unit.
- ❖ The maximum physical address space in the real address mode is 1M byte, just like in 8086.
- ❖ In the protected virtual address mode it uses all the 24 address lines to access up to 16M bytes of physical memory.
- ❖ Since 80286 in having separate address lines and data lines, the processing speed will be improved and simplifies the hardware.
- ❖ The 80286 processor is not having the on – chip clock generation facility. An external 82284 clock generator is required to produce clock signal.
- ❖ The memory for 80286 is set up as an odd bank and an even bank, just like in 8086.
- ❖ The machine status word of 80286 is useful in PVAM
- ❖ The 80286 processor consists of total of 11 status flags.
- ❖ When a program is assembled and made ready for execution in PVAM, a unique, 8- byte quantity called a descriptor is produced for each segment.
- ❖ The descriptors for an 80286 are kept in the form of tables in memory and read into the processor as needed.
- ❖ There are tow types of descriptor tables Global descriptor tables and Local descriptor .
- ❖ The Global Descriptor Table Register (GDTRO) is a 24 – bit register and Local Descriptor Table Register (LDTR) is a 16 – bit registers.
- ❖ The task set register of Task register is a 16 – bit register.
- ❖ The Interrupt Descriptor Table Register is a 24 – bit register
- ❖ The designers of 32 – bit microprocessors have implemented many powerful features of mainframe computer to increases the capabilities of microprocessor chip.

- ❖ The important features of 32 – bit microprocessor includes pipelining, on – chip cache, memory management, and floating point arithmetic.
- ❖ Pipelining is the process in which instruction fetch and execute cycles are overlapped.
- ❖ With memory management technique, the programmers can write much larger programs than those that could fit in the main memory space available to the processors.
- ❖ With the introduction of on – chip cache memory the average access time of the processor can be reduced.

### INTEL 80386 MICROPROCESSOR:

- ❖ The 80386 is an advanced high performance 32 – bit CMOS microprocessor.
- ❖ It contains about 2,75,000 transistors. It is used in 132 – pin Grid Array package.
- ❖ It allows users to work under operating systems such as PC – DOS, UNIX.
- ❖ It consists of 32 – bit address bus and 32 – bit bus. Multiplexing of addresses bus and data buses is not used in the processor.
- ❖ In capable of addressing 4 G bytes of physical memory, and through its memory management unit, it can address 64 Tera bytes of virtual memory.
- ❖ It can operate from a 12.5, 16, 20, 25 or 33 MHz clock frequency.
- ❖ The 80386 processor has highly pipelined architecture and can perform instruction fetching, decoding, executing and memory management functions in parallel.
- ❖ It contains memory management hardware on the chip and it support multitasking
- ❖ The 80386 is software compatible at the object code level with the intel 8086, 80186, and 80286.
- ❖ It contains eight 32 – bit general purpose registers. EAX, EBX, ECX, EDX, ESI, EDI, EBP and ESP.
- ❖ The 386 processor can process 8, 16 and 32 – bit data
- ❖ It contains six 16 – bit segment registers CS, DS, ES, SS, FS and GS. GS, DS and FS are data segment registers.
- ❖ The block diagram of 80386 consists of six functional units Bus interface Unit, Cache Prefetch Unit, Decoding Unit, Execution Unit, Segmentation Unit, and Paging Unit.
- ❖ 386 has two interrupt lines NMI and INTR NMI is a non maskable interrupt and INTR is a maskable interrupt
- ❖ 386 processor can work in two modes: real mode an protected mode. In real mode it is capable of addressing 1 MB of physical memory. The real mode is used to execute 8086 object code .
- ❖ The protected mode provides virtual memory addressing, multilevel protection, paging and multitasking capabilities .
- ❖ The function of BIU of 80386 is to interface memory and I/O devices to 80386
- ❖ The prefetch unit prefetches instructions when the bus interface unit is not executing bus cycles .
- ❖ The instruction decoding unit translates instructions from the prefetch queue into microcodes.
- ❖ The execution unit processes the instructions from the instruction queue.
- ❖ The segmentation unit translates the logical addresses into linear addresses at the request of execution unit
- ❖ The paging unit translates the linear addresses into physical addresses.

- ❖ 80386 processor can work with different data types: Integers, Ordinal (unsigned), Near Pointer Far pointer, String, Bit fields, Bit string and packed/unpacked BCD.
- ❖ 80386 is having nearly about 129 instructions
- ❖ It consists of a 32 – bit status register

**EXRCEISE -1**

1. The bit capacity of 68000 microprocessor is \_\_\_\_\_
  - 1) 8-bit
  - 2) 12-bit
  - 3) 16-bit
  - 4) 24-bit
2. The 68000 microprocessor is \_\_\_\_\_ pin IC
  - 1) 20 pin
  - 2) 60 pin
  - 3) 68 pin
  - 4) 64 pin
3. The power supply required for 68000 processor is
  - 1) +5V
  - 2) +10V
  - 3) -5V
  - 4) -10V
4. 68000 is manufactured by using \_\_\_\_\_ technology
  - 1) NMOS
  - 2) PMOS
  - 3) HMOS
  - 4) CMOS
5. The maximum internal clock frequency of 68000 processor is
  - 1) 20 MHz
  - 2) 15 MHz
  - 3) 25 MHz
  - 4) 10 MHz
6. The number of address lines present on 68000 processor
  - 1) 16
  - 2) 20
  - 3) 28
  - 4) 24
7. Addressing capacity of 68000 processor is
  - 1) 64 KB
  - 2) 16 MB
  - 3) 1MB
  - 4) 10MB
8. The modes of operations of 68000 are:
  - 1) Minimum mode and maximum mode
  - 2) user mode and supervisor mode
  - 3) Supervisor mode and operating system mode
  - 4) None of these
9. The 68000 processor supports
  - 1) Memory mapped I/O technology only
  - 2) I/O mapped I/O technology only
  - 3) Both memory mapped I/O and I/O mapped I/O
  - 4) None
10. The length of program Counter register of 68000 processor is :
  - 1) 24-bit
  - 2) 32-bit
  - 3) 64-bit
  - 4) 16bit
11. 68000 processor is an example for \_\_\_\_\_
  - 1) RISC processor
  - 2) CISC processor
  - 3) DISC processor
  - 4) None
12. The aim of RISC design is:
  - 1) To increase the execution time by reducing the computing speed
  - 2) To increase the computing aped by reducing the execution time of instruction
  - 3) To reduce the hardware by reducing the number of instructions
  - 4) None
13. The 68000 processor consists of \_\_\_\_\_
  - 1) 24 address lines and 16-dta lines
  - 2) 16-address lines and 24-data lines
  - 3) 24-address lines and 24-data lines
  - 4) 24-data lines and 32-address lines
14. Two supply voltages and two ground pins are used in 68000 processor in order to
  - 1) Reduce noise at high frequencies
  - 2) Increase noise at high frequency
  - 3) Reduce noise at low frequencies
  - 4) Increase noise at low frequencies
15. The status register of 68000 processor composed of \_\_\_\_\_ and \_\_\_\_\_
  - 1) System byte, processor byte
  - 2) User byte, processor byte
  - 3) System byte, user byte
  - 4) None of these
16. The flags available in the user byte of 68000 processor are
  - 1) C,V,N and X
  - 2) C,V,X and Z
  - 3) C,V,N,O and Z
  - 4) C,V,N,X and Z

**ECET(CSE-I)**

17. The byte addressing of 68000 includes \_\_\_\_\_  
 1) Odd address only 2) Even address only 3) both odd and even addresses 4) None
18. The word addressing of 68000 includes \_\_\_\_\_  
 1) Odd addresses in increments of 2 2) Even addresses in increments of 2  
 3) Odd addresses in increments of 4 4) Even addresses in increments of 4
19. The long word addressing of 68000 includes \_\_\_\_\_  
 1) Odd addresses in increments of 2 2) Even addresses in increments of 2  
 3) Odd addresses in increments of 4 4) Even addresses in increments of 4
20. In the 68000 the first operand of a two – operand instruction is \_\_\_\_\_ and the second operand is \_\_\_\_\_  
 1) Source , destination 2) Destination, source 4) Destination , destination  
 3) Source, source 4) Destination , destination
21. Since the 68000 processor uses 24 bit addresses, while using the address registers to hold memory addresses, the processor always:  
 1) Discard least significant 8-bits 2) Discards second byte of the address  
 3) Discards uppermost 8-bits 4) None of these
22. The instruction code length of 68000 varies from :  
 1) One to six bytes 2) One to four bits 3) one to three bytes 4) One to five bytes
23. All the internal registers of 68000 processors are of 32-bit length where as its ALU is:  
 1) 32-bit but uses only 16-bit length 2) 16-bit only  
 3) 24-bit but uses 16-bit length only 4) None of these
24. Total number of instructions and opcodes available in 68000 processor are :  
 1) 100 and 1000 2) 500 and 1000 3) 56 and 1000 4) 56 and 560
25. The instruction set of 68000 processor does not includes IN and OUT instructions because  
 1) Memory mapped I/O technology only 2) I/O mapped I/O technology only  
 3) Both memory mapped I/O and I/O mapped 4) None of these

**Key for EXERCISE-1**

1-3	2-4	3-1	4-3	5-3	6-4	7-2	8-2	9-1	10-2
11-1	12-2	13-1	14-1	15-3	16-4	17-3	18-2	19-4	20-1
21-3	22-4	23-2	24-3	25-1					

**EXERCISE-2**

1. The 80286 is an example for \_\_\_\_\_ bit microprocessor  
 1) 8-bit 2) 16-bit 3) 32-bit 4) 64-bit
2. The number of pins of 80286 processor is \_\_\_\_\_  
 1) 40 2) 60 3) 68 4) 100
3. The number of address lines available on 80286 processor  
 1) 16 2) 24 3) 32 4) 40
4. The physical addressing capacity of 80286 is  
 1) 1MB 2) 2MB 3) 4MB 4) 16MB
5. Identify the processor which uses virtual memory concept  
 1) 8086 2) 80186 3) 80286 4) 8088
6. Memory management unit is present in the following processor  
 1) 8085 2) 8086 3) 80186 4) 80286

7. Multiplexing of address and data buses not used in the following processor  
 1) 68000      2) 80286      3) 80386      4) All the above
8. The virtual addressing capacity of 80286 processor is  
 1) 1MB      2) 1GB      3) 2GB      4) 4MB
9. The 80286 processor was mainly designed for  
 1) Multi-user      2) Single user system      3) Parallel processing      4) Pipeline processing
10. Total number of flags available in 80286 processor  
 1) 16      2) 11      3) 14      4) 13
11. The modes of operations of 80286 processor are  
 1) User mode and supervisory mode      2) Real mode and minimum mode  
 3) Protected virtual mode and maximum mode      4) Real mode and protected virtual mode
12. Total number of transistors present in 80286 processor  
 1) 1,29,000      2) 1,30,000      3) 29000      4) 1,75,000
13. The number of pins of 80386 processor  
 1) 68      2) 132      3) 40      4) 273
14. 80386 processor is a logical extension of \_\_\_\_\_  
 1) 80186      2) 8086      3) 80286      4) None of these
15. Number of address lines available on 80386 processor  
 1) 24      2) 36      3) 32      4) 64
16. The 80386 is an example for \_\_\_\_\_  
 1) 16-bit processor      2) 20-bit processor      3) 32-bit processor      4) 64-bit processor
17. The 386 processor is designed by using high speed \_\_\_\_\_ technology  
 1) NMOS      2) HMOS      3) PMOS      4) HCMOS III
18. The Physical addressing capacity of 80386 processor is  
 1) 1GB      2) 2GB      3) 4GB      4) 8GB
19. Virtual addressing capacity of 80386 processor is  
 1) 4GB      2) 4 TB      3) 8TB      4) 64 TB
20. Identify the features (s) of 80386 processor  
 1) Multitasking      2) memory management      3) Pipelined architecture      4) All above
21. The number of basic instructions available in 80386 processor  
 1) 117      2) 129      3) 156      4) 175
22. Identify the processing modes of 80386 processor from the following  
 1) Maximum and minimum mode      2) User mode and supervisor mode  
 3) protected mode, real – address mode V86 mode      4) None of these
23. The number of flags present in 80386 processor  
 1) 8      2) 16      3) 11      4) 13
24. The types of data on which 80386 can operate  
 1) Bytes, words      2) Bits and strings      3) Ordinal numbers and bit strings      4) All above
25. The maximum clock frequency of 80386 processor is  
 1) 15 MHz      2) 25 MHz      3) 30 MHz      4) 33 MHz

**KEY for EXERCISE -2**

1-2	2-3	3-2	4-4	5-3	6-4	7-4	8-2	9-1	10-2
11-4	12-2	13-2	14-3	15-3	16-3	17-4	18-3	19-4	20-4
21-2	22-3	23-4	24-4	25-4					

- ❖ Single chip microcomputers, also known as micro controllers, used primarily to perform dedicated functions.
- ❖ **DCS-51 SERIES OF MICROCONTROLLERS.**
- ❖ The Intel MCS – 51 is a widely used 8 – bit single – chip micro controller family.
- ❖ The family members of the MCS – 51 series are : 8051 AH, 8031 AH, 8751 AH, 80C51, 80C31, 8052 and 8032.
- ❖ The original 8051 was built in HMOS 1 technology .
- ❖ Most of these family members are having at least 64 bytes of R/W memory , and 1 K bytes of ROM on the chip. The range of I/O lines varies from 16 to 40
- ❖ The details of 8031 and 8051 micro controllers are given below .

Micro controller used	Technology ROM	On – chip program memory	On-chip data memory R/W memory
8051 AH	HMOS II	4 K Bytes	128 bytes
80C51	CHMOS	4 K bytes	128 bytes
8031 AH	HMOS II	None	128 bytes
80C31	CHMOS	None	128 bytes

- ❖ The major features of MCS – 51 series of micro controllers:
  1. 8 – bit CPU is present
  2. On – chip oscillator and clock circuitry
  3. 32 I/O lines are present.
  4. 64 K address space for external data memory
  5. 64 K address space for external program memory
  6. Two 16-bit timer /counters are present on the chip.
  7. A five source interrupt structure with two priority levels
  8. Full duplex serial port
  9. Boolean processor
  10. Special function registers (21) are present.
- ❖ 8051 has separate address space for Program Memory and Data Memory. The Program memory can be up to 64K bytes. The lower 4K bytes may reside on – chip. The Data memory can consist of up to 64K bytes off – chip RAM, in addition to which , it includes 128 bytes of con – chip RAM and Special Function Registers (SFR).
- ❖ This series of controllers can operate with a 12 MHz clock and has a very powerful instruction set
- ❖ These are having four programmable I /O ports (32 I/O lines)
- ❖ 80851 /8031 provides five interrupt sources.
- ❖ 8051 /8031 uses five addressing modes Register, Direct, Register Indirect, Immediate and Base – Register plus Index – Register indirect.
- ❖ On 8051 /8031 an integrated bit processor called Boolean Processor is present.
- ❖ Both 8031 and 8051 are available in 40 Pin IC. They require single + 5V power supply.
- ❖ The power dissipation of these IC's is 1 watt

- ❖ The 8051 /8-31 controllers take one microsecond for addition and 4 micro seconds for division and multiplication.

#### THE INTEL 8048 SERIES OF MICROCONTROLLERS:

- ❖ This series consists of number of 8 – bit microcomputers. They are introduced in 1976.
- ❖ The family members of 8048 are 8048, 8748, 8035, 8041, 8021 and 8022.
- ❖ All members of 8048 are 40 pin devices except 8021 which is 28 pin device.
- ❖ The features of 8048 are
  1. It was constructed with High performance MOS technology (HMOS).
  2. It consists of 8 – bit Time / Event counter.
  3. Two single level interrupts are present
  4. 90% of the instructions are of single byte length only.
  5. Reduced power consumption
  6. Compatible with 8080 /8085 Peripherals.
  7. Easily expandable memory and I /O
  8. All instructions will take one or two cycles up to 1.36 Micro sec.
- ❖ The 8048 microcomputer requires single + 5V power supply.
- ❖ The 8048 is having 1K bytes of ROM and 64 bytes of RAM on the chip.
- ❖ It is having extensive bit handling capability and facility for both BCD and binary arithmetic.
- ❖ This series is also called first generation micro-controllers.

#### **EXERCISE**

1. 8048 is an example for
  - 1) Single chip 8-bit microcomputer
  - 2) Single chip 16-bit microcomputer
  - 3) Single chip 20-bit microcomputer
  - 4) None of these
2. The number of pin of 8048 .
  - 1) 28
  - 2) 40
  - 3) 64
  - 4) 68
3. The 8048 is having on – chip ROM of :
  - 1) 1 Kb
  - 2) 2 KB
  - 3) 4 KB
  - 4) 16 KB
4. The 8048 is having on – chip RAM of:
  - 1) 16 bytes
  - 2) 32 bytes
  - 3) 40 bytes
  - 4) 64 bytes
5. 8048 is compatible with the peripherals of \_\_\_\_\_ processors
  - 1) 8085/8080
  - 2) 8086/8088
  - 3) 80286/80186
  - 4) 80386/80486
6. The instructions of 8048 are:
  - 1) One byte only
  - 2) One byte and two byte
  - 3) One to three byte
  - 4) None
7. The maximum clock frequency of 8048 is
  - 1) 5MHz
  - 2) 8MHz
  - 3) 11 MHz
  - 4) None of these
8. 8051/8031 are example of \_\_\_\_\_ micro-controllers.
  - 1) 8-bit
  - 2) 16-bit
  - 3) 24-bit
  - 4) 32-bit
9. 8031/8051 are available in
  - 1) 40 pin pack
  - 2) 64 pin pack
  - 3) 28 pin pack
  - 4) None of these
10. 8031/8051 are manufactured using \_\_\_\_\_ technology
  - 1) HCMOS
  - 2) HMOSH
  - 3) HMOS
  - 4) All the above

11. The internal ROM capacity of 8031 is  
 1) no ROM      2) 4KB      3) 128 bytes      4) 8 KB
12. The internal ROM capacity of 8051 is  
 1) no ROM      2) 4KB      3) 128 bytes      4) 8 KB
13. The internal RAM capacity of 8031 is  
 1) no ROM      2) 4KB      3) 128 bytes      4) 8 KB
14. The internal RAM capacity of 8051 is  
 1) no ROM      2) 4KB      3) 128 bytes      4) 8 KB
15. The number of I/O ports present on 8031/8051 controllers  
 1) two 8-bit      2) four 8-bit      3) two 16-bit      4) four 16-bit
16. The time it takes to complete the addition operation on 8031/8051  
 1) 1 micro second      2) 2 micro seconds      3) 3 micro seconds      4) 4 micro seconds
17. The time it takes to complete the multiplication/ division operation on 8031/8051  
 1) 1 micro second      2) 2 micro seconds      3) 3 micro seconds      4) 4 micro seconds
18. The number of timer/counters presents on 8031/8051  
 1) 1      2) 2      3) 3      4) 4
19. The program memory of 8031/8051 can be expandable from 4 KB to \_\_\_\_\_  
 1) 8KB      2) 16 KB      3) 32 KB      4) 64 KB
20. The power consumption of 8051 is \_\_\_\_\_  
 1) 1 Watt      2) 1 Milli watt      3) 5 Milli watts      4) 5 Watts
21. The number of interrupt sources present for 8051  
 1) three      2) Four      3) five      4) six
22. The 8031/8051 can operate with a maximum clock frequency of  
 1) 12 MHz      2) 10 MHz      3) 15 MHz      4) 20 MHz
23. The number of special function registers present in 8051 are  
 1) 10      2) 128      3) 64      4) 21
24. How many serial ports are present on 8051  
 1) two      2) only one      3) three      4) four
25. The number of addressing modes available in 8051  
 1) five      2) six      3) eight      4) 15

## ANSWERS

1-1	2-2	3-1	4-4	5-1	6-2	7-3	8-1	9-1	10-4
11-1	12-2	13-3	14-3	15-4	16-1	17-4	18-2	19-4	20-1
21-3	22-1	23-4	24-2	25-1					

## EXERCISE

1. No. of comparators needed in 8 bit parallel comparator A/D converter is  
1)1      2)8      3)64      4)2552.
2. An 8085 processor is connected with a crystal of 6MHz frequency. The frequency of the system clock is  
1) 6MHz                  2)2MHz  
3)3MHz                  4)12MHz
3. The content of stack pointer is 80FBH. The content of stack pointer after POP operation is  
1)80FDH                  2) 80FBH  
3) 80FFH                  4)2560H
4. What do9 the content of program counter specify ?  
1)address of instruction being executed  
2)address of the next instruction to be executed  
3)address of the instruction executed last  
4)no. of instructions
5. Which of the following flag follows the MSB of result of each instruction ?  
1)sign                  2)zero  
3) parity                  4)carry
6. No. of T-states required to perform a memory read or memory write operation in 8085 is  
1)1      2)2      3)3      4)4
7. A RAR is classified under -----group of instruction set  
1) Arithmetic                  2)logic  
3) branch                  4)data transfer
8. No. of general purpose registers in 8085 are  
1)3      2)6      3) 8      4)5
9. Microprocessor were introduced in the year  
1)1951                  2) 1961  
3)1971                  4) 1981

10. Flag bits in arithmetic unit provide  
1)status type information  
2) repeatability  
3)facilities for recheck      4)all
11. The fetching, decoding and executing off an instruction is broken down in to several time Intervals ,each of the se intervals ,involving one or more clock periods, is called  
1) A instruction cycle  
2) machine cycle  
3) process cycle      4)none
12. In LIFO ,only the  
1)top of the stack is immediately assessable  
2)first in is assessable  
3)top of the stack is never assessable  
4)first in is not assessable
13. Mneumonics are used in writing a program in a language  
1) assembly language      2) fetch cycle  
3)micro instruction      4) object program
14. OP code is  
1) part of the instruction which tells the computer what operation to perform  
2) an auxiliary that stores the data  
3) a register that receive instructions from the memory  
4) of the instructions in the instruction set.
15. A state during which nothing happens is known as  
1) LDA                  2 ) NOP  
3) HLT                  4)SUB
16. Interaction between CPU and a peripheral device during an input operations known as  
1) Hand shaking                  2)flagging  
3) relocation                  4) subroutine

## ECET(CSE-I)

17. Addressing in which the instruction contains the address of the to be operated on is known as ----- addressing.  
 1)immediate      2)implied  
 3)register      4) direct
18. The 8085 has -----software restarts and -----hardware restarts.  
 1)10,5      2) 7,5      3) 8,4      4)6,6
19. Address to which a software or hardware restart branches is known as  
 1) vector location      2)SID  
 3)SOD      4) TRAP
20. In 8085 to a disable whole interrupt system ( except TRAP)  
 1)DI instruction may be used  
 2)DO instruction may be used.  
 3)the INTERRUPT instruction may be used  
 4) EI instruction may be used
21. For a microprocessor system using IO mapped system IO , the following statement is false  
 1)all data transfer instructions are not available  
 2)IO and memory address spaces are different  
 3)IO address space is greater  
 4) memory space available is greater
22. The stack is specialised temporary -----access memory affected during ----- and -----instructions.  
 1) random, store, load  
 2) random ,PUSH, POP  
 3)sequential ,store ,POP  
 4) sequential ,PUSH ,POP
23. Microprocessor contains a zero and a carry flag ,these are located on the  
 1)Interrupt control      2)status register  
 3) either 1 or 2      4)none
24. In the generic MP

- 1) instruction cycle time period is shorter than the machine cycle time period  
 2) instruction cycle time period is greater than the machine cycle time period  
 3) instruction cycle time period is exactly half of the machine cycle time period  
 4) none
25. In which of the following IO mode of operation , IO port content can directly added to a register  
 1) IO mapped IO  
 2)memory mapped IO  
 3) peripheral IO  
 4) Hand shaking
26. Address in which the location of the data is containing with in the mnemonic is known as  
 1)immediate addressing  
 2) implied addressing  
 3) register addressing  
 4) direct addressing
27. What is the purpose of ready signal  
 1) it is used to indicate the user that CPU is working and ready for use  
 2) it is used to provide proper wait states when CPU is communicating with slow peripheral devices  
 3) it is used to provide proper slowing down of fast peripherals so as to communicate at CPU'S speed  
 4) none
28. Stack pointer store the  
 1) address of bottom of stack  
 2) address of the top of stack  
 3) contents of the bottom of stack  
 4) contents of stack
29. The -----counter ,which is a part of the control unit counts from 0000 to 1111.

- It sends -----of the next instruction to the memory.
- memory signal
  - digital signal
  - program address
  - instruction reference
30. 8085 µP is available as
- 14-pin DIP
  - 24-pin DIP
  - 16-pin DIP
  - 40-pin DIP
31. SUB instruction in 8085
- sets the zero flag
  - resets the zero flag
  - sets the carry flag
  - none
32. The only language which a computer can understand is
- HLL
  - assembly language
  - machine language
  - all
33. TRAP is -----where as RST 7.5, RST  
6.5, RST 5.5 are -----
- maskable, non maskable
  - maskable, maskable
  - non maskable, non maskable
  - non maskable, maskable
34. In µP 8080 and 8085 the----- cycle may have from one to five machine cycles
- micro instruction
  - source program
  - instruction
  - fetch
35. Hardware of the computer is
- physical components
  - programming components
  - hard components
  - none
36. The first company to bring out the µP was
- IBM
  - TEXAS instruments
  - MOTOROLA
  - INTEL corporation
37. µP was invented in
- Japan
  - USA
  - Germany
  - India
38. The technology used for the fabrication of the 8085 µP is
- TTL
  - CMOS
  - PMOS
  - NMOS
39. Which of the following µP is not a 8-bit µP
- 8085
  - 68000
  - Z80
  - 6502
40. The basic operation of µP consists of
- fetching instruction from memory
  - executing instructions
  - fetching and execution of instructions one by one
  - none
41. The stack pointer resides in
- RAM
  - µP
  - ROM
  - Either 1 or 3
42. In µP based system the stack is used to store
- program
  - data
  - contents of PC and registers
  - none
43. The stack pointer operates as
- FIFO
  - LIFO
  - LILO
  - FILO
44. In µP based system the address signals are sent out by
- I/O devices
  - memory
  - µP
  - all
45. When an 8085 µP is reset the address bus contains
- 0000H
  - 002CH
  - 0034H
  - 003CH
46. The no. of flags in 8085 is
- 2
  - 3
  - 5
  - 6
47. A µP is capable of addressing 1MB of memory. Its data bus width is
- 8
  - 12
  - 16
  - can not be predicted
48. A no. of one bit register used in µP to indicate certain conditions are usually

## ECET(CSE-I)

- referred to as  
 1) shift registers      2) latches  
 3) counters      4) flags
49. Which of the following statement is false  
 1)  $\mu$ P has bi-directional address bus  
 2)  $\mu$ P has unidirectional address bus  
 3)  $\mu$ P has bi-directional data bus  
 4)  $\mu$ P has an ALU
50. The following register keeps track of program during execution  
 1) address register      2) Program counter  
 3) Flag register      4) stack pointer.
51. Microprocessors were introduced in the year  
 1] 1951      2] 1961  
 3] 1971      4] 1981
52. Once the information is placed into a read-only memory  
 a] it can be modified easily  
 b] it is continuously modified  
 c] it cannot be modified easily  
 d] none of the above
53. Flag bits in arithmetic unit provide  
 a] status type information  
 b] repeatability  
 c] facilities for rechecks  
 d] all of them
54. The fetching, decoding and executing of an instruction is broken down into several time intervals. Each of these intervals, involving one or more clock periods, is called a  
 a] instruction cycle      b] machine cycle  
 c] process cycle      d] none of them.
55. In LIFO  
 a] only the top of the stack is immediately accessible  
 b] only the top of the stack is never accessible

- c] only the first-in is accessible  
 d] only the first-in is not accessible
56. The degree of nesting is depending upon  
 a] the storage capacity of the stack  
 b] the size of the stack  
 c] the type of memory      d] all of them
57. 64 k is  
 a] 6400      b] 64000  
 c] 65536      d] 66536
58. A microcomputer has a 64 k memory. What is the hexadecimal notation for the first memory location?  
 a] 0000      b] FFFF  
 c] 0FFF      d] 3FFF
59. In the above case the hexadecimal notation for the last memory location is  
 a] 0000      b] FFFF  
 c] 3FFF      d] 5FFF
60. In magnetic film memory, the memory element consists of  
 a] plated wires  
 b] super conductive material  
 c] nickel iron alloy  
 d] doped aluminium
61. An eight bit digital data 10101100 is fed to an ADC. The reference voltage is +10 volts. The analog output voltage will be  
 a] 1.05 V      b] 6.53 V  
 c] 10.10 V      d] 11.11 V
62. EAROM memory is  
 a] magnetically alterable  
 b] electrically alterable  
 c] either (a) or (b)      d] none of them
63. A secondary memory is  
 a] always volatile  
 b] always costlier than primary memory  
 c] always slower than primary memory  
 d] none of the above.
64. A microprocessor 8085 is the enhanced version of..... with essentially the same construction set.  
 a] 6800      b] 68000

65. A state during which nothing happens is known as  
 a]LDA      b]Nop  
 c]MAR      d]OP code
66. OP code  
 a]that part of the construction which tells the computer what operation to perform  
 b]an auxiliary register that stores the data to be added or subtracted from the accumulator  
 c]the register that receives the constructions from the memory  
 d]one of the constructions in the instruction set.
67. In 8085, the instruction register is part of the control unit. The contents of the instruction register are split into two nibbles. The upper nibble goes to the --  
 a]memory address  
 b]controller sequence  
 c]source programme  
 d]micro instruction
68. The mnemonics used in writing a program is called  
 a]assembly language      b]fetch cycle  
 c]micro instruction  
 d]object program
69. A fetch cycle is the  
 a]first part of the instruction cycle  
 b]last part of the instruction cycle  
 c]intermediate part of the instruction cycle  
 d]auxiliary part of the instruction cycle.
70. The ----- counter, which is a part of the control unit, counts from 0000 to 1111. It sends to the memory the ----- of the next instruction.  
 a]memory ---signal      b]digital ---signal  
 c]program--address  
 d]instruction---reference
71. In 8085, the MAR, or ----register, latches the address from the program counter. A bit later, the MAR applies this address to the --, where a read operation is performed  
 a]memory address, ROM  
 b]memory address, RAM  
 c]memory address, PROM  
 d]memory address, EPROM
72. In microprocessors like 8080 and the 8085, the ----cycle may have from one to five machine cycles  
 a]micro instruction      b]source program  
 c]instruction      d]fetch cycle
73. Repeated addition is one way to do multiplication. Programmed multiplication is used in most microprocessors because  
 a]their ALU's can only add and subtract  
 b]this saves on memory  
 c]a separate set of instructions is needed for the two  
 d]none of the above
74. A ----- is used to isolate a bit ; it does this because the ANI sets all other bits to zero.  
 a]subroutine      b]flag  
 c]label      d]mask
75. Interaction between a CPU and a peripheral device that takes place during an I/O operation is known as  
 a]handshaking      b]flagging  
 c]relocating      d]subroutine
76. Addressing in which the location of the data is contained within the mnemonic is known as  
 a]immediate addressing  
 b]implied addressing  
 c]register addressing  
 d]direct addressing
77. Addressing in which the instructions

- contains the address of the data to be operated on, is known as  
 a]immediate addressing  
 b]implied addressing  
 c]register addressing  
 d]direct addressing
78. Interrupt-driven I/O is a type of I/O transfer that  
 a]relies on hardware only  
 b]relies on software only  
 c]either of (a) or (b) above  
 d]both hardware and software
79. Restart is a special type of CALL in which  
 a]the address is programmed but not built into the hardware  
 b]the address is programmed but built into the hardware  
 c]the address is not programmed but built into the hardware  
 d]none of the above
80. 80805 has -----software restarts and -----hardware restarts.  
 a]10, 5                    b]8, 4  
 c]7, 5                    d]6, 6
81. Serial input data of 8085 can be loaded into bit 7 of the accumulator by  
 a]executing a RIM instruction  
 b]executing RST 1        c]using TRAP  
 d]none of them
82. In 8085, TRAP is  
 a]always maskable  
 b]cannot interrupt a service sub-routine  
 c]used for catastrophic events like temporary power failure  
 d]lowest priority interrupt
83. The address to which a software or hardware restart branches is known as  
 a]Vector location                    b]SID  
 c]SOD                                d]TRAP
84. Vectored interrupt is an interrupt that takes the program to a vector location TRAP vectors to 0024 H, RST 7.5 to 003 CH, RST 6.5 to 0034 H and  
 a]RST 5.5                        b]JRST 6.5  
 c]24 H to 48H                    d]JRST 5.5 to 002 CH
85. In 8085, usually the vector location and the next two memory locations contain a JMP instruction. This allows the program to branch to  
 a)a longer sub routine  
 b)a shorter sub routine  
 c)a sub routine free path  
 d]none of them
86. TRAP is -----where as RST 7.5, RST 6.5, RST 5.5 are-----  
 a]maskable, non-maskable  
 b]maskable, maskable  
 c]non-maskable, non-maskable  
 d]non-maskable, maskable
87. In 8085, to disable the whole interrupt system (except TREAP)  
 a]the DI instruction may be used  
 b]the DO instruction may be used  
 c]the INTERRUPT instruction may be used  
 d]the EI instruction may be used.
88. Here are some initialising instructions MVI A, IDH SIM After the SIM is executed, which are the interrupts that are masked?  
 a]5.5 only                        b]6.5 only  
 c]7.5 and 5.5                    d]5.5 and 5.5
89. A micro processor with a 16-bit address bus is used in a linear memory selection configuration (i.e. Address bus lines are directly used as chip selects of memory chips) with 4 memory chips. The maximum addressable memory space is  
 a]64 K    b]16 K    c]8 K    d]4 K

90. A micro processor system using IO mapped IO the following system is NOT true  
 a]memory space available is greater  
 b]not all data transfer instructions are available  
 c]IO and Memory address spaces are distinct  
 d]IO address space is greater.
91. How many outputs are there in the output of a 10-bit D/A converter?  
 a]1000            b]1023  
 c]1024            d]1224
92. In the above case what is the percentage resolution ?  
 a]0.0978 %      b]0.1 %  
 c]0.205 %        d]0.5 %
93. A pair of 2114s can store ----- words of -----bits each.  
 a]214, 8            b]1024, 8  
 c]4228, 16        d]2114, 16
94. The contents of the command register are 23H. Then port C  
 a]is an input port  
 b]is an output port  
 c]is both input as well as output port  
 d]none
95. The stack is a specialised temporary ----- access memory during -- and -- instructions.  
 a]random, store, load  
 b]random, push, load  
 c]sequential, store, pop  
 d]sequential, push, pop
96. The generic microprocessor contains a zero and a carry flag. These are located on the  
 a]interrupt control  
 b]status register  
 c]either (a) or (b)      d]none of them
97. In the generic microprocessor  
 a]instruction cycle time period is shorter than machine cycle time period  
 b]machine cycle time period is shorter than instruction cycle time period  
 c]instruction cycle time period is exactly half of machine cycle time period  
 d]instruction cycle time period is exactly equal to machine cycle time period
98. The contents of the program counter after the call operation point to the first instruction on the  
 a]stack            b]subroutine  
 c]either of them    d]none of them
99. The memory address of the last location of a 1 k byte memory chip is given as OFBFFFH.  
 What will be the address of the first location?  
 a]OF 817H            b]OF 818H  
 c]OF 800H            d]OF 801H
100. What is the length of accumulator?  
 a]8 bits            b]12 bits  
 c]16 bits            d]18 bits
101. How many lines are there in address bus?  
 a] 8 bits            b]12 bits  
 c]16 bits            d]18 bits
102. What is the length of stack Pointer?  
 a] 8 bits            b]12 bits  
 c]16 bits            d]18 bits
103. What is the length of instruction Register?  
 a] 8 bits            b]12 bits  
 c]16 bits            d]18 bits
104. What is the length of Memory Address Register?  
 a] 8 bits            b]12 bits  
 c]16 bits            d]18 bits
105. What is the length of Data Buffer Register?

executed so far.

122. How many lines are there in data bus?  
a]6    b]8    c]12    d]16
123. How many interrupt control lines are there?  
a]6    b]8    c]12    d]16
124. What is the memory word size?  
a]6 bits                          b]8 bits  
c]12 bits                         d]16 bits
125. What is the length of A-register?  
a]6 bits                                  b]8 bits  
c]12 bits                                d]16 bits
126. What is the length of IR (instruction register)?  
a]6 bits    b]8 bits  
c]12 bits                                        d]16 bits
127. What is the length of PC (program counter)?  
a]6 bits    b]8 bits  
c]12 bits                                        d]16 bits
128. What is the length of SP (stack pointer)?  
a]6 bits    b]8 bits  
c]12 bits                                        d]16 bits
129. What is the length of status Word?  
a]6 bits    b]8 bits  
c]12 bits                                        d]16 bits
130. What is the length of temporary register?  
a]6 bits    b]8 bits  
c]12 bits                                        d]16 bits
131. What is the length of Data Buffer Register?  
a]6 bits    b]8 bits  
c]12 bits                                        d]16 bits
132. How many flags are there?  
a]4    b]5    c]6    d]8
133. How many interrupts are there?  
a]4    b]5    c]6    d]8
134. What is the memory word addressing capability ?  
a]32 K    b]64 K  
c]256 K    d]512 K

135. How many I/O ports can be accessed by direct method?  
a]8    b]256  
c]32 K    d]64 K
136. How many I/O ports can be accessed by memory mapped method?  
a]8    b]256  
c]32 K    d]64 K
137. Which of the following interrupts has the highest priority ?  
a]RST 5.5                                      b]RST 7.5  
c]TRAP    d]INTR
138. Which of the following interrupts has the lowest priority ?  
a]RST 5.5                                      b]RST 7.6  
c]TRAP    d]INTR
139. If interrupt service request have been received from all of the following interrupts, then which one will be serviced last ?  
a]RST 5.5    b]RST 6.5    c]RST 7.5
140. If interrupt service request have been received from all of the following interrupts, then which one will be serviced first ?  
a]RST 5.6    b]RST 6.5    c]RST 7.5
141. Which of the following is/are vectored interrupts?  
a]RST 5.5    b]RST 6.5  
c]RST 7.5    d]INTR
142. Which of the following is unmaskable interrupts?  
a]RST 5.5                                      b]RST 7.5  
c]TRAP    d]INTR
143. If instruction RST is written in a program the program will jump to location ?  
a]0020 H                                        b]0024 H  
c]0028 H                                        d]002 CH



ANSWERS:MICROCONTROLLERS

- |           |        |        |        |        |
|-----------|--------|--------|--------|--------|
| 1)D       | 2)C    | 3) A   | 4)B    | 5)A    |
| 6)C       | 7) B   | 8)B    | 9)3C   | 10)D   |
| 11)A      | 12)A   | 13)A   | 14)A   | 15)B   |
| 16)A      | 17)D   | 18)C   | 19)A   | 20)A   |
| 21)C      | 22)B   | 23)B   | 24)B   | 25)B   |
| 26)B      | 27)B   | 28)B   | 29)C   | 30)D   |
| 31)A      | 32)C   | 33)D   | 34)C   | 35)A   |
| 36)D      | 37)B   | 38)D   | 39)B   | 40)C   |
| 41)B      | 42)C   | 43)B   | 44)C   | 45)A   |
| 46)C      | 47)D   | 48)D   | 49)A   | 50)B   |
| 51[C]     | 52[C]  | 53[A]  | 54[B]  | 55[A]  |
| 56[A]     | 57[C]  | 58[A]  | 59[B]  | 60[C]  |
| 61[B]     | 62[B]  | 63[C]  | 64[C]  | 65[B]  |
| 66[A]     | 67[B]  | 68[A]  | 69[A]  | 70[C]  |
| 71[B]     | 72[C]  | 73[A]  | 74[D]  | 75[A]  |
| 76[B]     | 77[D]  | 78[D]  | 79[C]  | 80[B]  |
| 81[A]     | 82[C]  | 83[A]  | 84[D]  | 85[A]  |
| 86[D]     | 87[A]  |        | 88[C]  | 89[A]  |
| 90[D]     |        |        |        |        |
| 91[B]     | 92[A]  | 93[B]  | 94[A]  | 95[D]  |
| 96[B]     | 97[B]  | 98[B]  | 99[C]  | 100[B] |
| 101[D]    | 102[D] | 103[B] | 104[D] | 105[B] |
| 106[D]    | 107[B] | 108[D] | 109[D] | 110[C] |
| 111[D]    | 112[B] | 113[B] | 114[B] | 115[B] |
| 116[B]    | 117[A] | 118[C] | 119[B] | 120[D] |
| 121[D]    | 122[B] | 123[A] | 124[B] | 125[B] |
| 126[B]    | 127[D] | 128[D] | 129[D] | 130[B] |
| 131[B]    | 132[B] | 133[B] | 134[B] | 135[B] |
| 136[C]    | 137[C] | 138[D] | 139[A] | 140[C] |
| 141[AB&C] | 142[C] | 143[C] | 144[B] | 145[D] |
| 146[B]    | 147[D] | 148[C] | 149[A] | 150[D] |

151[C,D] 152[A] 153[C] 154[A] 155[B]  
156[D] 157[B]