Lab 2: Combinational Circuits in Chisel

The lab session will show you how to describe combinational circuits with Chisel. You will run unit tests to test your circuit. You will also synthesize your circuit for an FPGA and test it with the FPGA board. Move **cd** command to change directories until you land in the directory named **lab2**. Note that to go back one directory you can use the command **cd ../**.

Background Reading

This lab is loosely based on Chapter 2 and 5 of Digital Design with Chisel book.

A Majority Voter

Majority voting means that the output of the circuit is the majority of the inputs, e.g., if a==1, b==0, and c==1 the result shall be 1.
Your task is to implement the circuit in Chisel.

Running sbt:

Follow all the necessary steps to run the sbt file and generate verilog code as done before in Lab 1.

```
pc16@pc16:~/chisel_labs_giki/lab2$ sbt run
[info] welcome to sbt 1.9.6 (Private Build Java 17.0.8.1)
[info] loading project definition from /home/pc16/chisel_labs_giki/lab2/project
[info] loading settings for project lab2 from build.sbt ...
[info] set current project to lab2 (in build file:/home/pc16/chisel_labs_giki/la
b2/)
[info] running Majority
[success] Total time: 2 s, completed Sep 21, 2023, 1:09:54 PM
pc16@pc16:~/chisel_labs_giki/lab2$
```

Once you have generated the verilog code, it's time to test your scala code before moving to Vivado.

Testing Sbt:

Having the tests before the implementation is called test driven development and is common in software development, but it is also good practice in hardware design. This time the tests are given to you, in a later lab session you will write your own tests.

Testing Combinational Circuits

For the majority circuit we provide the test given below that can be found under the **src>test>scala** folder of **lab2**:

1. MajorityPrinter:

A test that simply prints the logic table of the circuit. This form of test is helpful for debugging, but not for automated regression tests.

Test 1: Majority Printer

```
pc16@pc16:~/chisel_labs_giki/lab2$ sbt "testOnly MajorityPrinter"
[info] welcome to sbt 1.9.6 (Private Build Java 17.0.8.1)
[info] loading project definition from /home/pc16/chisel_labs_giki/lab2/project
[info] loading settings for project lab2 from build.sbt ...
[info] set current project to lab2 (in build file:/home/pc16/chisel_labs_giki/lab2/)
Logic table for Majority
  a     b     c    -> out
false false false -> 0
true false false -> 0
false true false -> 0
true true false -> 1
false false true -> 0
true false true -> 1
false true true -> 1
true true true -> 1
[info] MajorityPrinter:
[info] Majority print results
[info] - should pass
[info] Run completed in 1 second, 454 milliseconds.
[info] Total number of tests run: 1
[info] Suites: completed 1, aborted 0
[info] Tests: succeeded 1, failed 0, canceled 0, ignored 0, pending 0
[info] All tests passed.
[success] Total time: 2 s, completed Sep 21, 2023, 1:14:21 PM
pc16@pc16:~/chisel_labs_giki/lab2$
```

The next step is to move to vivado and implement the Verilog code on the nexys 4 board following the steps as given in Lab1. Also, please go through the given Readme file to find some lab tasks that you need to do.