1 Introduction

In this lab, we experimented with CD4007, a 14-pin IC consisting of 3 nMOS pMOS pairs. Schematic of CD4007 from its datasheet [1] is given in Figure 1.

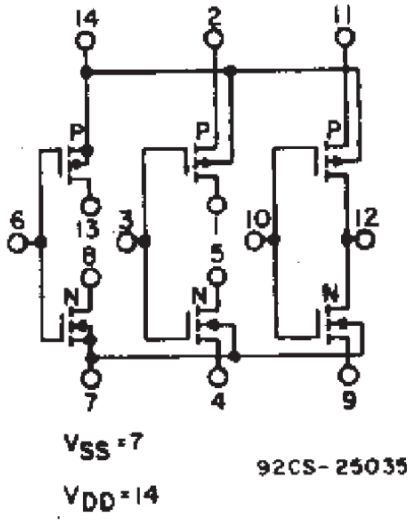


Figure 1. Schematic for CD4007 as per [1].

Since we were to experiment with Resistive Load Inverters only, we used the down leftmost nMOS only. Pin 7 was connected to ground and Pin 14 (V_{DD}) was connected to the $5V\ 1A$ Fixed Channel of the DC Power Supply. We connected Drain of the nMOS (Pin 8) to one of the adjustable channels of the DC Power Supply with a Decade Box connected (series) in between in order to switch values of R without need to tinker with the circuit.

We used a model [2] we have found online for the LTspice simulations requested. The circuit we used for simulations is given below (Figure 2):

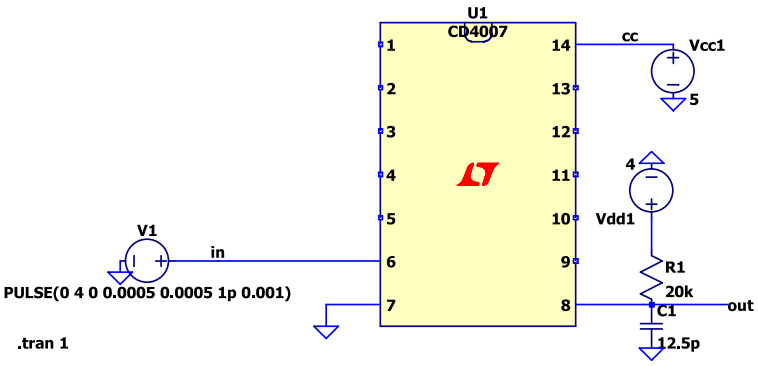


Figure 2. LTspice circuit we used for simulations, CD4007 model by [2]

2 Static Characteristics

2.1 Theory

Resistive Load Inverter, which consists of a nMOS, Resistor and V_{DD} which the output current is supplied from. We consider Gate of the nMOS to be input and Drain of the nMOS to be output. Circuit Diagram of a Resistive Load Inverter is given in Figure 3:

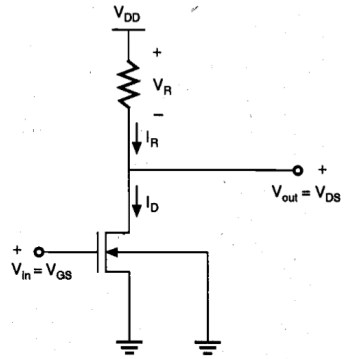


Figure 3. Resistive Load Inverter by [3] (Page 149).

I_{in} is always very small because properties of MOS. It works as a pull-down network where; When input is logic low, nMOS operates in cutoff mode and Drain-Source resistance is very high therefore no current flows through the transistor. This makes the output logic high since current from V_{DD} will flow through R and will exit at V_{out}.

On the opposite; When input voltage V_{in} is logic high, Drain and Source of the transistor will be shorted and current will flow through transistor to the ground. Since there will be current flowing through and the Drain-Source resistance of the transistor will be low because it is conducting, Output voltage V_{out} will be small.

We will be concerned with how V_{out} changes in accord to changes in V_{in}. Plot of output voltage against input voltage is called Voltage Transfer Curve (VTC). Ideally, VTC of an inverter would look like this (Figure 4):

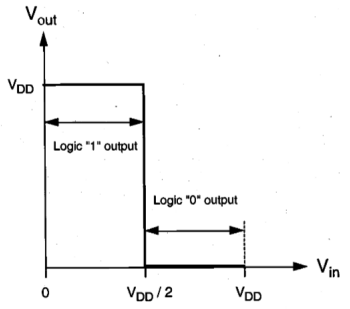


Figure 4. Ideal VTC by [3] (Page 142).

As seen in Figure 4, ideal inverter has no transition region, where value of output voltage is between maximum and minimum values. With real transistors and under influence of physical laws, ideal VTC is not possible and real VTC's have transition regions where output voltage is neither logic high nor logic low. Realistic VTCs rather look like Figure 5:

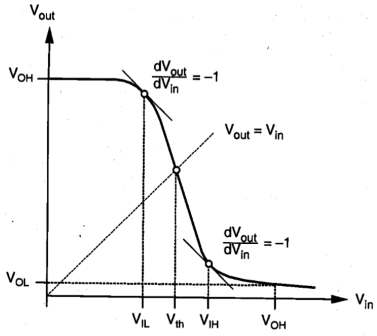


Figure 5. Realistic nMOS inverter VTC by [3] (Page 144).

Figure 5 shows VTC of a realistic nMOS inverter. There are some points marked with labels on axes; these are important voltages that are used as a guideline when mapping voltages which are continuous to logic high and logic low values that are discrete and binary. These are:

V_{OH} Highest output voltage that can be observed (1)

V_{IH} Lowest input voltage that results in a logic low response (2)

V_{OL} Lowest output voltage that can be observed (3)

V_{IL} Highest input voltage that results in a logic high response (4)

V_{th} Input/Output voltage value that satisfies $V_{in} = V_{out}$. (5)

Formulas used for calculation of these voltage points are;

$$V_{OH} = V_{DD} \text{(Since no current flows through nMOS.)} \tag{6}$$

$$V_{IH} = V_{T0} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{k_n \cdot R_L}} - \frac{1}{k_n \cdot R_L} \text{[3] (Page 154)} \tag{7}$$

$$V_{OL} = V_{DD} - V_{T0} + \frac{1}{k_n \cdot R_L} - \sqrt{(V_{DD} - V_{T0} + \frac{1}{k_n \cdot R_L})^2 - \frac{2V_{DD}}{k_n \cdot R_L}} \text{[3] (Page 152)} \tag{8}$$

$$V_{IL} = V_{T0} + \frac{1}{k_n \cdot R_L} \text{[3] (Page 153)} \tag{9}$$

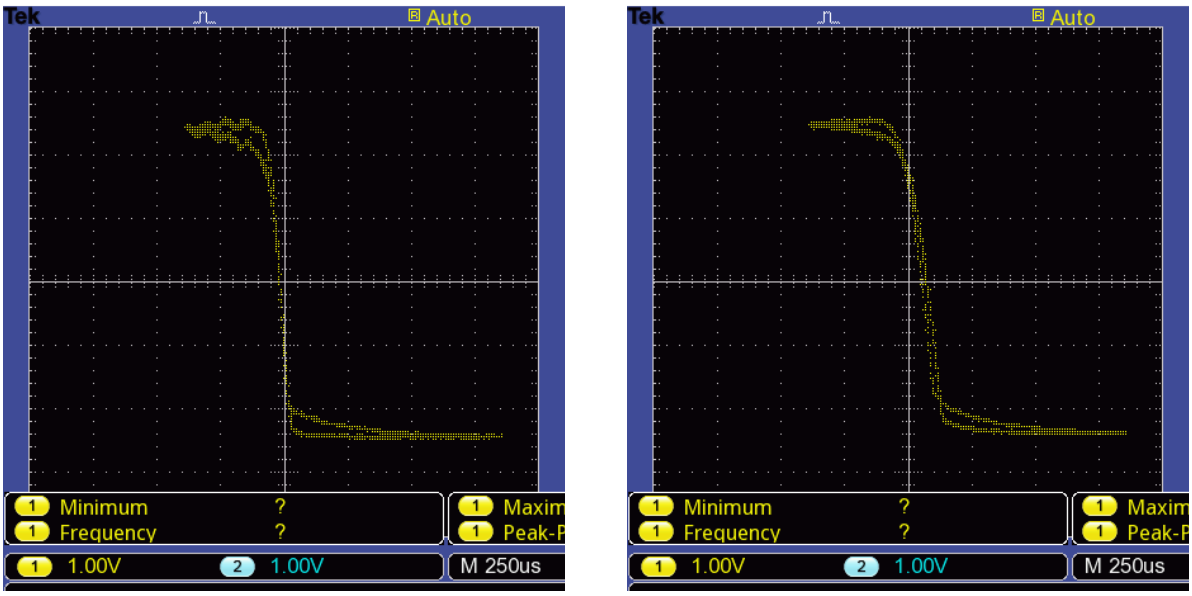
$$V_{th} = \text{Found by substituting } V_{in} = V_{out} \text{ then solving for } V_{th} \tag{10}$$

From these derivations it would be expected that (Disregarding terms that do not come from our control variables); V_{IL} would decrease as R increases, V_{IH} would increase as V_{DD} increases and decrease as R increases, V_{OL} would depend on V_{DD} and R. V_{OH} is equal to V_{DD}.

2.2 Experiment

We set up the circuit on a real breadboard and performed measurements accordingly. Oscilloscopes were used to view V_{in} (Channel 1, X axis) and V_{out} (Channel 2, Y axis). We connected V_{in} to an arbitrary function generator which was configured to generate $0V - 5V$ square wave with 1.0 kHz frequency so that we could observe V_{out} for every value of V_{in} between $0V$ and $5V$.

2.2.1 $V_{DD} = 5V$

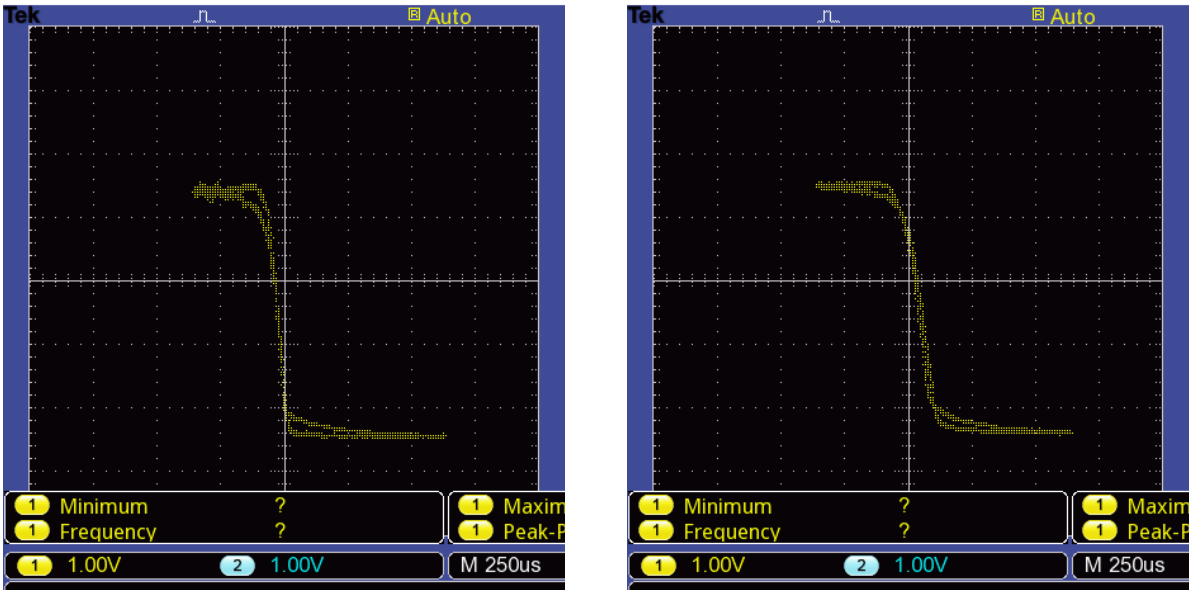


(a) $R = 100k\Omega$, $V_{DD} = 5V$ **(b)** $R = 20k\Omega$, $V_{DD} = 5V$

Figure 6. $\frac{V_{out}}{V_{in}}$ curves for $R = 100k\Omega$ (Figure 6a) and $R = 20k\Omega$ (Figure 6b) when $V_{DD} = 5V$.

By comparing Figure 6b with Figure 6a it can be seen that as R increased, V_{IH}, V_{TH} decreased, squeezing transition region into a narrower area. It can also be said that V_{IL} changed from $1V$ to $1.1V$ but this is not very clear. V_{OL} seems to have stayed the same.

2.2.2 $V_{DD} = 4V$



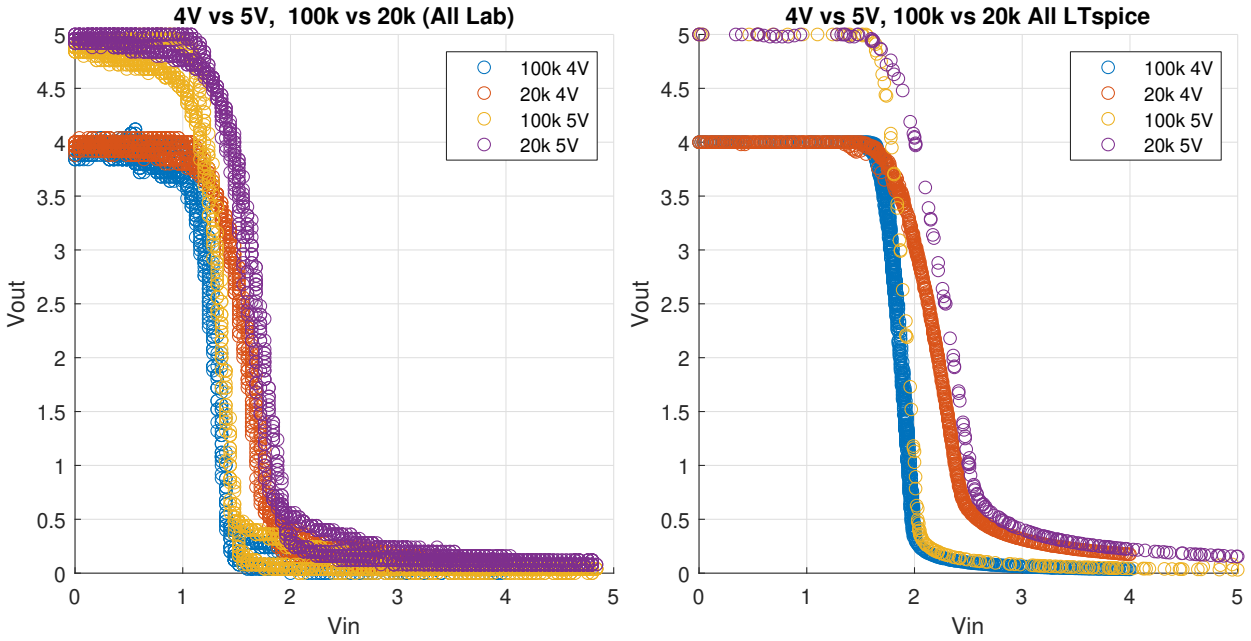
(a) $R = 100k\Omega$, $V_{DD} = 4V$. **(b)** $R = 20k\Omega$, $V_{DD} = 4V$.

Figure 7. $\frac{V_{out}}{V_{in}}$ curves for $R = 100k\Omega$ (Figure 7a) and $R = 20k\Omega$ (Figure 7b) when $V_{DD} = 4V$.

By comparing Figure 7b with Figure 7a we see that changes that happen upon changing R is consistent with the previous part where V_{DD} was equal to $5V$. V_{OH} seems to be decreased from arount $5V$ to $4V$ which makes sense because $V_{OH} = V_{DD}$ (Equation 6).

We also did this part's experiments in LTspice and merged the data with the exported plot data from oscilloscope in order to confirm that the changes happen when changing V_{DD} and R are consistent.

With help of MATLAB we prepared a plots that compare lab experiment and simulation VTC curves (Figure 8a, 8b).



(a) VTC Plots (Lab data). **(b)** VTC plots (Simulation data).

Figure 8. VTC plots for lab data and simulation data prepared using MATLAB.

Figures 8a and 8b look similar except that simulation data has very different V_{th}. It can be observed that changing parameters has had similar/same effects on both simulations and in lab experiments. Since Texas Instruments did not publicly share a SPICE model for CD4007 (Or we could not find it) we used a third party model [2] we found on internet. This might be one of the reasons why we got different critical voltages in simulations. Also, the lab data is noisier than the simulation data.

2.3 Important Voltages

Tables 1 and 2 show the important voltage values (Picked from data) obtained from Lab Experiments and LTspice respectively:

Table 1. Table of important voltages obtained from lab experiment (In Volts).

		V_{DD}									
		$5V$					$4V$				
		V_{OL}	V_{OH}	V_{IL}	V_{IH}	V_{TH}	V_{OL}	V_{OH}	V_{IL}	V_{IH}	V_{TH}
R	$100k\Omega$	0.04	4.90	0.92	1.56	1.44	0.04	4.00	0.96	1.56	1.32
	$20k\Omega$	0.10	4.90	1.08	2.00	1.68	0.08	4.00	1.10	1.96	1.68

Table 2. Table of important voltages obtained from LTspice simulations (In Volts).

		V_{DD}									
		$5V$					$4V$				
		V_{OL}	V_{OH}	V_{IL}	V_{IH}	V_{TH}	V_{OL}	V_{OH}	V_{IL}	V_{IH}	V_{TH}
R	$100k\Omega$	0.08	5.00	1.62	2.09	1.93	0.03	4.00	1.63	2.05	1.90
	$20k\Omega$	0.15	5.00	1.62	2.65	2.31	0.17	4.00	1.68	2.53	2.19

.

Then we calculated noise margins and width of transition region (Volts) for each case. Equations for noise margins and transition region width are;

$$NM_H = V_{OH} - V_{IH} \tag{11}$$

$$NM_L = V_{IL} - V_{OL} \tag{12}$$

$$\text{Transition} = V_{IH} - V_{IL} \tag{13}$$

Noise margins and transition widths for lab experiments and simulations we found are given in Tables 3 and 4:

Table 3. Noise Margin and Transition Region Width Tables for different R and V_{DD} values obtained from lab experiment (In Volts).

	$V_{DD} = 5V$			$V_{DD} = 4V$		
R	NM_H	NM_L	Transition	NM_H	NM_L	Transition
$100k\Omega$	3.34	0.88	0.64	2.44	0.92	0.6
$20k\Omega$	2.9	0.98	0.92	2.04	1.02	0.86

Table 4. Noise Margin and Transition Region Width Tables for different R and V_{DD} values obtained from LTspice (In Volts).

	$V_{DD} = 5V$			$V_{DD} = 4V$		
R	NM_H	NM_L	Transition	NM_H	NM_L	Transition
$100k\Omega$	2.81	1.54	0.47	1.95	1.60	0.42
$20k\Omega$	2.35	1.47	0.93	1.47	1.51	0.85

2.4 Results

The value of V_{OL} and V_{IH} decreased as the resistor was increased from $20k\Omega$ to $100k\Omega$. This change was consistent between experiment and simulation and for both values of V_{DD}.

The value of V_{OH} did not change with changes in R. V_{OH} depended only on V_{DD}. Noise margin high increased when switching from $20k\Omega$ to $100k\Omega$ and increasing V_{DD}.

According to the results of the lab experiment and LTspice simulations, increasing the resistor value decreased the V_{OL} and V_{IL} values, so the noise margin low value also decreased. Additionally, the sharpness of the transition region increases with increasing the resistance.

Upon increasing V_{DD} from $4V$ to $5V$, V_{OL} and V_{IL} values are almost unchanged. Changes in noise margin low were inconsistent between experiment and simulation but the inconsistency did not have much effect on transition region width.

3 Dynamic Characteristics

3.1 Theory

The resistive load inverter circuit in Figure 3 does not seem to have any capacitances, but we know that capacitances are everywhere. And capacitances mean delays. Therefore the resistive load inverter will also have delays/switching times. Let us assume that a capacitor was connected between ground and the wire whose end node is labeled V_{out}. After this small change, the network is essentially something like the following Figure:

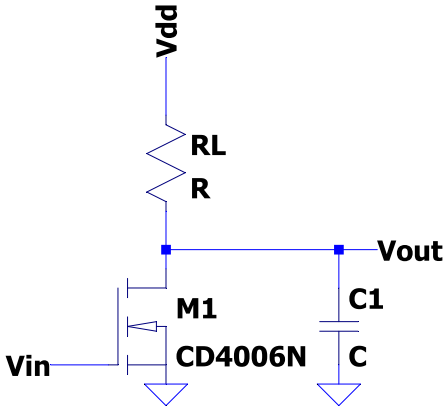


Figure 9. Resistive load inverter where capacitances(except transistor) are accounted as C and load resistance is R.

We are interested in how much time does our inverter need to react to change in inputs. Therefore we will have to evaluate two situations; when output is switching from low to high and vice versa. When output has just became high (Assuming capacitance is not too high and is emptied in previous switch), network will be like the following (Figure 10):

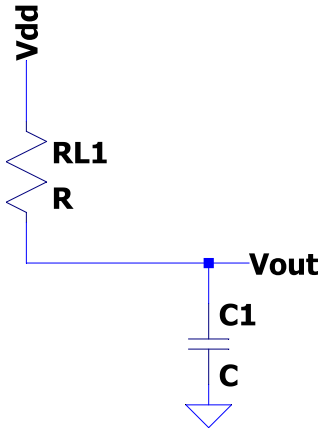


Figure 10. Resistive load inverter when output is just switched from low to high.

In this situation, the network is an RC circuit where V_{DD} will be initially shorted to ground because we assume C is fully discharged ($V_{out} = 0$ because connected to ground). As capacitor becomes charged (R and C will determine the charging speed) ground will be disconnected and V_{out} will approach V_{DD}. Delay in this stage which is caused by capacitor charging will be τ_{PLH}.

Now we have the second state left to analyse which is output switching from high to low;

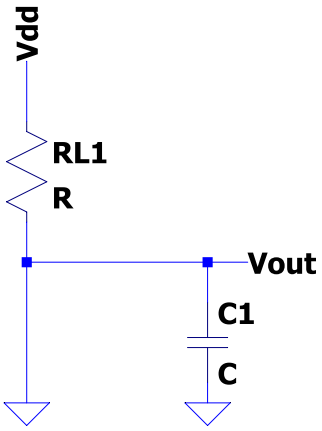


Figure 11. Resistive load inverter when output is just switched from high to low (We assume capacitor is charged).

Circuit of Figure 11 will discharge the capacitor to ground; since there are no explicit resistances in the path between capacitor and ground, discharging will always be faster than charging case (switching from low output to high output). Delay in this stage which is caused by capacitor persisting the high output while discharging will be τ_{PHL}. Therefore we can infer that:

$$\tau_{PLH} >> \tau_{PHL} \tag{14}$$

And that the time difference will increase as R increases.

Deriving τ_{PLH} and τ_{PHL} (taking midpoint as reference):

$$V_{o(\%50)} = \frac{V_{OH} + V_{OL}}{2} \tag{15}$$

$$V_o(t) = (V_{DD}^2 - V_{DD} * V_{OL}) \cdot e^{-t/(R_L \cdot C)} \tag{16}$$

When output voltage is equal to $V_{o(\%50)}$ time will be τ_{PLH} ($V_o(\tau_{PLH}) = V_{o(\%50)}$).

$$V_o(\tau_{PLH}) = (V_{DD}^2 - V_{DD} \cdot V_{OL}) \cdot e^{-\tau_{PLH}/(R_L \cdot C)} \tag{17}$$

$$\tau_{PLH} = (R_L \cdot C) \cdot \ln(\frac{V_{DD}^2 - V_{OL} \cdot V_{DD}}{V_{o(\%50)}}) \tag{18}$$

3.2 Experiment

In the lab experiment we have applied a high frequency (at least 50 kHz) square wave as V_{in} and measured the time delay between the moment when input decreases to $\%50$ of its maximum and the moment that the inverter has raised the output voltage to $\%50$ of its maximum (τ_{PLH}). We have performed this procedure for 4 values of R. Our results are given in Table 5. We also have plotted the table's data (Figure 12).

Experiment Results:

Table 5. Measured switching times (τ_{PLH}).

R_{load} (Ω)	t_p
$1k\Omega$	32 ns
$10k\Omega$	460 ns
$40k\Omega$	1.4 μs
$100k\Omega$	3.8 μs

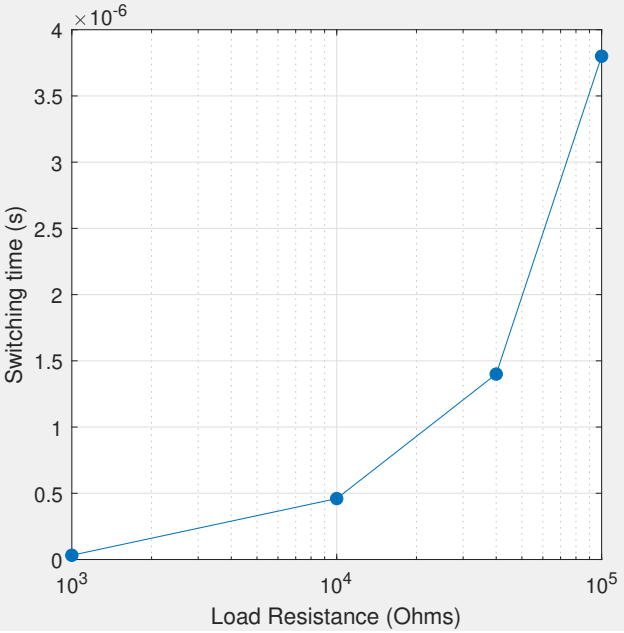


Figure 12. Plot of switching times in Table 5.

Switching time has increased with R.

4 LTspice R Sweep

4.1 Observing changes in VTC

We used circuit in Figure 2 and changed R_1's value to parameter R_L in order to sweep the resistance. Simulation results are given in Figure 13:

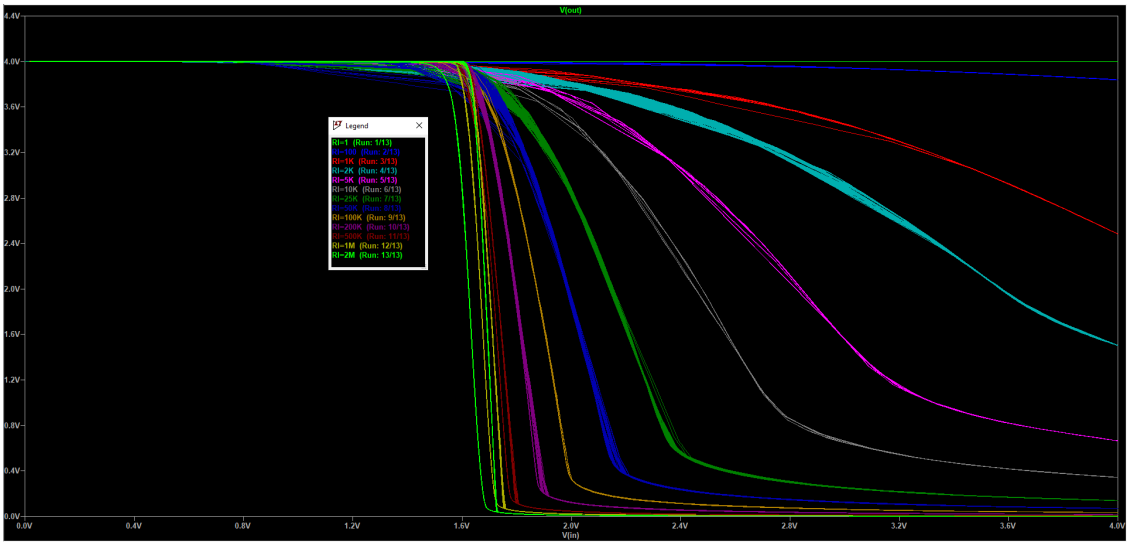


Figure 13. VTC for different R values.

As expected, higher R values result in smaller transition area which makes the inverter become closer to the ideal, but this has a cost that we discuss in the next part.

We also have experimented with sweeping V_{DD} while R was fixed at $20k\Omega$ (V_{CC} and amplitude of V_{in} were also adjusted accordingly). VTC's for different V_{DD}s are given in Figure 14:

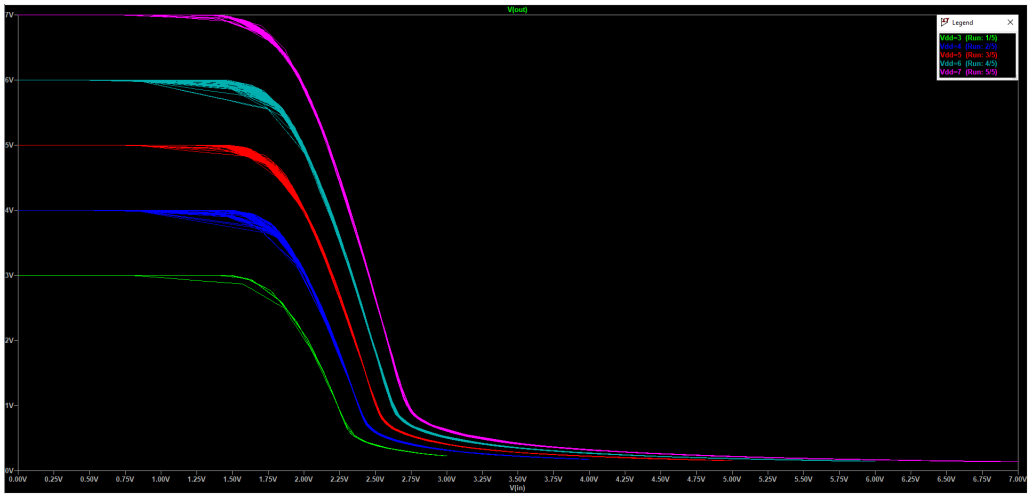


Figure 14. VTC for different V_{DD} values.

In Figure 14 we see that V_{OH} is fully dependent on V_{DD}, Transition region width slightly increased with V_{DD} and V_{OL} did not change much.

4.2 Observing changes in Propagation Delay

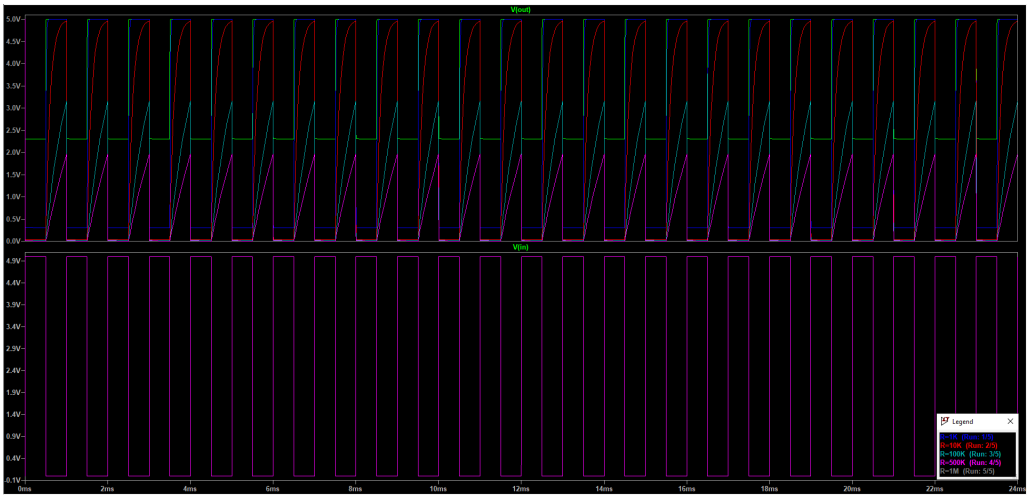


Figure 15. YT plot of V_{out} and V_{in} for different R values (Green: $1k\Omega$, Blue: $10k\Omega$, Red: $100k\Omega$, Pink: $500k\Omega$, Cyan: $1M\Omega$

Looking at Figure 15, we can say that our inference in Equation 14 holds true as upon increasing R, the delay when output is switching from low to high (Upper pane, left side) has increased. While τ_{PHL} did not change considerably.

References

[1] *CMOS Dual Complementary Pair Plus Inverter*, Texas Instruments, 2003. [Online]. Available: https://www.ti.com/lit/ds/symlink/cd4007ub.pdf?ts=1634468875083

[2] *MODELO PARA EL CHIP CD4007*, Facultad de Ingeniería, Universidad de la Republica Uruguay, 2010. [Online]. Available: https://eva.fing.edu.uy/file.php/585/materiales/HD/SPICE/cd4007.mod

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[4] MATLAB, *Version R2021b*. Natick, Massachusetts: The MathWorks Inc., 2021.