

# Verilog HDL

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ICARUS VERILOG

# Icarus Verilog

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- A Verilog simulation and synthesis tool.
- Operates as a compiler that compiles source code written in Verilog into some target format.
- For simulation, the compiler can generate an intermediate form called vvp assembly.
- For synthesis, the compiler generates netlists.



***Icarus Verilog***

More info @ <http://iverilog.icarus.com>

# Integrated Circuit Design Processes

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**Formal and precise description of a complex circuit in an abstract level**

**Automated analysis and simulation**

Automated synthesis into a netlist (specification of electronic component and how they are connected)

Automated placing of electronic components and routing of wires to be sent for fabrication

# How we do?

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**Formal and precise description of a complex circuit in an abstract level**

Write the Verilog source code in a text editor

**Automated analysis and simulation**

Using the Icarus Verilog

Automated synthesis into a netlist  
(specification of electronic component and how they are connected)

Using the Icarus Verilog  
(not done in this course)

Automated placing of electronic components and routing of wires to be sent for fabrication

# Using Icarus Verilog for Simulation

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Verilog source code  
( filename.v)



*iverilog -o filename.vvp file.v*

vvp assembly  
(filename.vvp)



*vvp filename.vvp*

Simulation output

# Installing Icarus Verilog

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In Ubuntu based Linux :

- `sudo apt-get install Verilog`

For Windows :

- Install the setup at <http://bleyer.org/icarus/>
- Set the path environmental variable if not automatically set.

A full guide for all operating systems :

- [http://iverilog.wikia.com/wiki/Installation Guide](http://iverilog.wikia.com/wiki/Installation_Guide)

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Lets do some examples .....