Verilog HDL

ICARUS VERILOG

Icarus Verilog

- A Verilog simulation and synthesis tool.
- Operates as a compiler that compiles source code written in Verilog into some target format.
- For simulation, the compiler can generate an intermediate form called vvp assembly.
- For synthesis, the compiler generates netlists.



More info @ http://iverilog.icarus.com

Integrated Circuit Design Processes

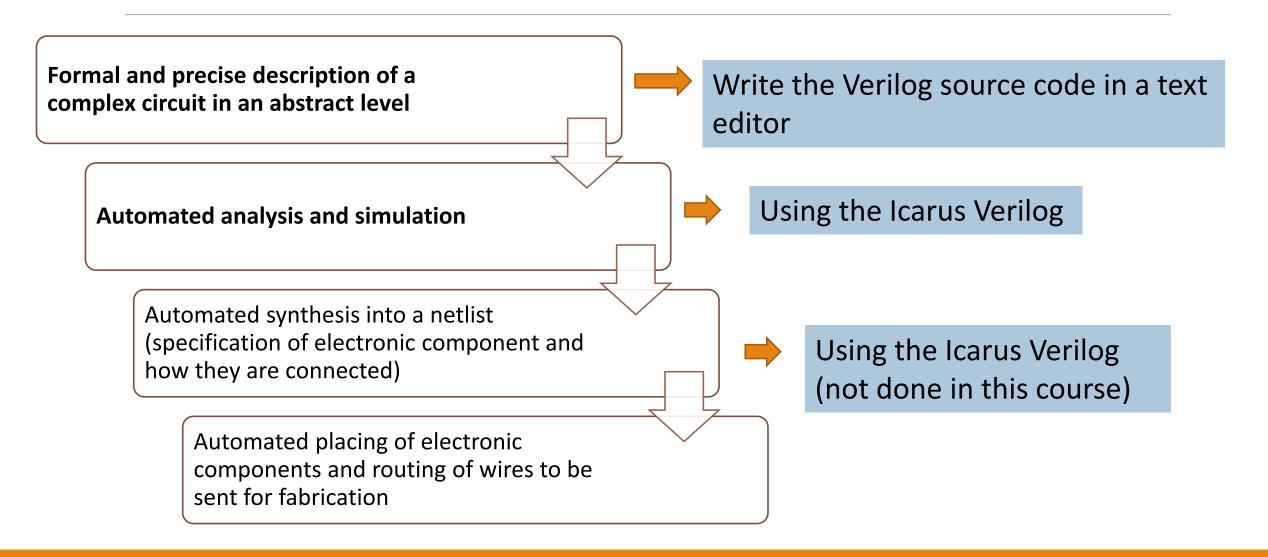
Formal and precise description of a complex circuit in an abstract level

Automated analysis and simulation

Automated synthesis into a netlist (specification of electronic component and how they are connected)

Automated placing of electronic components and routing of wires to be sent for fabrication

How we do?



Using Icarus Verilog for Simulation

Verilog source code (filename.v)



iverilog -o filaname.vvp file.v

vvp assembly (filename.vvp)



vvp filename.vvp

Simulation output

Installing Icarus Verilog

In Ubuntu based Linux:

sudo apt-get install Verilog

For Windows:

- Install the setup at http://bleyer.org/icarus/
- Set the path environmental variable if not automatically set.

A full guide for all operating systems :

http://iverilog.wikia.com/wiki/Installation Guide

Lets do some examples