The PCI bus
Peripheral Component Interconnect

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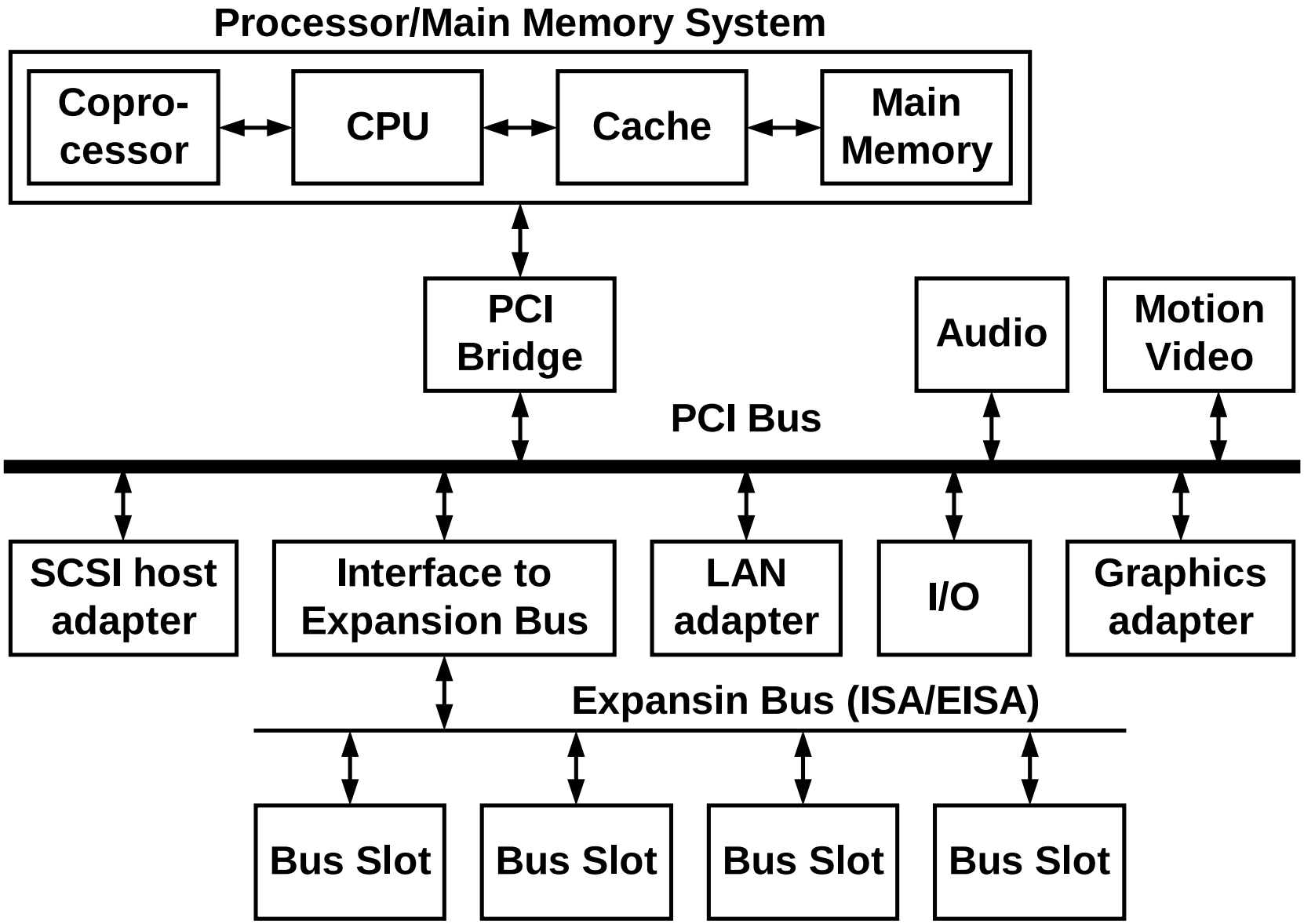
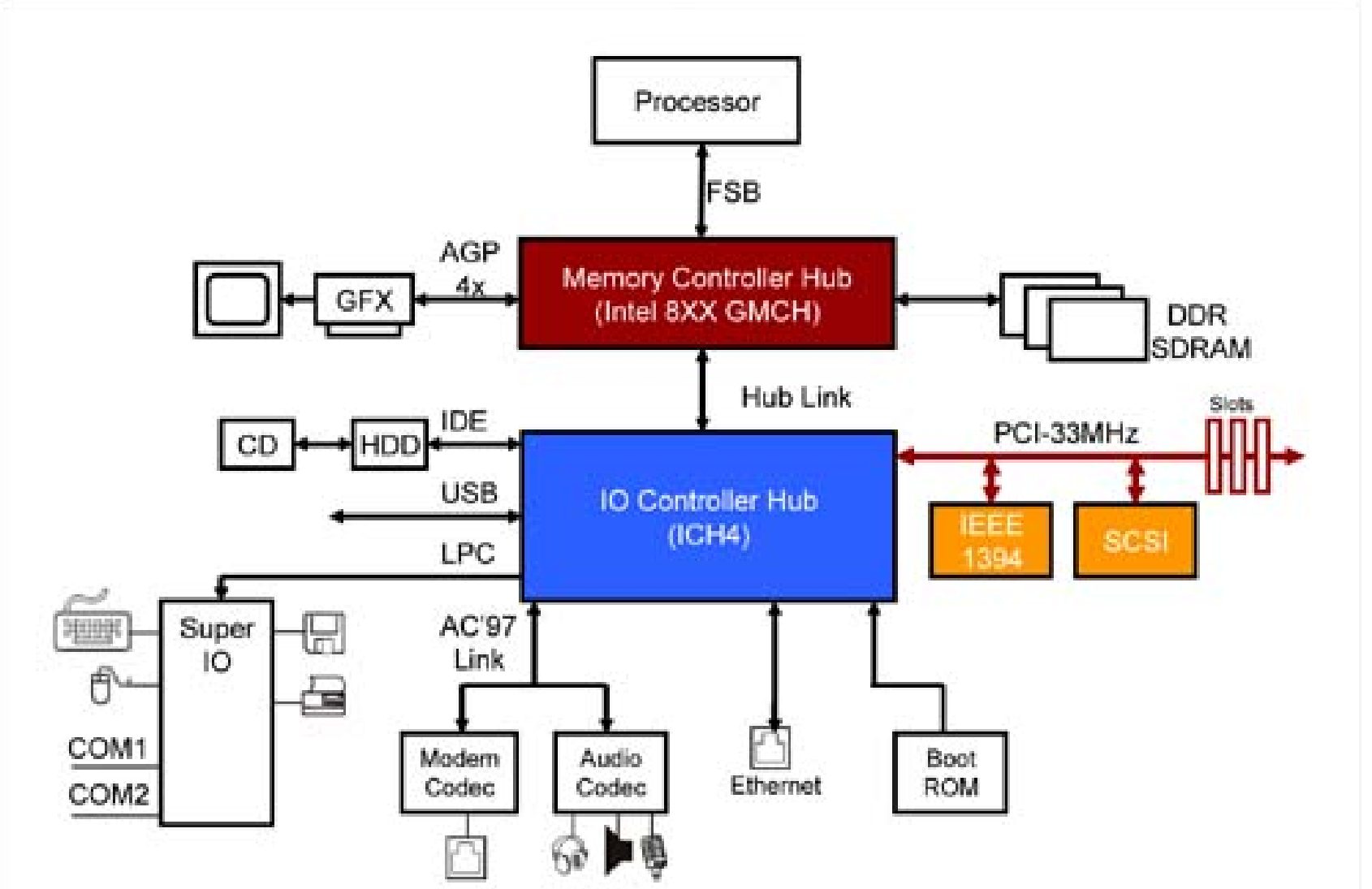
Main features

- Stared in 1990 by Intel
- Now standards maintained by PCI-SIG (Special Interest Group)
- PCI Bus is slower (33 MHz/66 MHz) than Host Bus (100,133,400, 800 MHz Front Side Bus (FSB))
- Coupling of the processor and expansion bus by means of a bridge

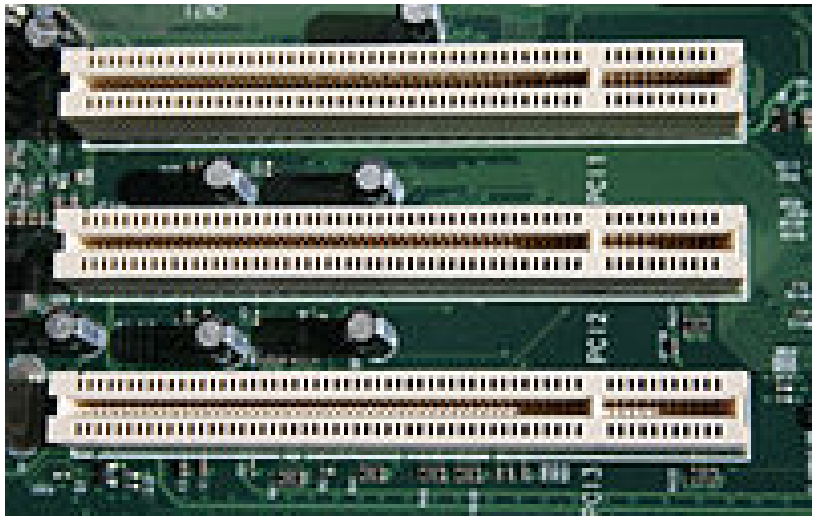
Block diagram of a PCI bus system



Latest Generation of PCI Chipsets



Ver 1.0 PCI 32 bit 5V



32-bit standard bus width , 33 MHz Clock, max transfer rate of 133 Mbytes/s
expansion to 64 bits with a maximum transfer rate of 266 Mbytes/s,
5 V

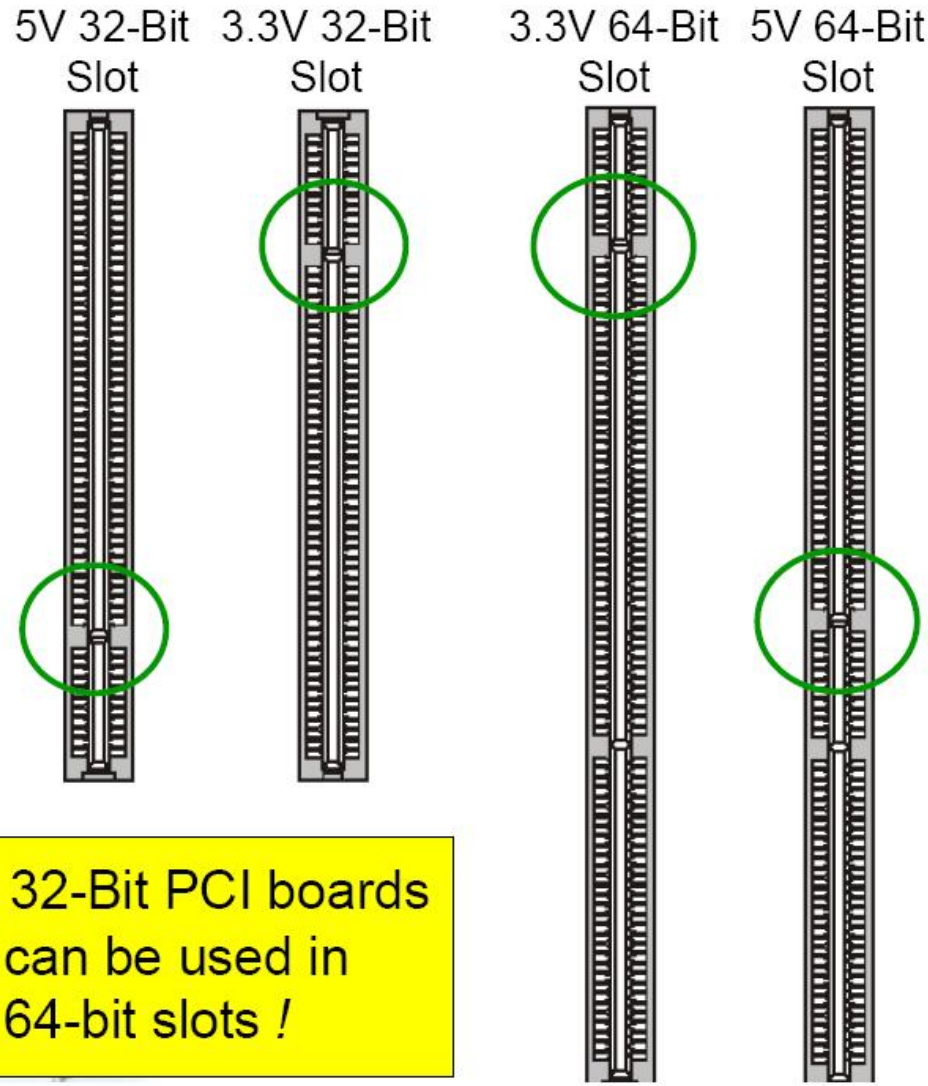
Main features

- 2.0
  - 3.3 V Flipped notch
  - Universal card 3.3 and 5 V have two notches
- 2.1
  - Optional 66 MHz PCI-32/66 266 MB/s, PCI-64/66 532 MB/s
- 2.2
  - Mini PCI for Laptops
- 2.3
  - Stopped 5 V only adapter. Available with 3,3 V
- 3.0
  - No 5 V support

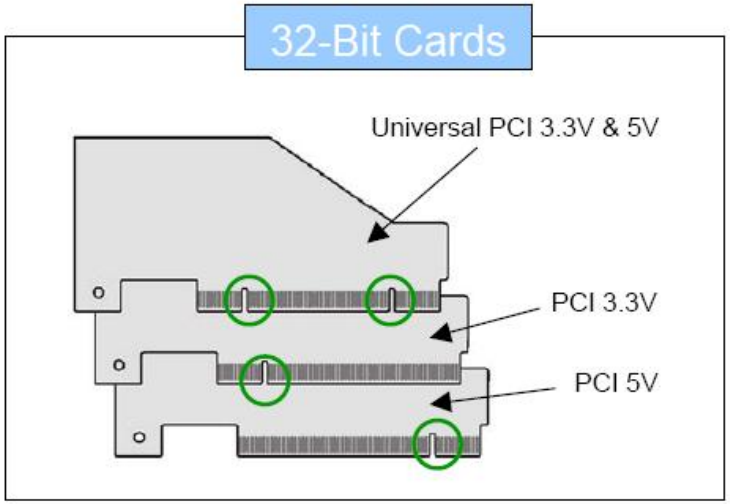
Main features

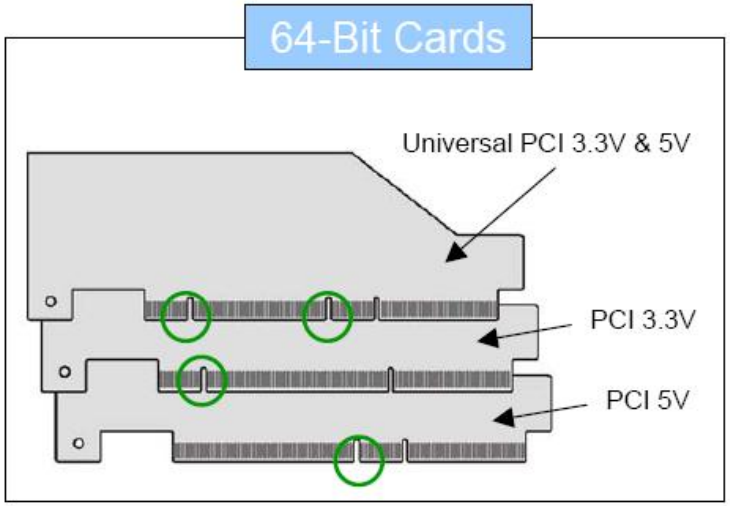
- PCI-X 1.0 (PCI Extended)
  - PCI X 66 PCI X 133 = 66MHx and 133 MHz
  - With 64 bit PCI-64/66 532 Mbytes/s,PCI-X 64/133 1064 Mbytes/s
  - 3.3 and 5 V or 3.3 V only (No 5 V)
- PCI X 2.0
  - Fully backward compatible
  - 2 additional speeds
  - PCI-64/266 2.13 GB/s,PCI-X 64/533 4.26GB/s
- PCI X 3.0
  - PCI-X 1066 8.53GB/s
  - PCI-X 2133 17.07GB/s

32-Bit vs 64-Bit Slots/Boards



32-Bit PCI boards can be used in 64-bit slots *!*



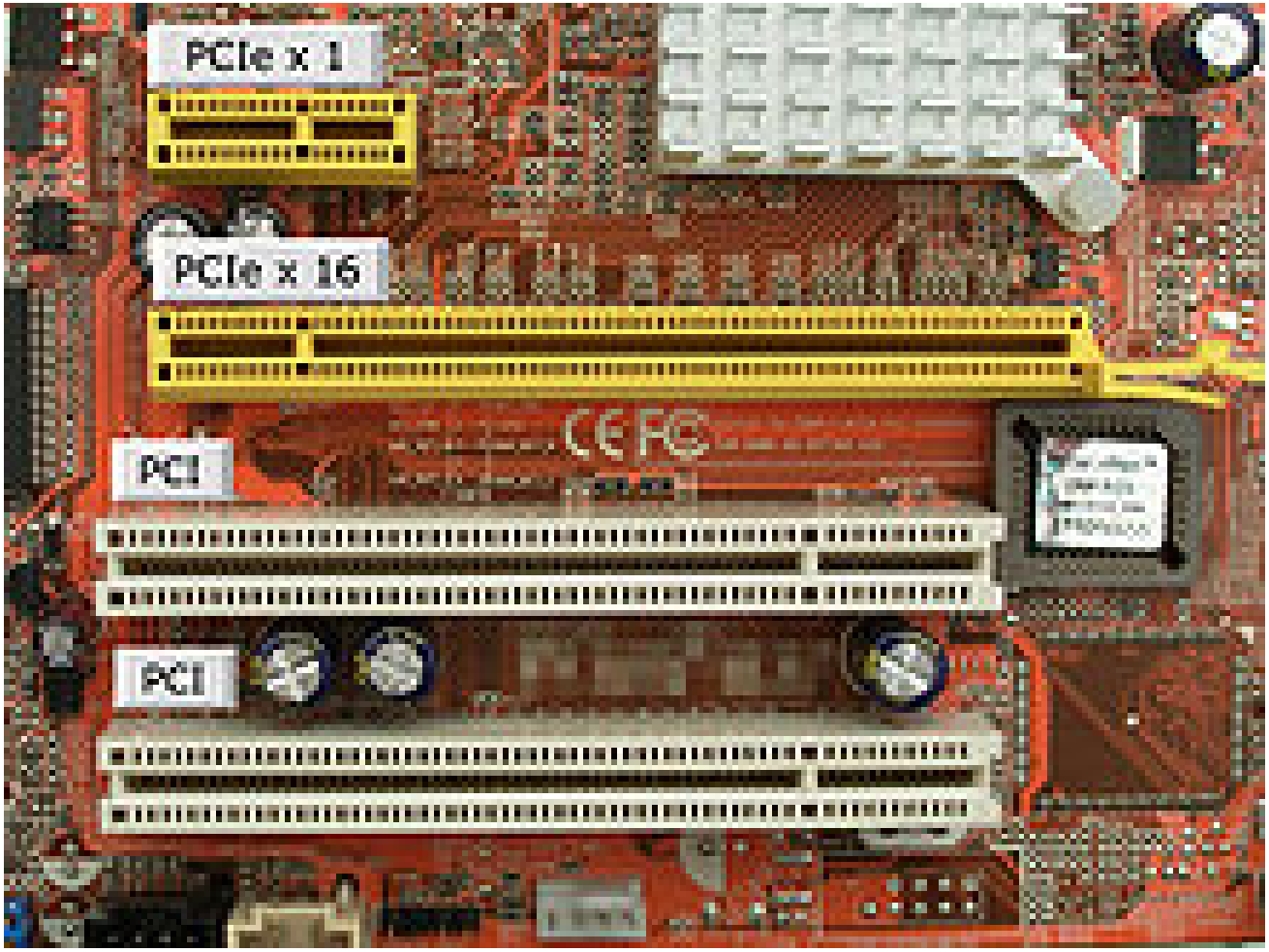


PCI 64bit 3.3 V and 5V

PCIe- PCI Express

- Incompatible with PCI and PCIx
- A serial bus
- Studied separately

PCI 5V, PCI express x1 and x16



Signals

- CLK
  - Clock provide timing reference for all transfers (Synchronous bus)
  - All signals (Except Reset/Int) sampled on the rising edge of the cock
  - Min frequency=0 Hz for clock to be suspended for power saving purposes

- RST# (#=active low)
  - Hardware reset of a PCI device
  - PCI devices configuration registers, state machines, O/P siignals will be placed in initial state
  - Remain active for 100us after CLK become stable to ensure all PCI devices are reset (Power on reset)

Address and Data lines

- AD[31:0] – Address and Data are multiplexed and has two phases
  - Address phase – Transfer 32 bit address
  - Data phase – Transfer 32 bit of data
- C/BE[3:0]#- Bus Command and Byte Enable are multiplexed
  - Address phase: Carries bus command that define the type of transfer to be performed
  - Data phase: Carries byte enable (active low) information
  - | MSB | | | LSB |
  - | C/BE[3]# | C/BE[2]# | C/BE[1]# | C/BE[0]# |

Interface Control Lines

- FRAME#
  - Driven by a initiater
  - To signal start of new bus transaction
  - Address phase occurs during the first clock after high to low transition
  - Then data phase starts
  - Hold low to end of transaction or one before last data phase

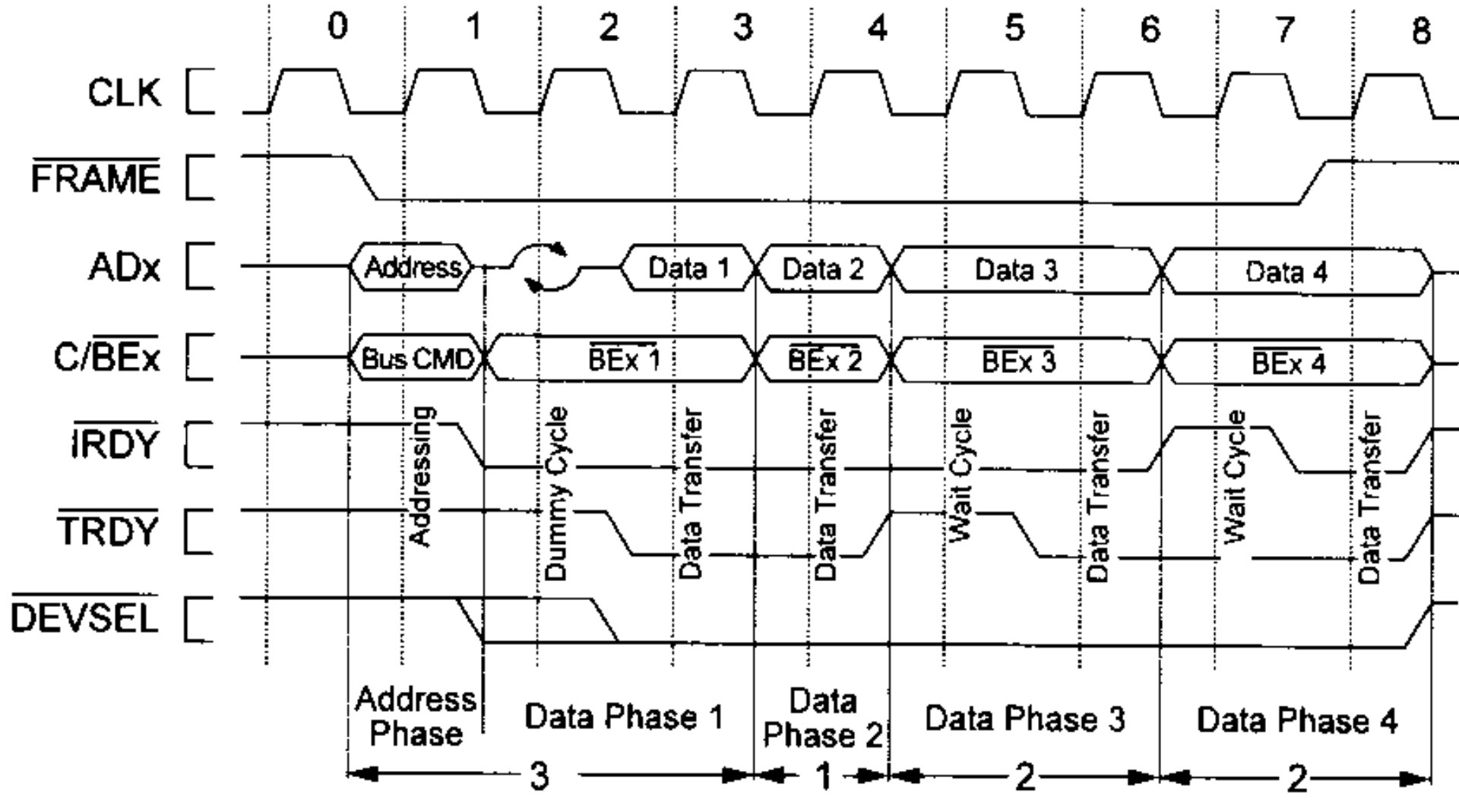
IRDY# Initiator Ready

- Driven low by the initiator
- To indicate that initiator is ready to complete current data phase
- Write data phase
  - Indicate Initiator has placed valid data on AD[31:0]
- Read data phase
  - Indicate Initiator ready to accept data
- Once asserted Initiator holds IRDY# low until TRDY# is low to complete transfer or target se STOP# to terminate
- This permit the initiator to insert wait state to sloe the data transfer

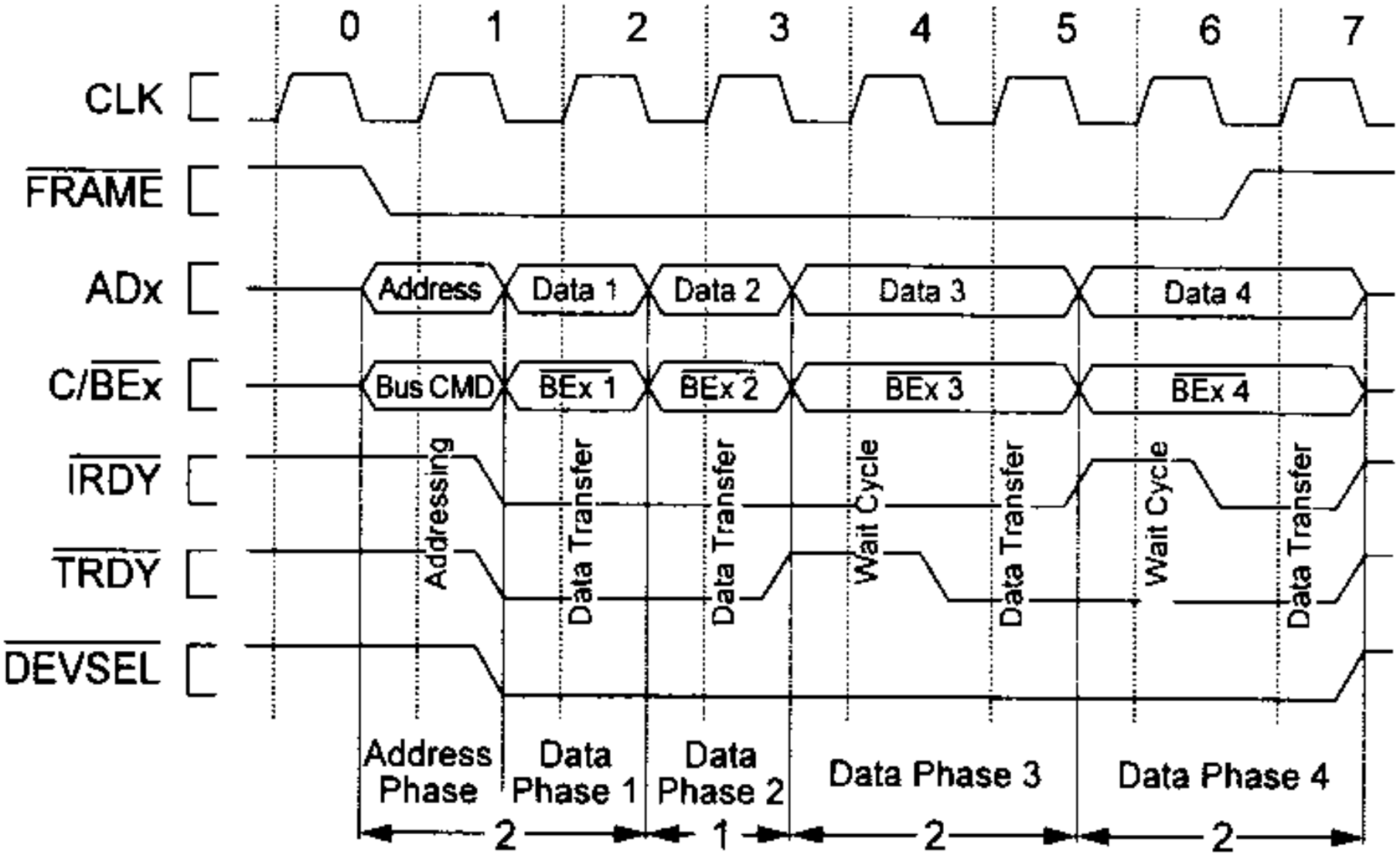
TRDY# Targert ready

- Driven low by the target
- To indicate that target is ready to complete current data phase
- Write data phase
  - Indicate Target ready to accept data
- Read data phase
  - Indicate target has placed valid data on AD[31:0]
- Once asserted Target holds TRDY# low until IRDY# is low to complete
- This permits target to initiate wait state as needed to slow the data transfer

The PCI read transfer burst



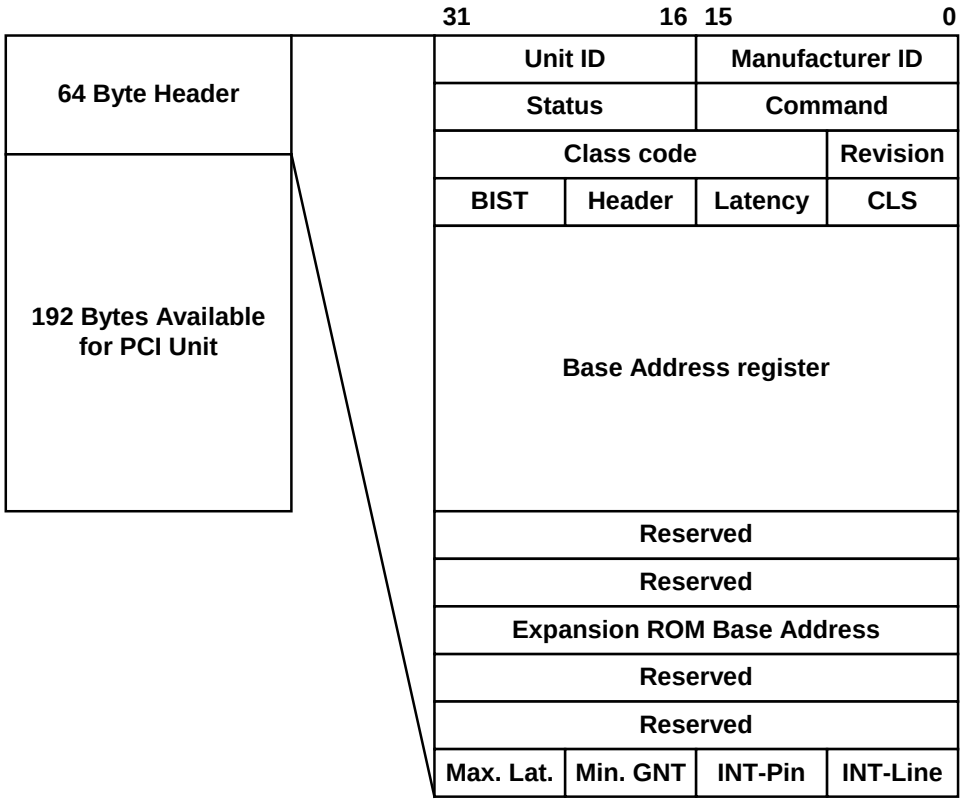
The PCI write transfer burst.



Auto configuration

- PCI device supports rigorous auto configuration mechanism
- Each PCI device and each function of a device (if multifunction device) has 256 byte configuration are of 64 nos 32 bit registers (64x4 bytes=256 Bytes)

Configuration Address Space

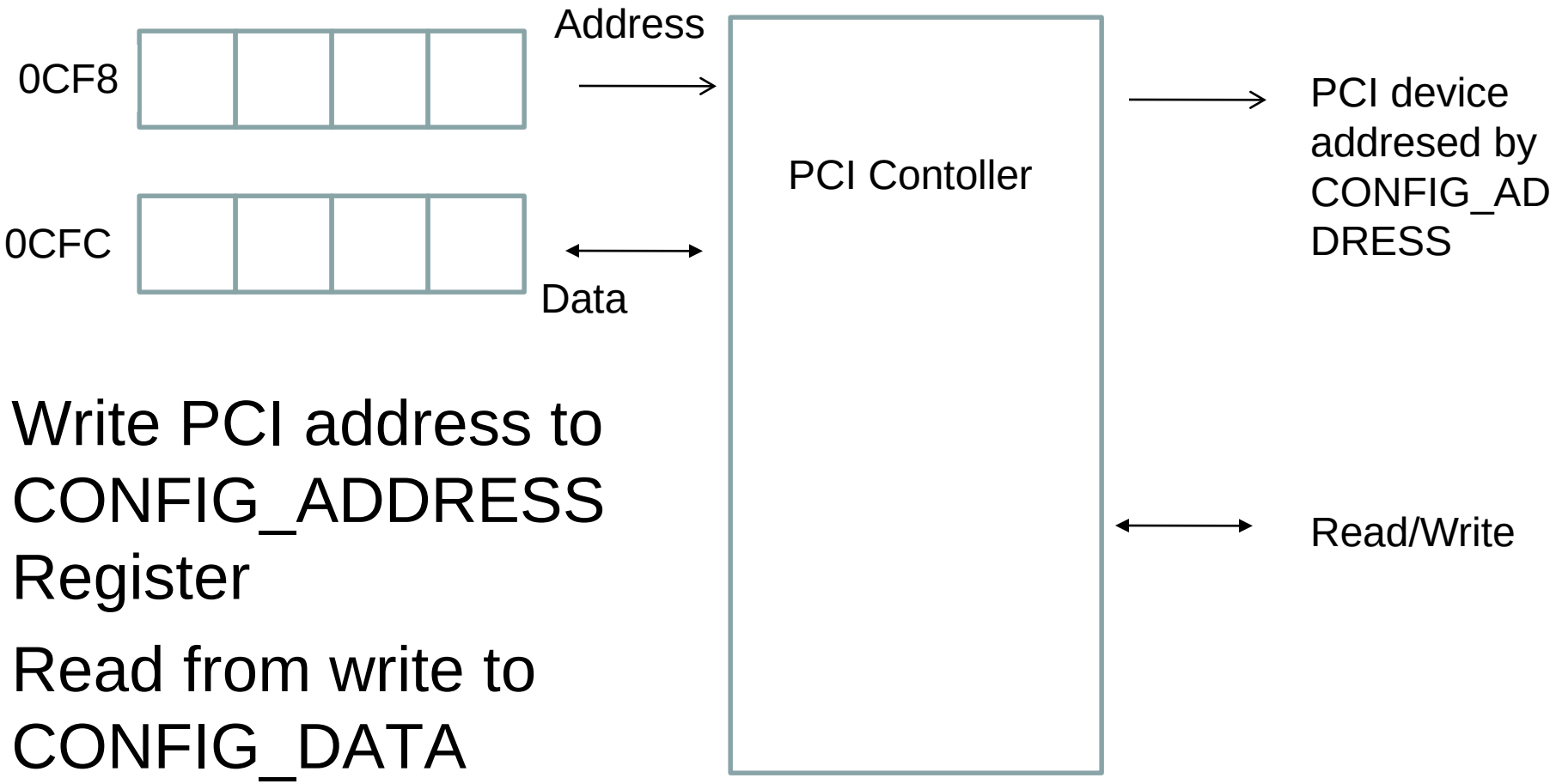


- First 64 are fixed header area. It include device identification data for driver loading such as
  - Manufacturer ID
    - allocated by PCI SIG
  - Unit ID, revision
    - identifies unit
  - Class code
    - type of PCI unit

I/O address of PCI bus

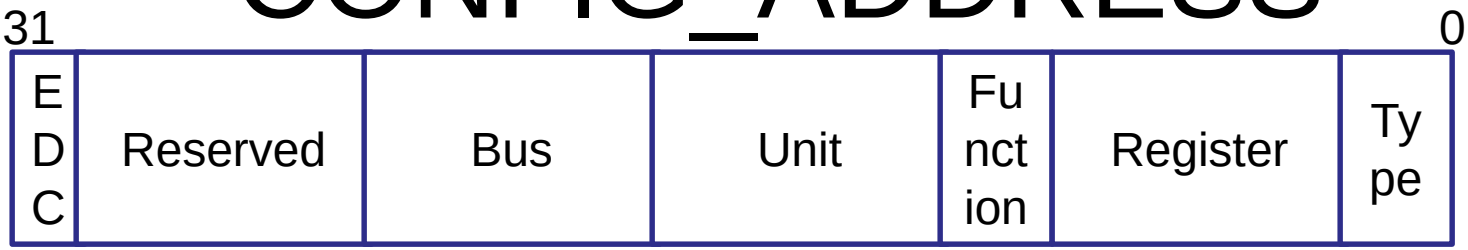
- It uses I/O address space of PC to read/write PCI configuration registers
- PC I/O address previously reserved for mother board are given to PCI configuration
  - 0CF8h - CONFIG_ADDRESS 32 bit
  - 0CFCh - CONFIG_DATA 32 bit
- These addresses do not conflict with ISA/EISA/MCA I/O address
- Write PCI address to CONFIG_ADDRESS Register
- Read from write to CONFIG_DATA Register

I/O address of PCI bus



- Write PCI address to CONFIG_ADDRESS Register
- Read from write to CONFIG_DATA Register

CONFIG_ADDRESS



- Register bit 2-7 64 possible registers in configuration area
- Function bit 8-10: 8 possible functions in multifunction device
- Units bit 11-15: One of 32 possible PCI Agents
- BUS bit 16-23: If several busses arrange in hierarchy (closest to CPU=0)
- EDC=0 Config data not activates
- Type 2 bits: Transfer type 00 Decode Unit (Read/Write content of the reg by decoding, 01 Value copy to ADX: Read /write as a single value

- Bus Arbitration
  - Parallel arbitration
  - Hidden arbitration
  - Arbitration algorithm is not defined
- DMA
  - Burst transfers
- Interrupts
  - INTA# activated
  - Data: interrupt vector

Bus Cycles

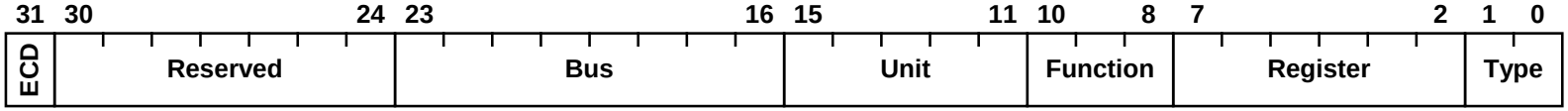
- INTA sequence (0000)
- special cycle (0001)
- I/O read access (0010)
- I/O write access (0011)
- memory read access (0110)
- memory write access (0111)
- configuration read access (1010)
- configuration write access (1011)
- memory multiple read access (1100)
- dual addressing cycle (1101)
- line memory read access (1110)
- memory write access with invalidation (1111)

Status and Command Registers

- Status:
  - PER: Parity error
  - SER: System error
  - MAB: Master abort
  - TAB: Target abort received
  - STA: Target abort signaled
  - DEVTIM: DEVSEL timing
    - 00=fast 01=medium 10=slow 11=reserved
  - DP: Data parity error
  - FBB: Fast back-to-back cycles supported/unsupported
- Command:
  - BEE: Fast back-to-back cycles (Back-to-Back Enable)
  - SEE: SERR Enable
  - WC: Wait cycle control
  - PER: Parity error (Parity Error Response)
  - VPS: VGA palette snoop
  - MWI: Memory write access with invalidation
  - SC: Special cycle
  - BM: Busmaster
  - MAR: Activate/deactivate Memory address area
  - IOR: Activate/deactivate I/O address area

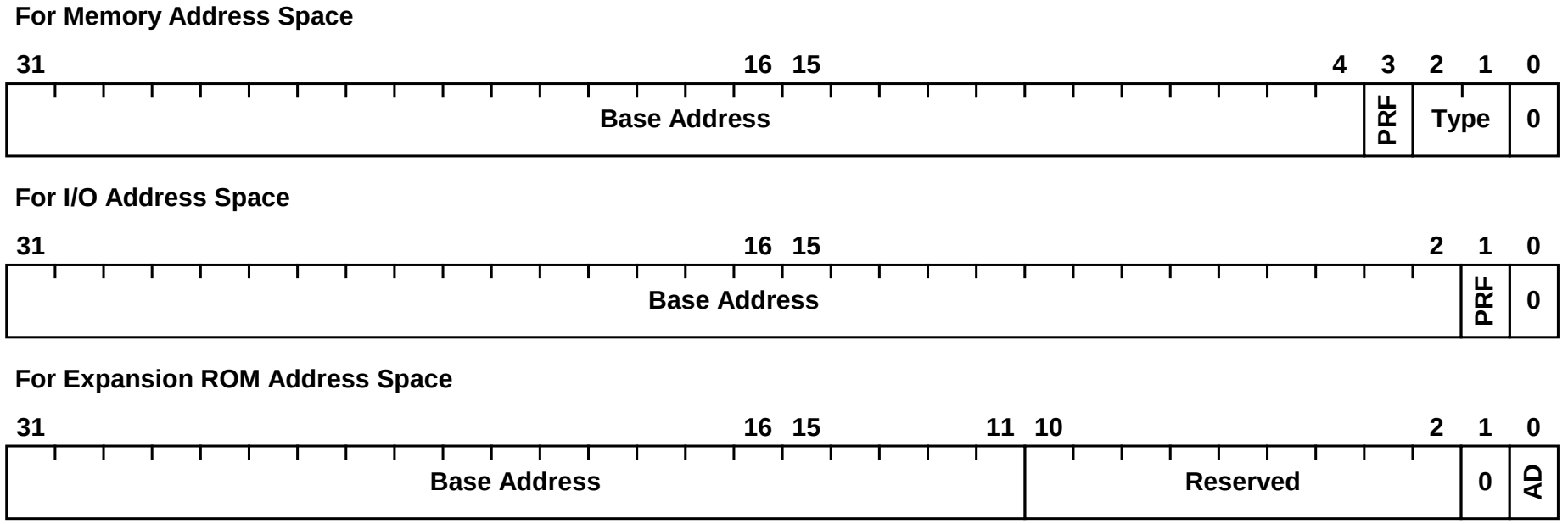
Accessing Configuration Address Space

- Configuration Mechanism #1
  - CONFIG-ADDRESS (0cf8h) and CONFIG-DATA (0cfch) registers are defined in the I/O area



- Configuration Mechanism #2 (for PC systems)
  - 4k I/O address range between c000h and ccffh

Base Address Registers



- PRF: Prefetching not possible/prefetching possible
- Type: Positioning type
  - 00=any 32-bit address, 01=less than 1M, 10=any 64-bit address, 11=reserved
- AD: Address decoding and expansion ROM deactivated/activated