Serial Communication

Kamalanath Samarakoon

Characteristic Directions

- Full duplex

- Half duplex
- Simplex

Number of devices connected
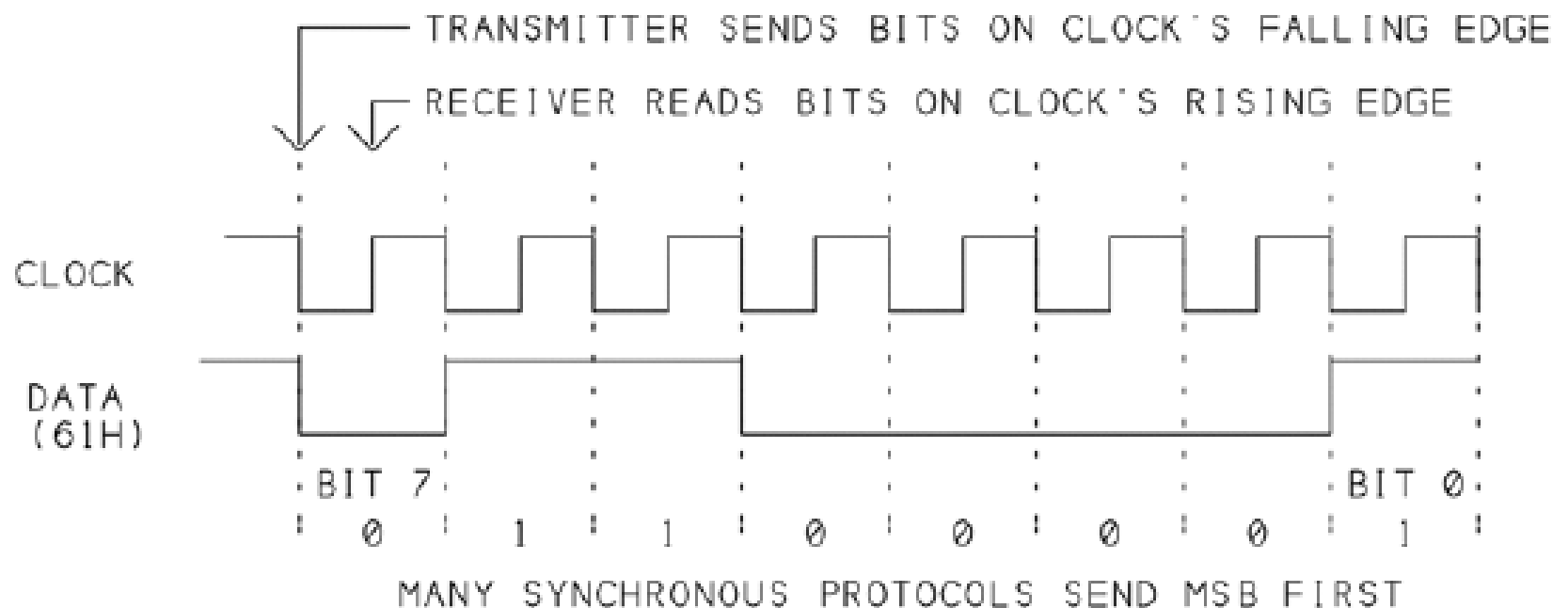
- Point to point
- Multidrop

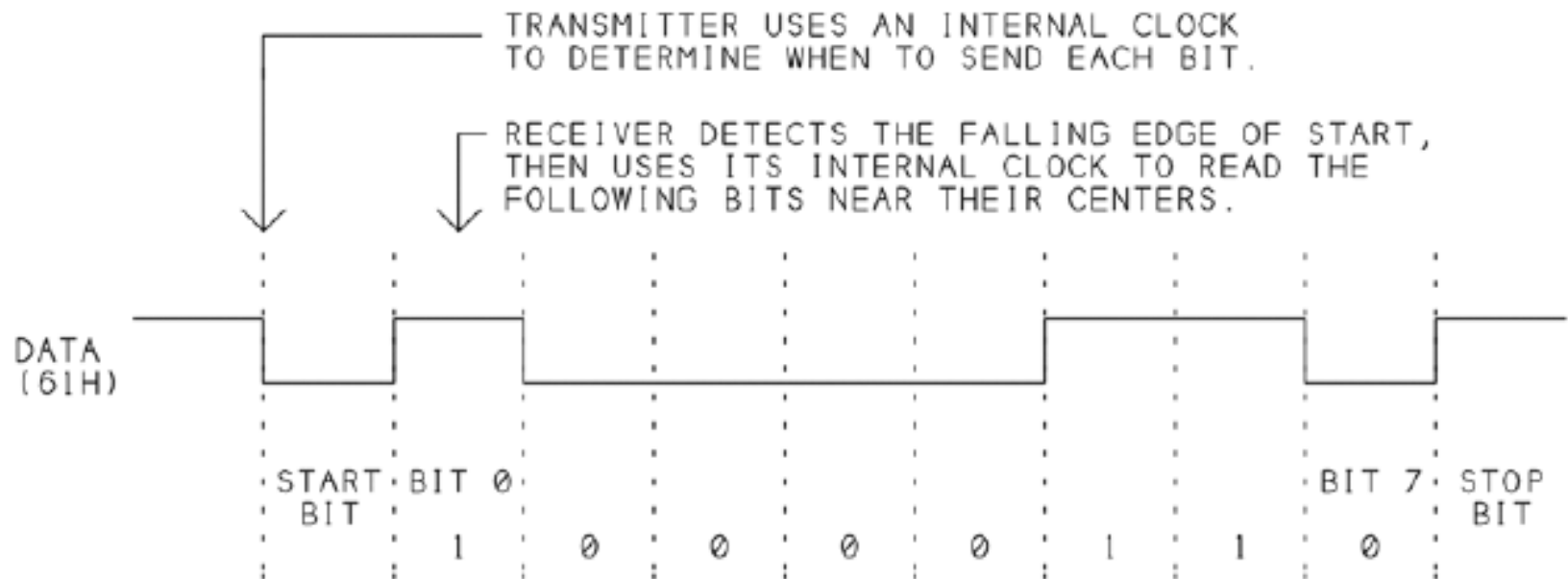# Formats

- Synchronous
- Asynchronous

Synchronous communication

(A) SYNCHRONOUS TRANSMISSION

TRANSMITTER SENDS BITS ON CLOCK'S FALLING EDGE

RECEIVER READS BITS ON CLOCK'S RISING EDGE

CLOCK

DATA
(61H)

BIT 7   BIT 0
0   1   1   0   0   0   0   1

MANY SYNCHRONOUS PROTOCOLS SEND MSB FIRST

Asynchronous communication

(B) ASYNCHRONOUS TRANSMISSION

TRANSMITTER USES AN INTERNAL CLOCK
TO DETERMINE WHEN TO SEND EACH BIT.

RECEIVER DETECTS THE FALLING EDGE OF START,
THEN USES ITS INTERNAL CLOCK TO READ THE
FOLLOWING BITS NEAR THEIR CENTERS.

DATA
(61H)

START BIT 0   BIT 7 STOP
BIT   BIT
      1   0   0   0   0   1   1   0

ASYNCHRONOUS PROTOCOLS SEND LSB FIRST

Add parity for error detecting

1 8 N 1 = 8N1   1 7 E 1 = 7E1

Signal

- Single ended
- Differential

Line termination

Serial communication protocols

- Slow
  - RS 232
  - RS485
- Fast
  - USB
  - I^{2}C (IEEE 1384)
  - FireWire

RS232

- Most popular interface before USB
- Was available in almost all computer to mainframe
- Advantages
  - Was commonly available
  - Can do that USB could not
  - Less number of wires compared to parallel
  - Inexpensive
  - Very long cable (50 ft max)/USB 16ft // 10-15 ft
  - 3 wires to communicate (Unlike parallel)

RS232

- Disadvantages
  - Cannot connect more than two devices
  - Max speed 20,000 bits/s
  - Very long lines need differential interface (RS485)

RS232 Evolution

- Originally
  - PC to dumb terminal
- Then
  - PC to Internet
- Also PC to
  - Mouse
  - Printer
  - Another PC
  - Microcontroller

RS232

- RS (Recommended Standard)
- Standard is – EIA 232F (Electronic Industry Association)
- This standard defines
  - Names and functions of signals
  - Electrical Characteristic of signals
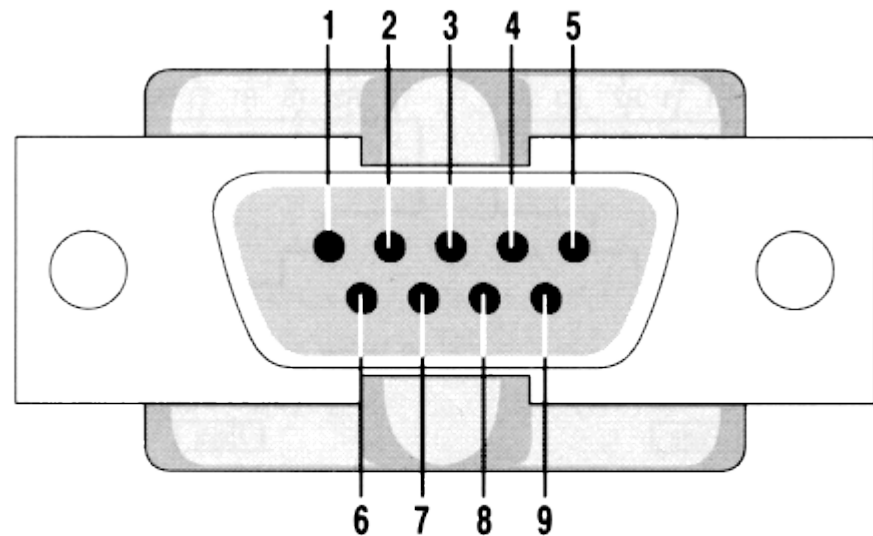 - Mechanical standard (size, shape pin assignment)

RS232

- 25 pins or 9 pins
- Logic 0 +3 to +25 V
- Logic 1 -3 to -25 V
- - 3 to +3 V undefined
- O/C V <25 V w.r.t to Ground
- S/C   I 500mA driver should be able to drive
- Max speed 20,000 bps for 50 ft

Connectors RS232 – 9 pin

- Equipment
  - Female
- Cable
  - Male

Pin	Signal	Pin	Signal
1	Data Carrier Detect	6	Data Set Ready
2	Received Data	7	Request to Send
3	Transmitted Data	8	Clear to Send
4	Data Terminal Ready	9	Ring Indicator
5	Signal Ground		

RS-232 Interface

RS-232 (EIA Std.) applicable to the 25 pin interconnection of Data Terminal Equipment (DTE) and Data Communications Equipment (DCE) using serial binary data
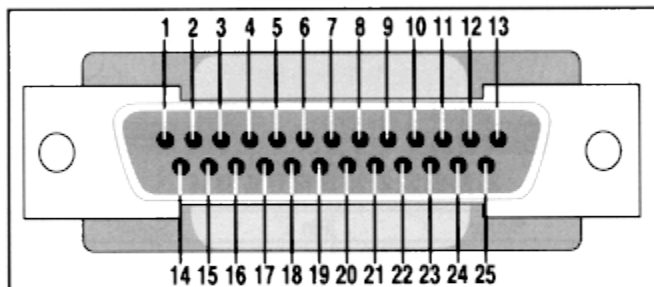

| Pin	Description	EIA CKT	From DCE	To DCE
1	Frame Ground	AA		
2	Transmitted Data	BA		D (Data)
3	Received Data	BB	D	
4	Request to Send	CA		C (Control)
5	Clear to Send	CB	C	
6	Data Set Ready	CC	C	
7	Signal Gnd/Common Return	AB		
8	Rcvd. Line Signal Detector	CF	C	
11	Undefined			
12	Secondary Rcvd. Line Sig. Detector	SCF	C	
13	Secondary Clear to Send	SCB	C	
14	Secondary Transmitted Data	SBA		D
15	Transmitter Sig. Element Timing	DB	T (Timing)	
16	Secondary Received Data	SBB	D	
17	Receiver Sig. Element Timing	DD	T	
18	Undefined			
19	Secondary Request to Send	SCA		C
20	Data Terminal Ready	CD		C
21	Sig. Quality Detector	CG		C
22	Ring Indicator	CE	C	
23	Data Sig. Rate Selector (DCE)	CI	C	
23	Data Sig. Rate Selector (DTE)	CH		C
24	Transmitter Sig. Element Timing	DA		T
25	Undefined			

Standard 9 to 25 pin cable layout for async data on a PC AT serial cable

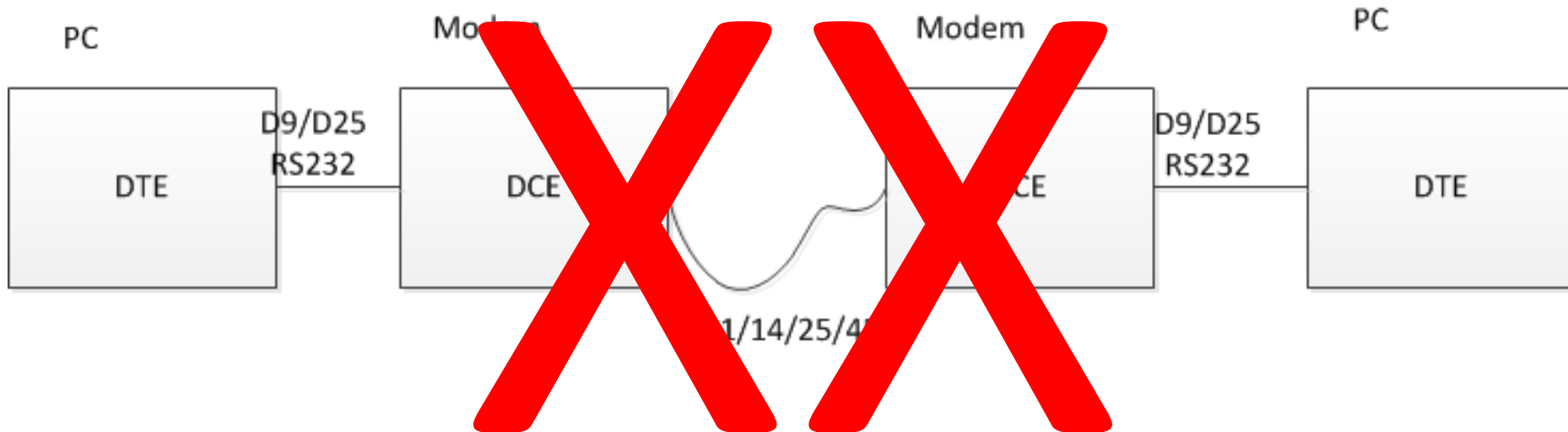| Description	Signal	9-pin DTE	25-pin DCE	Source DTE or DCE
Carrier Detect	CD	1	8	from Modem
Receive Data	RD	2	3	from Modem
Transmit Data	TD	3	2	from Terminal/Computer
Data Terminal Ready	DTR	4	20	from Terminal/Computer
Signal Ground	SG	5	7	from Modem
Data Set Ready	DSR	6	6	from Modem
Request to Send	RTS	7	4	from Terminal/Computer
Clear to Send	CTS	8	5	from Modem
Ring Indicator	RI	9	22	from Modem

Link
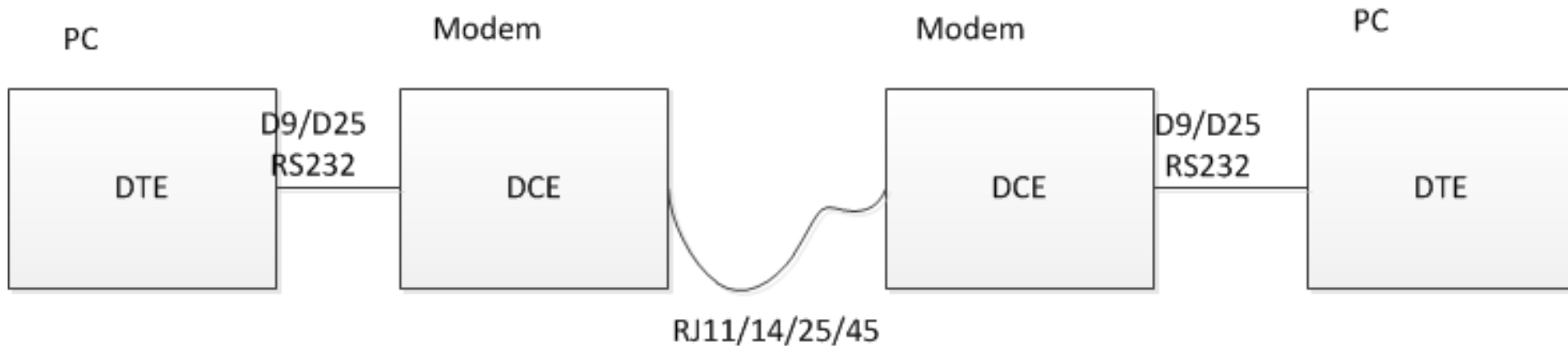
- RJ Registered Jack of Universal service ordering code
- RJ 11   6 points middle 2 connected
- RJ 14   6 points middle 4 connected
- RJ 25   6 points middle 6 connected
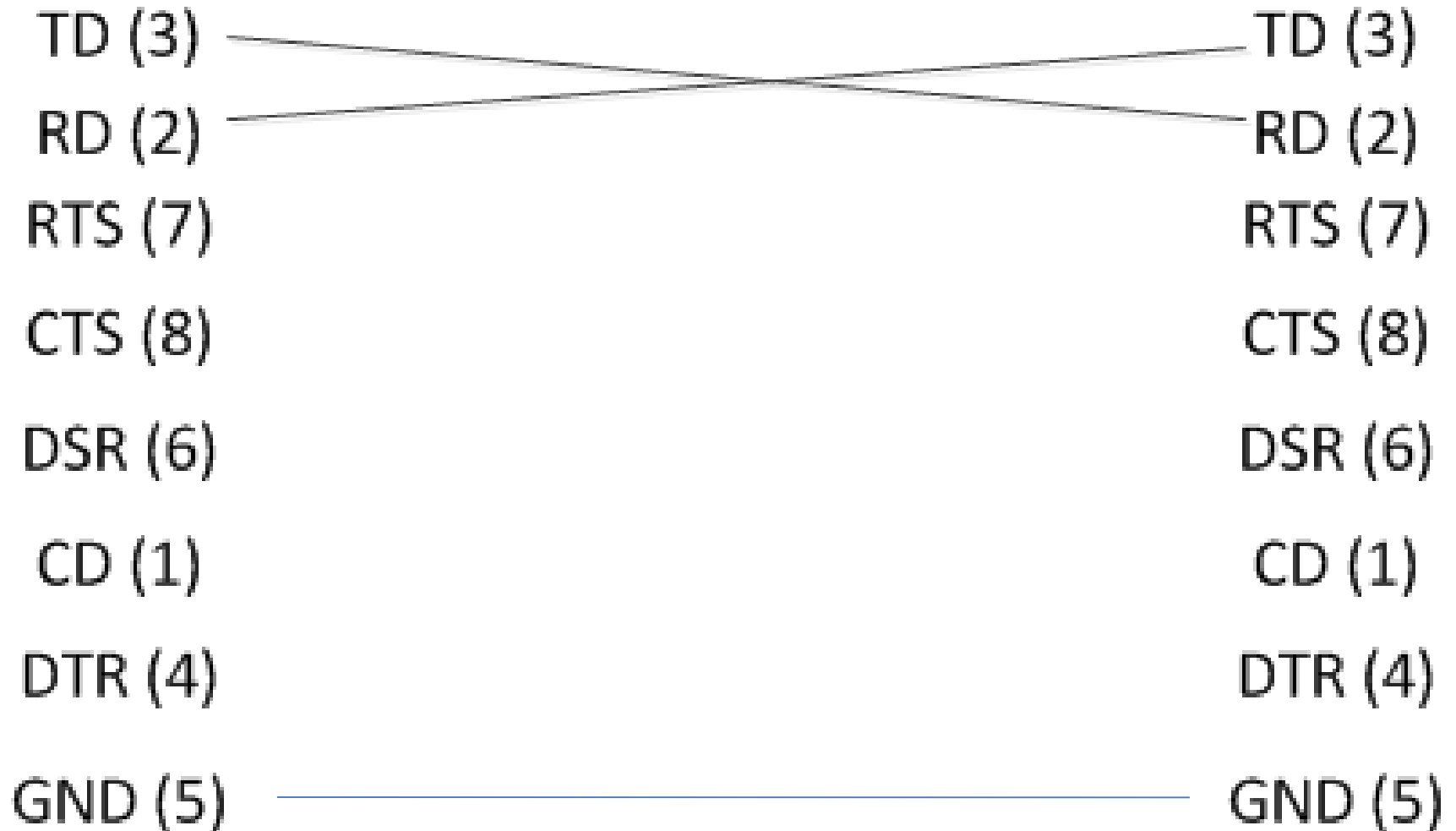- RJ 45   8 points
-
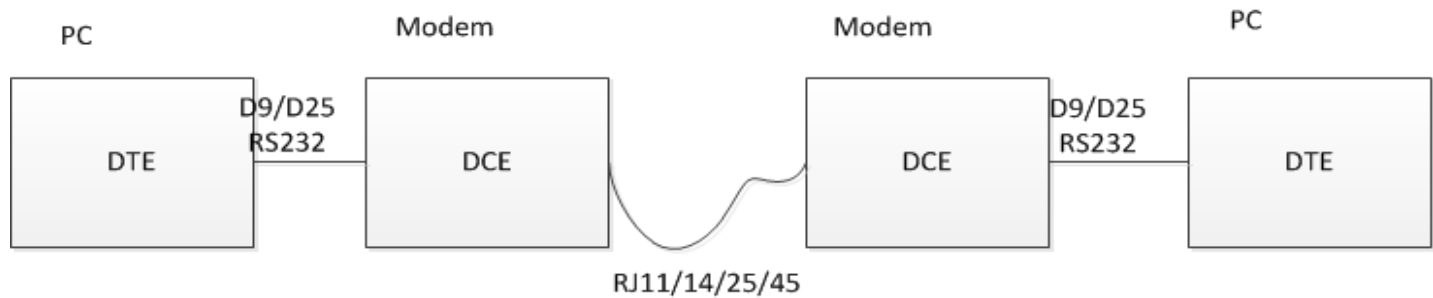
Full Name	Function	
TD	Transmit Data	Serial Data Output (TXD)
RD	Receive Data	Serial Data Input (RXD)
CTS	Clear to Send	This line indicates that the Modem is ready to exchange data.
DCD	Data Carrier Detect	When the modem detects a "Carrier" from the modem at the other end of the phone line, this Line becomes active.
DSR	Data Set Ready	This tells the UART that the modem is ready to establish a link.
DTR	Data Terminal Ready	This is the opposite to DSR. This tells the Modem that the UART is ready to link.
RTS	Request To Send	This line informs the Modem that the UART is ready to exchange data.
RI	Ring Indicator	Goes active when modem detects a ringing signal from the PSTN.

Null Modem

No Handshake

TD (3)   TD (3)

RD (2)   RD (2)

RTS (7)   RTS (7)

CTS (8)   CTS (8)

DSR (6)   DSR (6)

CD (1)   CD (1)

DTR (4)   DTR (4)

GND (5)   GND (5)

Full Handshake

Loop back Handshake

TD (3)
RD (2)
RTS (7)
CTS (8)
DSR (6)
CD (1)
DTR (4)
GND (5)

TD (3)
RD (2)
RTS (7)
CTS (8)
DSR (6)
CD (1)
DTR (4)
GND (5)
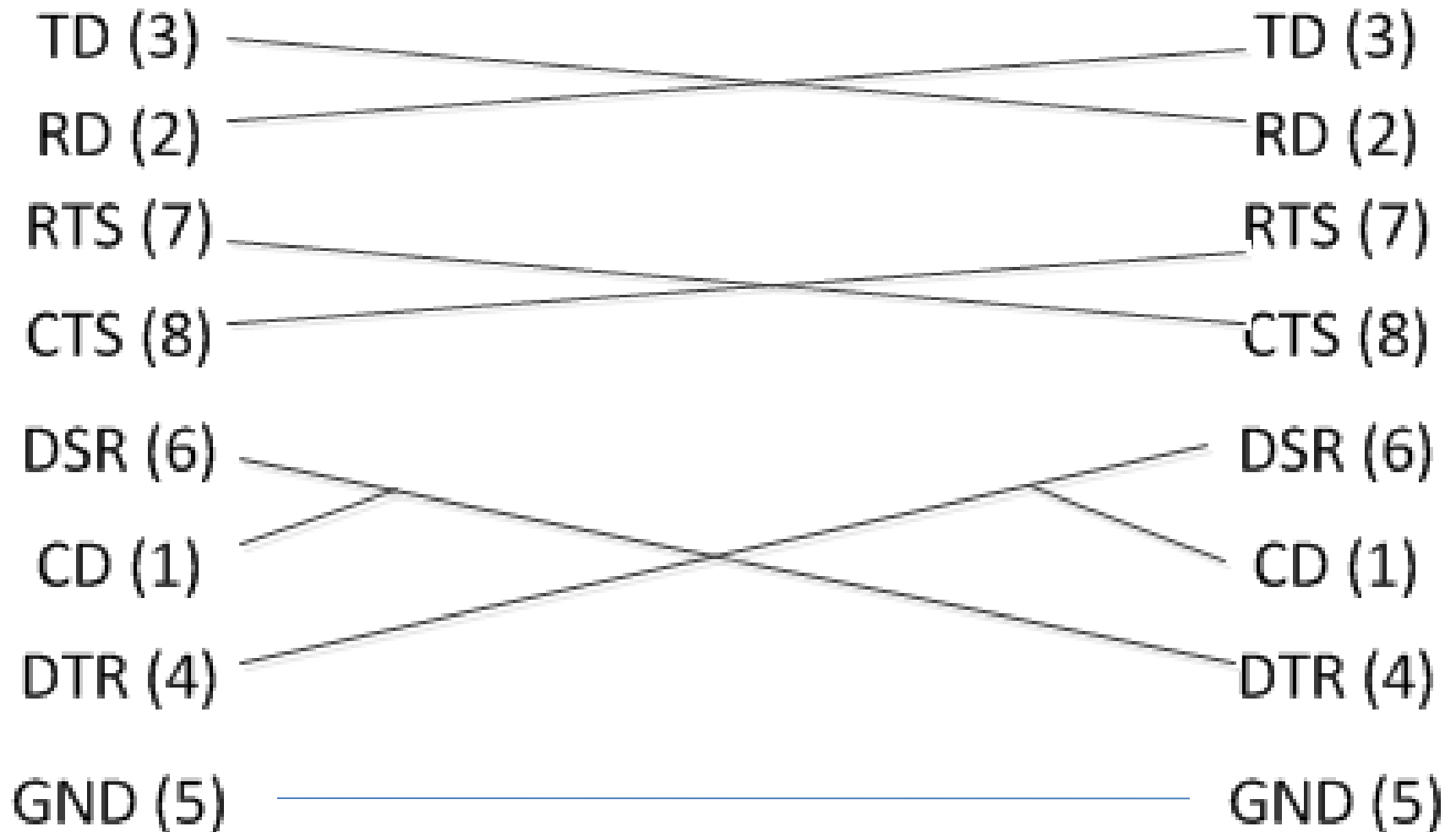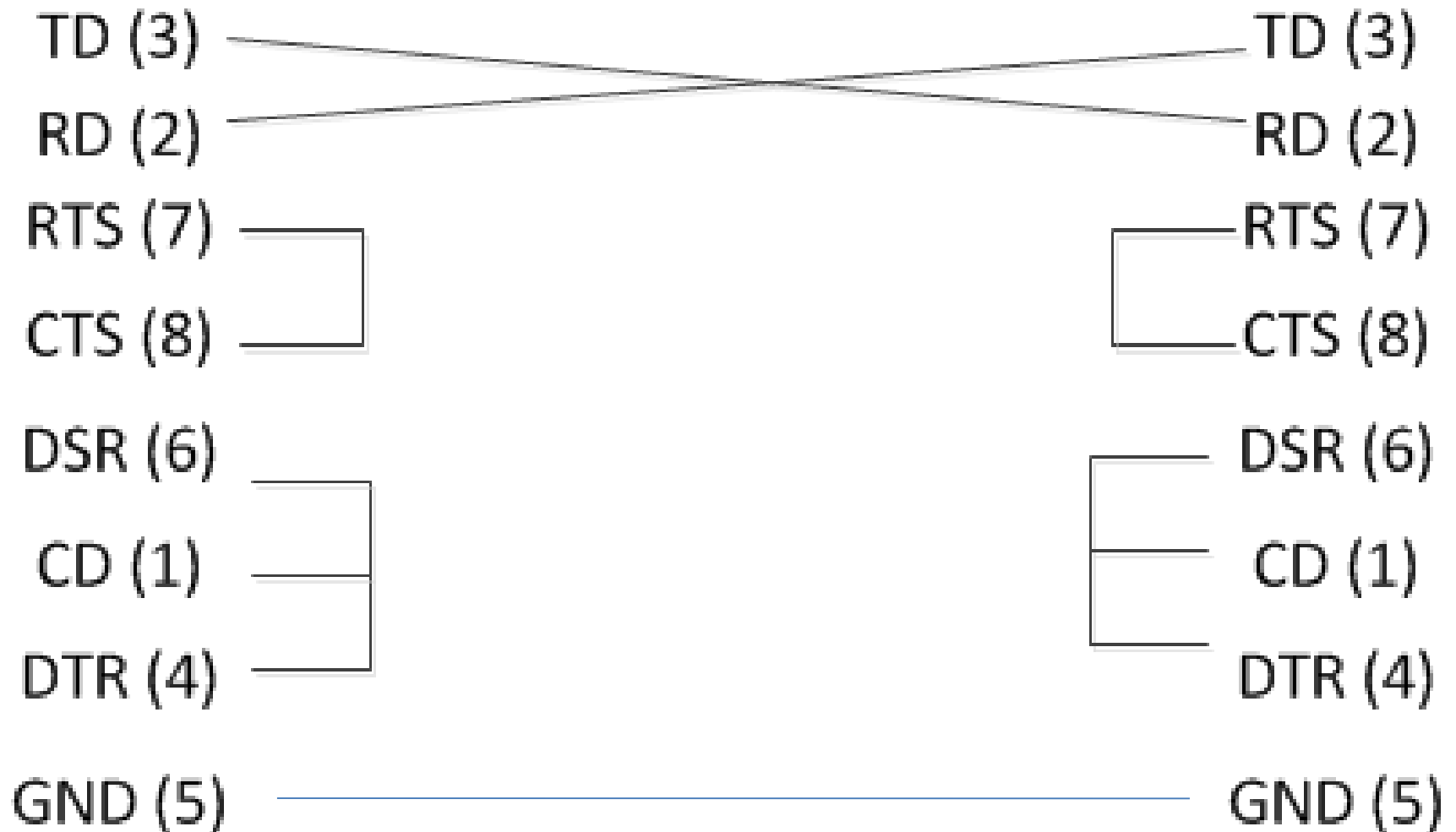
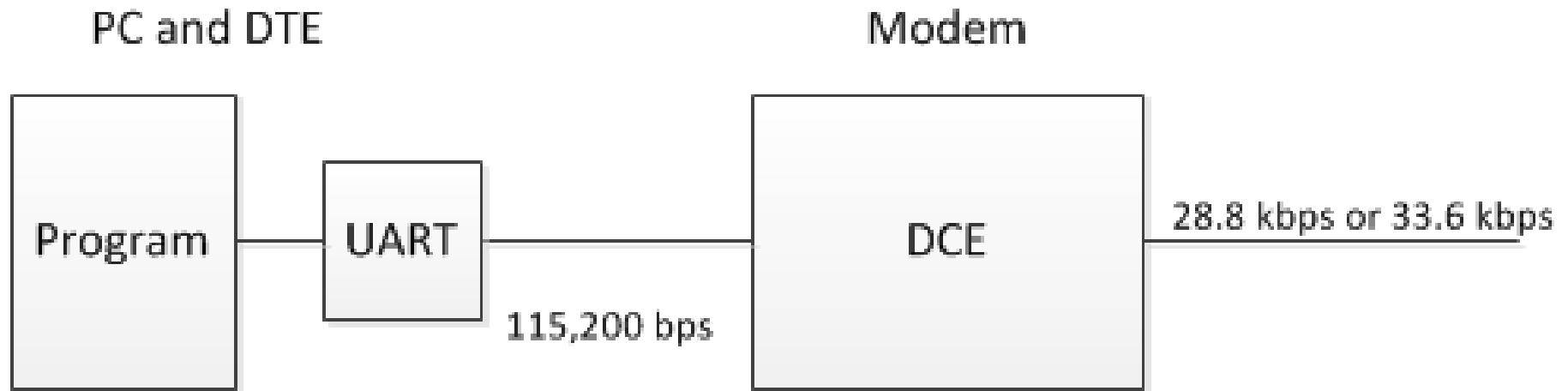# USART Universal Asynchronous Receiver/Transmitter

- IC Module inside the IC for serial communication

- Do parallel in PC to serial in RS232 conversion and back

- Supports Half duplex and Full Duplex

- Provide all standard RS232 handshaking and control lines

- 8250 57600 bps
- 16450   115200 bps
- 16550   16 Bytes FIFO Buffers
- 16650   32 Byte FIFO Buffers
- 16750   64 Byte FIFO Buffers 230,400 bps

Flow control

PC and DTE

Modem

```
┌───────────┐        ┌────────┐              ┌──────────────────┐
│           │        │        │              │                  │       28.8 kbps or 33.6 kbps
│  Program  │────────│  UART  │──────────────│       DCE        │────────────────────────────
│           │        │        │              │                  │
└───────────┘        └────────┘              └──────────────────┘
                              115,200 bps
```
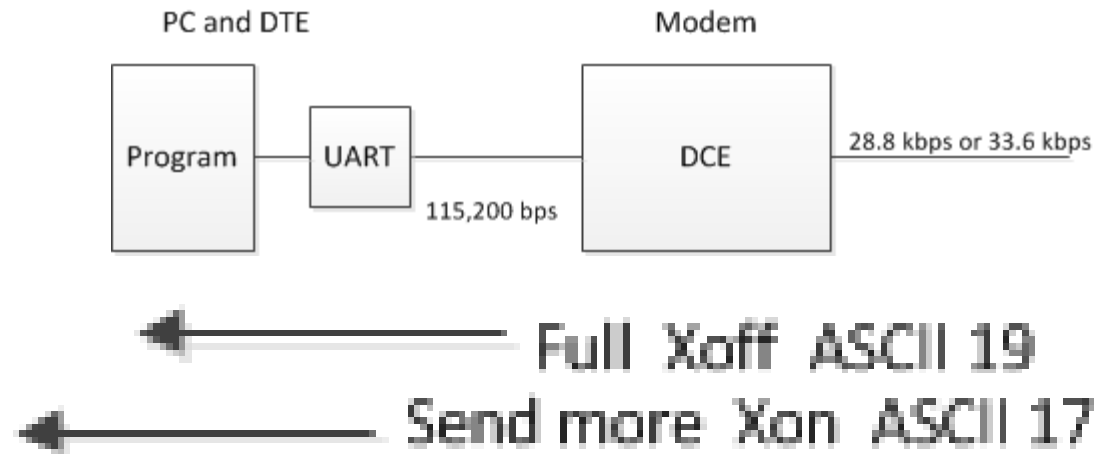
- Program should set 115,200 kbps and not 33.6 kbps as DCE do compressing

- DTE faster than DCE hence data can be lost

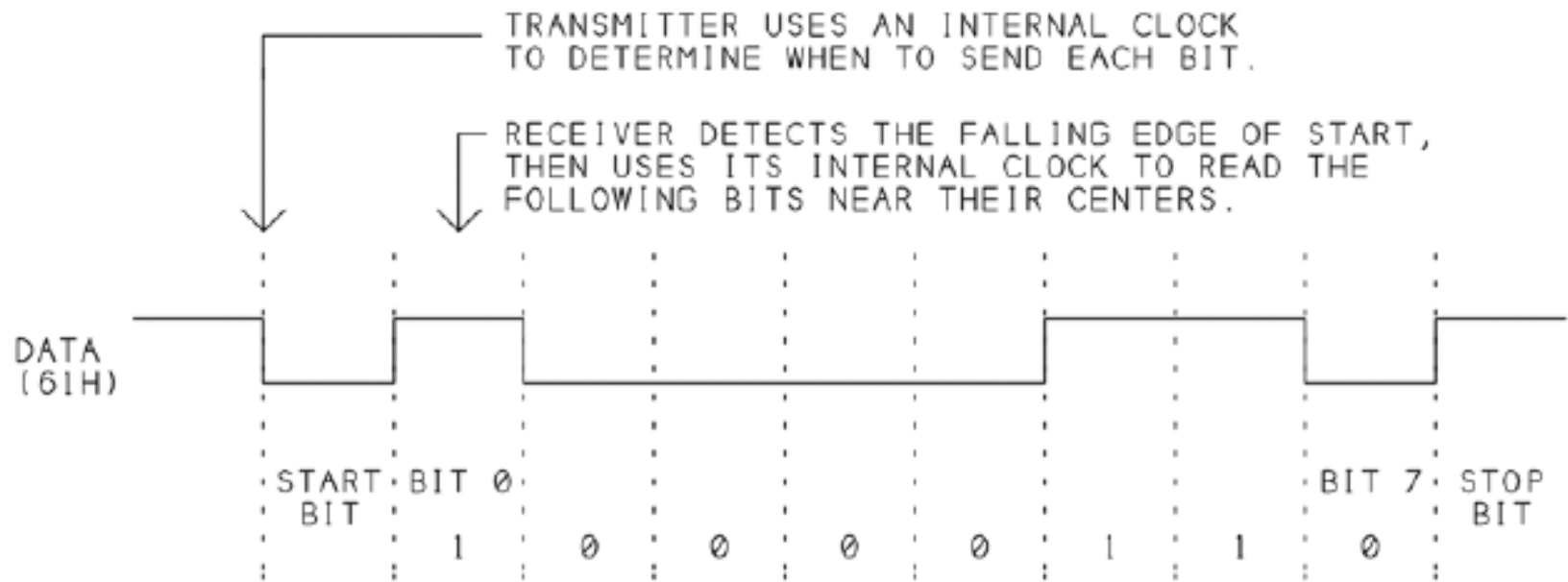- Hence use flow control

Flow control

- Software
- Xoff – Xon

- Hardware
  – Use RTS and DTS lines

Asynchronous communication

(B) ASYNCHRONOUS TRANSMISSION

TRANSMITTER USES AN INTERNAL CLOCK
TO DETERMINE WHEN TO SEND EACH BIT.

RECEIVER DETECTS THE FALLING EDGE OF START,
THEN USES ITS INTERNAL CLOCK TO READ THE
FOLLOWING BITS NEAR THEIR CENTERS.

DATA
(61H)

START BIT 0   BIT 7 STOP
BIT   BIT
      1   0   0   0   0   1   1   0

ASYNCHRONOUS PROTOCOLS SEND LSB FIRST

Add parity for error detecting

1 8 N 1 = 8N1   1 7 E 1 = 7E1

References

- Parallel port, Serial Port and USB
  - beyondlogic.org
  - http://retired.beyondlogic.org/spp/parallel.htm
- Jan Axelson
  - Parallel port complete
  - Serial port complete
  - USB complete

Asynchronous serial communication by USART

- UART uses clock that is 16 times bit frequency
- E.g. 300 bps 4800 Hz
- Detect start bit, wait 8, wait 16, read, wait 16, read...

```
TRANSMITTER CLOCK =
BIT RATE X 16

DATA OUT

RECEIVER CLOCK =
BIT RATE X 16

         ↑                    ↑                ↑
      DETECT          WAIT 24 CLOCK      WAIT 16 CLOCK
    START BIT         CYCLES TO READ      CYCLES TO
                      FIRST  DATA BIT     READ EACH
                                         FOLLOWING BIT

DATA IN                       1                 0
```
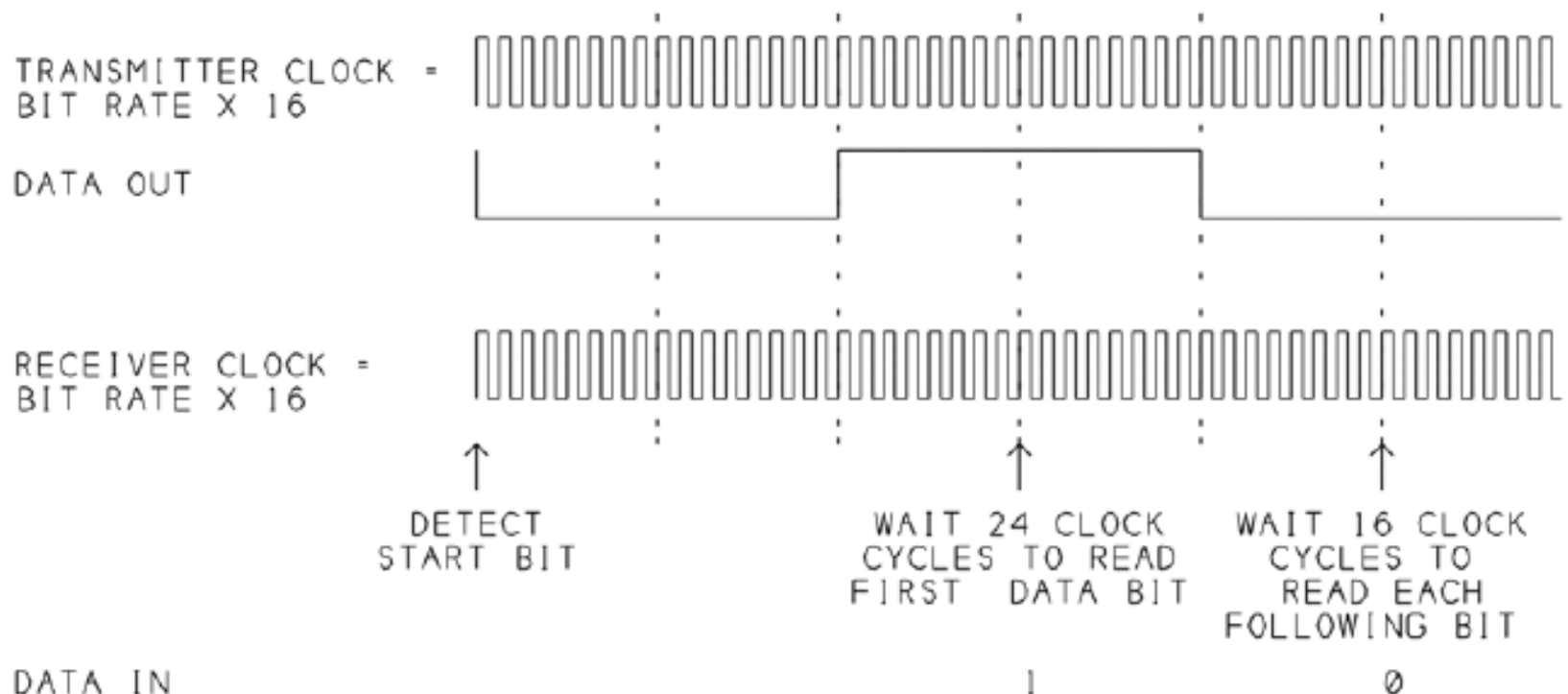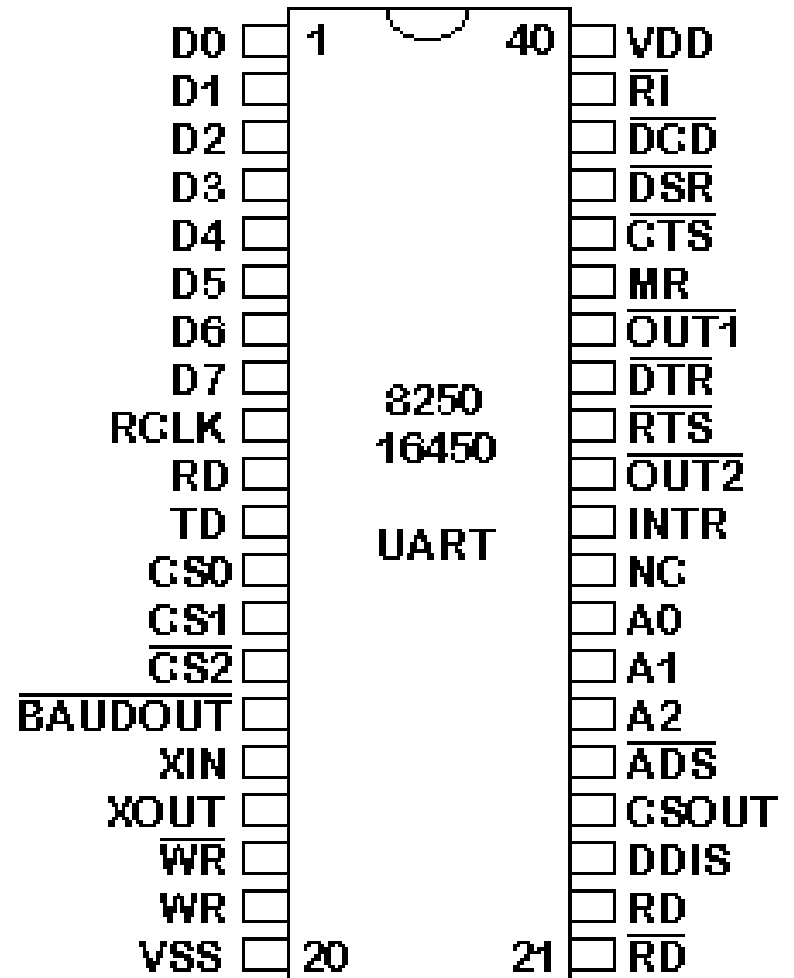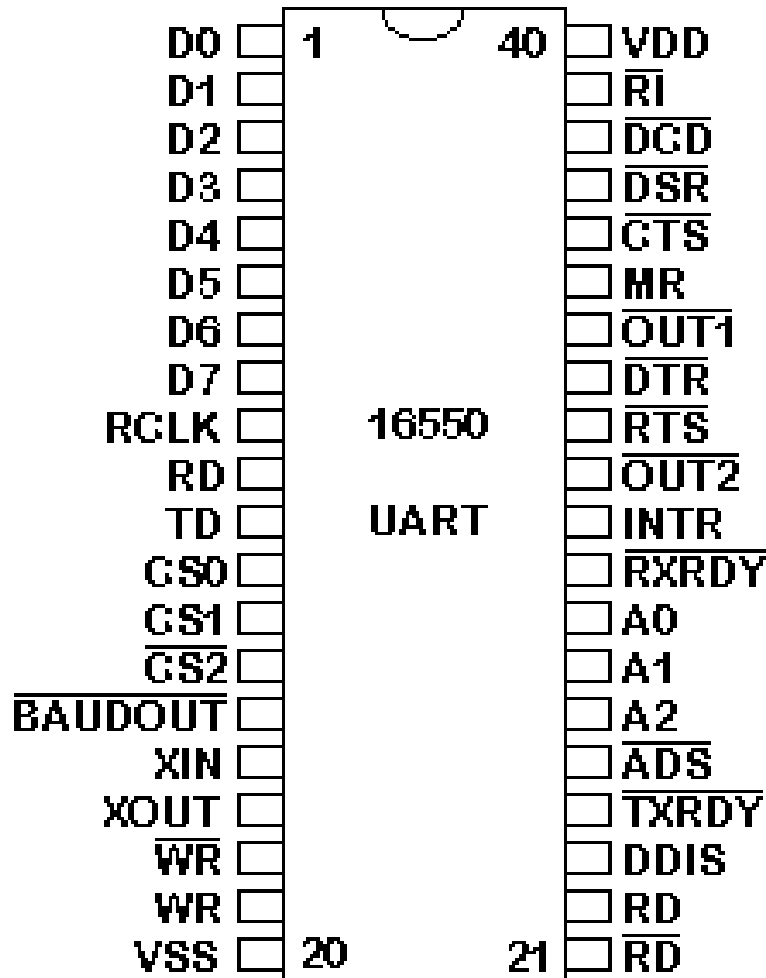
Calculation of bit rate

- In PC UART cock rate is 1.8432 MHz
- Calculate maximum bit rate

Quiz

- In PC UART cock rate is 1.8432 MHz
- Calculate maximum bit rate

- If bit rate is 9600bps   1200 bytes

- How many bytes it can transmit per second?

- How many data bytes it can transmit per second when data format is 7E1?
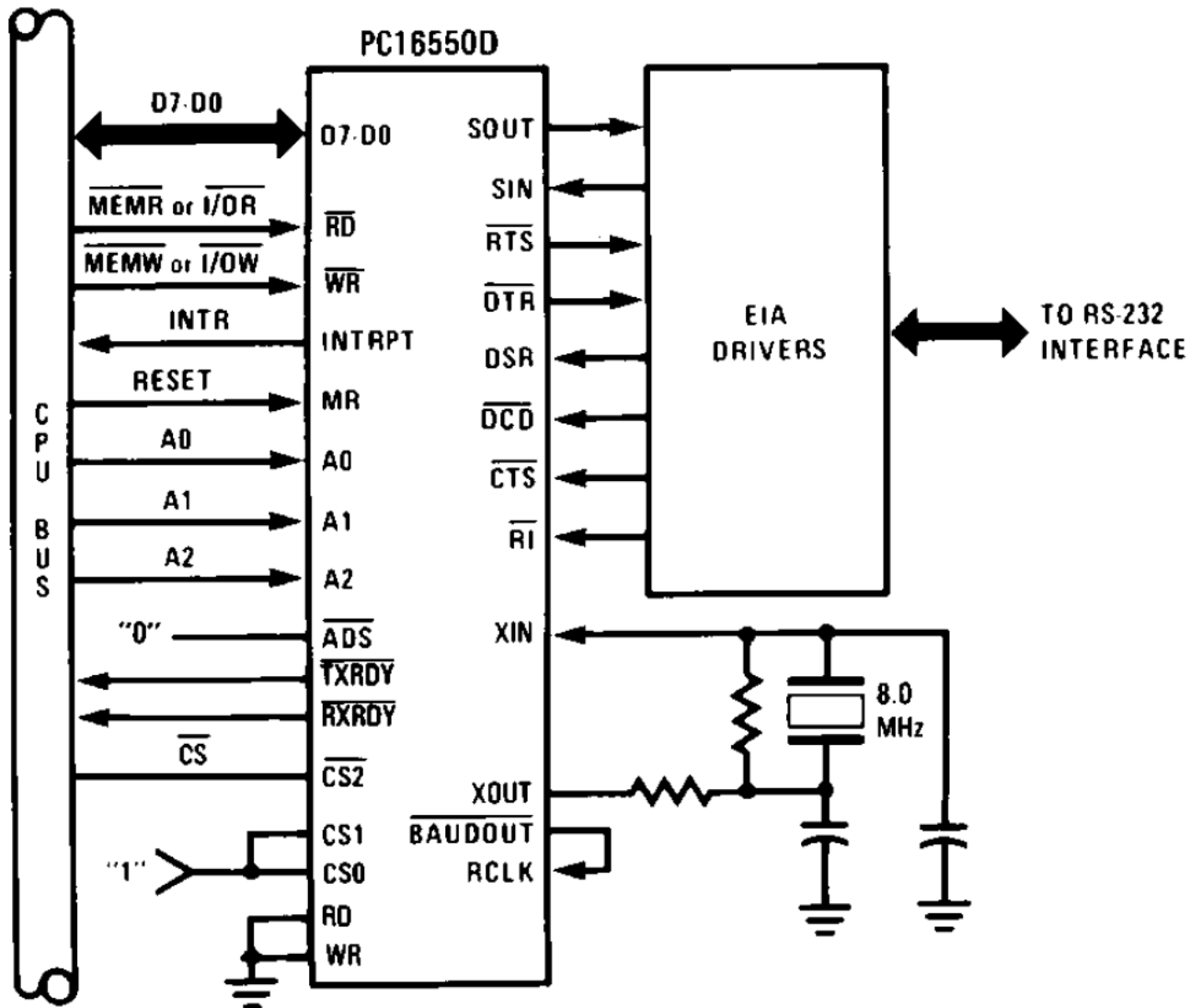   960 bytes

16550 UART

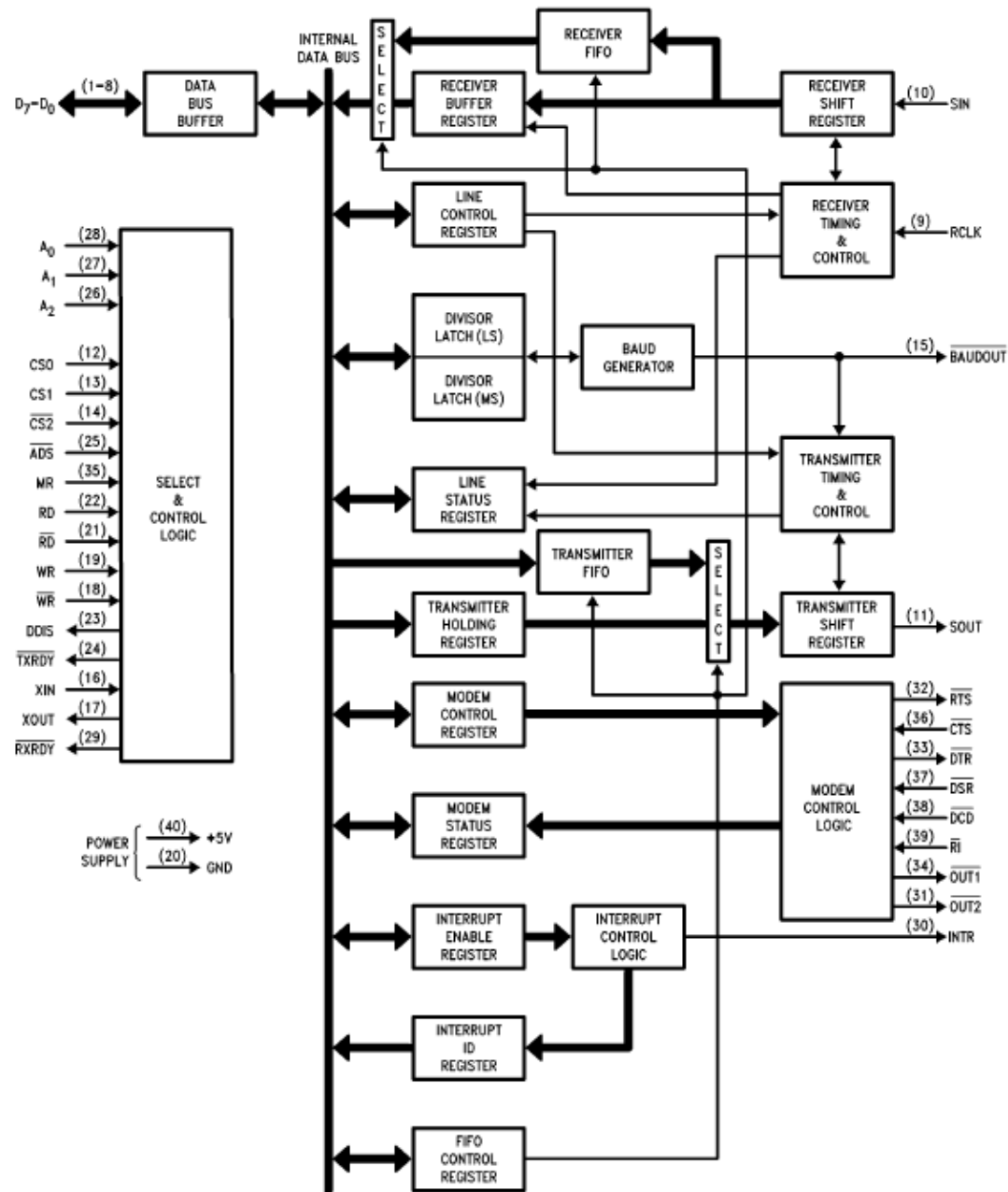| Left chip (16550 UART)			Right chip (8250/16450 UART)	
D0 — 1	40 — VDD		D0 — 1	40 — VDD
D1	RI		D1	RI
D2	DCD		D2	DCD
D3	DSR		D3	DSR
D4	CTS		D4	CTS
D5	MR		D5	MR
D6	OUT1		D6	OUT1
D7	DTR		D7	DTR
RCLK	RTS		RCLK	RTS
RD	OUT2		RD	OUT2
TD	INTR		TD	INTR
CS0	RXRDY		CS0	NC
CS1	A0		CS1	A0
CS2	A1		CS2	A1
BAUDOUT	A2		BAUDOUT	A2
XIN	ADS		XIN	ADS
XOUT	TXRDY		XOUT	CSOUT
WR	DDIS		WR	DDIS
WR	RD		WR	RD
VSS — 20	21 — RD		VSS — 20	21 — RD

16550 UART

8250 16450 UART

Block diagram

- PC Bus side
  - Data lines
  - Read and Write control
  - Interrupt control
  - Reset
  - Address Lines
- RS232 side
- Clock

UART

5.0 Block Diagram

D_7–D_0 (1–8) — DATA BUS BUFFER

INTERNAL DATA BUS

SELECT — RECEIVER FIFO

RECEIVER BUFFER REGISTER

RECEIVER SHIFT REGISTER — (10) SIN

LINE CONTROL REGISTER

RECEIVER TIMING & CONTROL — (9) RCLK

A_0 (28)
A_1 (27)
A_2 (26)

CS0 (12)
CS1 (13)
$\overline{CS2}$ (14)
$\overline{ADS}$ (25)
MR (35)
RD (22)
$\overline{RD}$ (21)
WR (19)
$\overline{WR}$ (18)
DDIS (23)
$\overline{TXRDY}$ (24)
XIN (16)
XOUT (17)
$\overline{RXRDY}$ (29)

SELECT & CONTROL LOGIC

DIVISOR LATCH (LS)

DIVISOR LATCH (MS)

BAUD GENERATOR — (15) $\overline{BAUDOUT}$

LINE STATUS REGISTER

TRANSMITTER TIMING & CONTROL

TRANSMITTER FIFO

SELECT

TRANSMITTER HOLDING REGISTER

TRANSMITTER SHIFT REGISTER — (11) SOUT

MODEM CONTROL REGISTER

POWER SUPPLY (40) +5V
(20) GND

MODEM STATUS REGISTER

MODEM CONTROL LOGIC
(32) $\overline{RTS}$
(36) $\overline{CTS}$
(33) $\overline{DTR}$
(37) $\overline{DSR}$
(38) $\overline{DCD}$
(39) $\overline{RI}$
(34) $\overline{OUT1}$
(31) $\overline{OUT2}$

INTERRUPT ENABLE REGISTER

INTERRUPT CONTROL LOGIC — (30) INTR

INTERRUPT ID REGISTER

FIFO CONTROL REGISTER

TL/C/8652–16

Registers

- Addresses = Base +7

- 12 registers some read and some write and R/W using DLAB (Devisor Latch Access Bit)

Registers

Base Address	DLAB	Read/Write	Abr.	Register Name
+ 0	=0	Write	-	Transmitter Holding Buffer
	=0	Read	-	Receiver Buffer
	=1	Read/Write	-	Divisor Latch Low Byte
+ 1	=0	Read/Write	IER	Interrupt Enable Register
	=1	Read/Write	-	Divisor Latch High Byte
+ 2	-	Read	IIR	Interrupt Identification Register
	-	Write	FCR	FIFO Control Register
+ 3	-	Read/Write	LCR	Line Control Register
+ 4	-	Read/Write	MCR	Modem Control Register
+ 5	-	Read	LSR	Line Status Register
+ 6	-	Read	MSR	Modem Status Register
+ 7	-	Read/Write	-	Scratch Register

DLAByte

Speed (BPS)	Divisor (Dec)	Divisor Latch High Byte	Divisor Latch Low Byte	
50	2304	09h	00h	
300	384	01h	80h	
600	192	00h	C0h	
2400	48	00h	30h	
4800	24	00h	18h	
9600	12	00h	0Ch	
19200	6	00h	06h	
38400	3	00h	03h	
57600	2	00h	02h	
115200	1	00h	01h	

LCR: Line Control Register

Bit 7	1	Divisor Latch Access Bit		
	0	Access to Receiver buffer, Transmitter buffer & Interrupt Enable Register		
Bit 6	Set Break Enable			
Bits 3, 4 And 5	Bit 5	Bit 4	Bit 3	Parity Select
	X	X	0	No Parity
	0	0	1	Odd Parity
	0	1	1	Even Parity
	1	0	1	High Parity (Sticky)
	1	1	1	Low Parity (Sticky)
Bit 2	Length of Stop Bit			
	0	One Stop Bit		
	1	2 Stop bits for words of length 6,7 or 8 bits or 1.5 Stop Bits for Word lengths of 5 bits.		
Bits 0 And 1	Bit 1	Bit 0	Word Length	
	0	0	5 Bits	
	0	1	6 Bits	
	1	0	7 Bits	
	1	1	8 Bits	

MCR: Modem Control Register

Bit	Notes
Bit 7	Reserved
Bit 6	Reserved
Bit 5	Autoflow Control Enabled (16750 only)
Bit 4	LoopBack Mode
Bit 3	Aux Output 2
Bit 2	Aux Output 1
Bit 1	Force Request to Send
Bit 0	Force Data Terminal Ready

Modem Status Register

Bit	Notes
Bit 7	Carrier Detect
Bit 6	Ring Indicator
Bit 5	Data Set Ready
Bit 4	Clear To Send
Bit 3	Delta Data Carrier Detect
Bit 2	Trailing Edge Ring Indicator
Bit 1	Delta Data Set Ready
Bit 0	Delta Clear to Send

LSR: Line Status Register

Bit	Notes
Bit 7	Carrier Detect
Bit 6	Ring Indicator
Bit 5	Data Set Ready
Bit 4	Clear To Send
Bit 3	Delta Data Carrier Detect
Bit 2	Trailing Edge Ring Indicator
Bit 1	Delta Data Set Ready
Bit 0	Delta Clear to Send

IER: Interrupt Enable Register

Bit	Notes
Bit 7	Reserved
Bit 6	Reserved
Bit 5	Enables Low Power Mode (16750)
Bit 4	Enables Sleep Mode (16750)
Bit 3	Enable Modem Status Interrupt
Bit 2	Enable Receiver Line Status Interrupt
Bit 1	Enable Transmitter Holding Register Empty Interrupt
Bit 0	Enable Received Data Available Interrupt

IIR: Interrupt Identification Register

Bit	Notes		
Bits 6 and 7	Bit 6	Bit 7	
	0	0	No FIFO
	0	1	FIFO Enabled but Unusable
	1	1	FIFO Enabled
Bit 5	64 Byte Fifo Enabled (16750 only)		
Bit 4	Reserved		
Bit 3	0	Reserved on 8250, 16450	
	1	16550 Time-out Interrupt Pending	
Bits 1 and 2	Bit 2	Bit 1	
	0	0	Modem Status Interrupt
	0	1	Transmitter Holding Register Empty Interrupt
	1	0	Received Data Available Interrupt
	1	1	Receiver Line Status Interrupt
Bit 0	0	Interrupt Pending	
	1	No Interrupt Pending	

Interfacing RS232 to TTL logic levels

- RS232

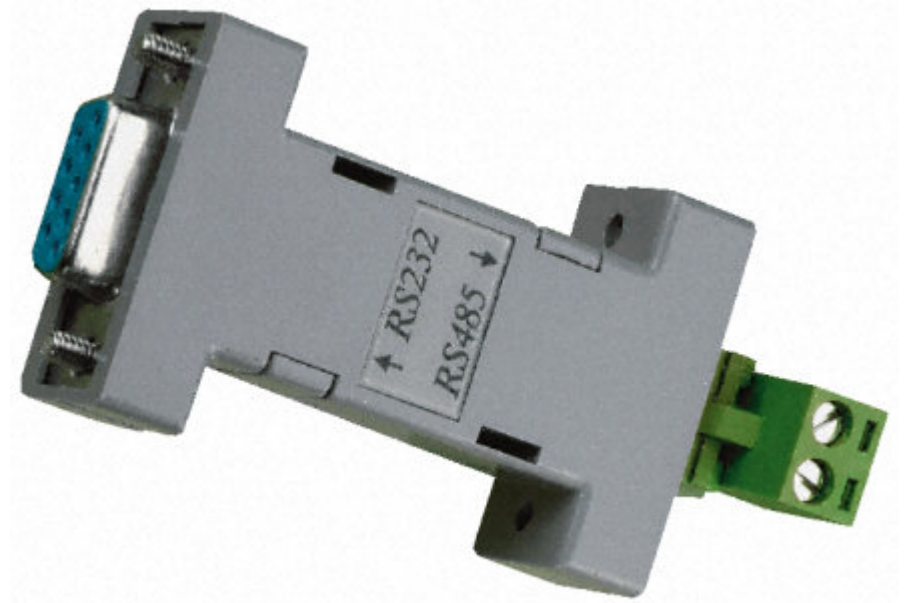| SPECIFICATIONS	RS232	RS423 (not wide use)	RS422	RS485
Mode of Operation	SINGLE-ENDED	SINGLE-ENDED	DIFFERENTIAL	DIFFERENTIAL
Total Number of Drivers and Receivers on One Line (One driver active at a time for RS485 networks)	1 DRIVER 1 RECVR	1 DRIVER 10 RECVR	1 DRIVER 10 RECVR	32 DRIVER 32 RECVR
Maximum Cable Length	50 FT.	4000 FT.	4000 FT.	4000 FT.
Maximum Data Rate (40ft. - 4000ft. for RS422/RS485)	20kb/s	100kb/s	10Mb/s-100Kb/s	10Mb/s-100Kb/s
Maximum Driver Output Voltage	+/-25V	+/-6V	-0.25V to +6V	-7V to +12V
Driver Output Signal Level (Loaded Min.) **Loaded**	+/-5V to +/-15V	+/-3.6V	+/-2.0V	+/-1.5V
Driver Output Signal Level (Unloaded Max) **Unloaded**	+/-25V	+/-6V	+/-6V	+/-6V
Driver Load Impedance (Ohms)	3k to 7k	>=450	100	54
Max. Driver Current in High Z State **Power On**	N/A	N/A	N/A	+/-100uA
Max. Driver Current in High Z State **Power Off**	+/-6mA @ +/-2v	+/-100uA	+/-100uA	+/-100uA
Slew Rate (Max.)	30V/uS	Adjustable	N/A	N/A
Receiver Input Voltage Range	+/-15V	+/-12V	-10V to +10V	-7V to +12V
Receiver Input Sensitivity	+/-3V	+/-200mV	+/-200mV	+/-200mV
Receiver Input Resistance (Ohms), (1 Standard Load for RS485)	3k to 7k	4k min.	4k min.	>=12k

RS 232 Vs RS485

- RS232 Limitations

	Speed	Distance	No of devices
RS232	20 kbps	50-100 ft	1
RS485	10Mbps	4000ft	25

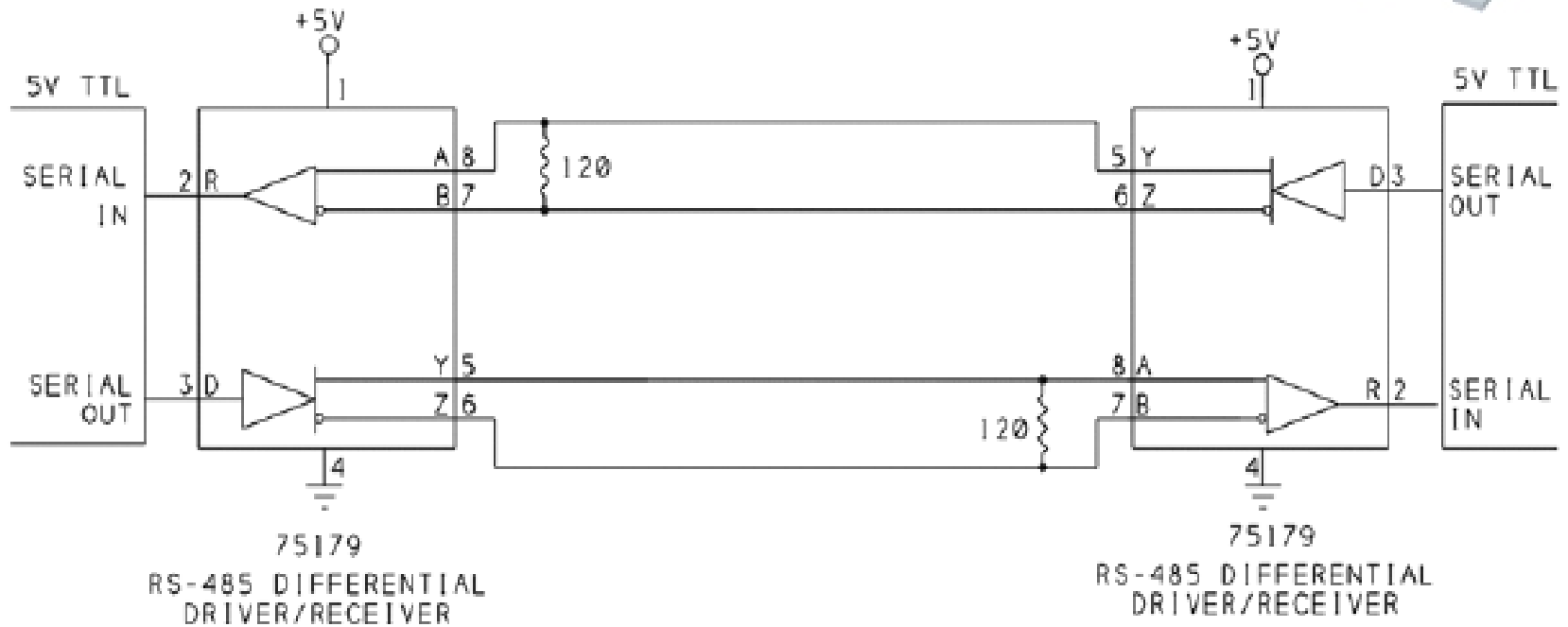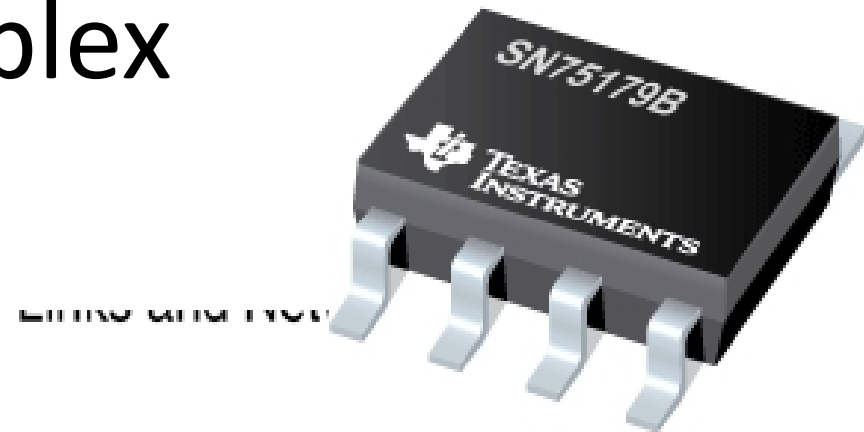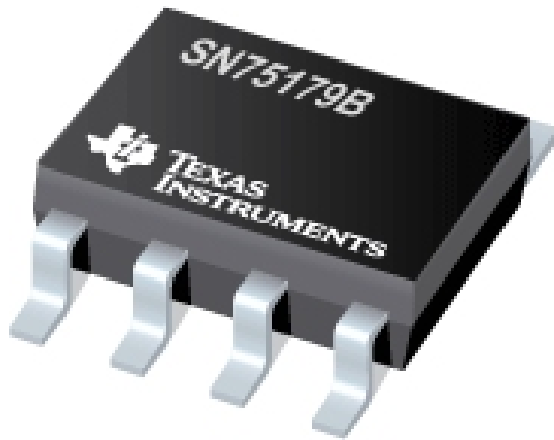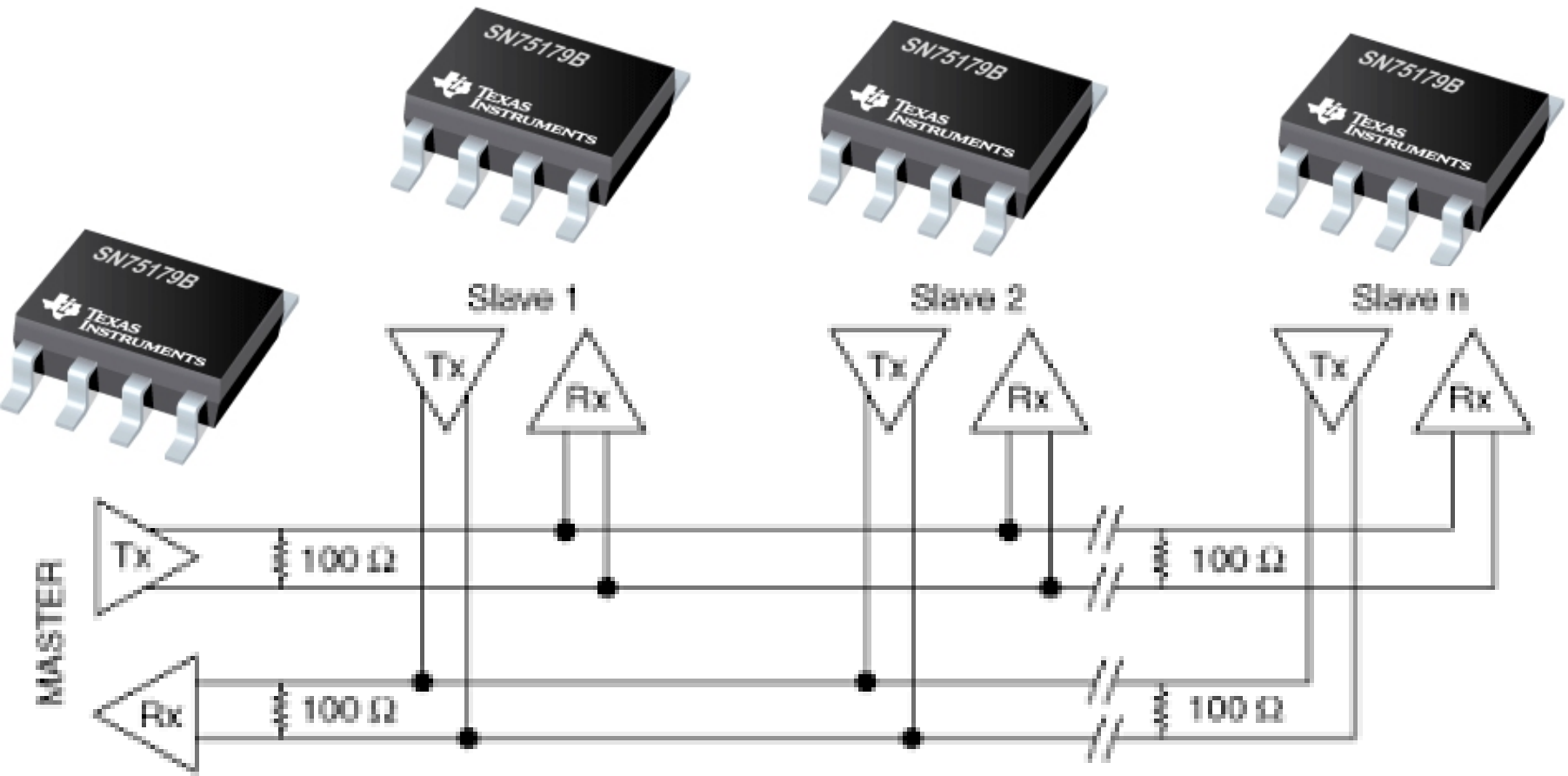| RS232	Dual supply or expensive V convertion
RS485	Single +5V TTL

How to get a port
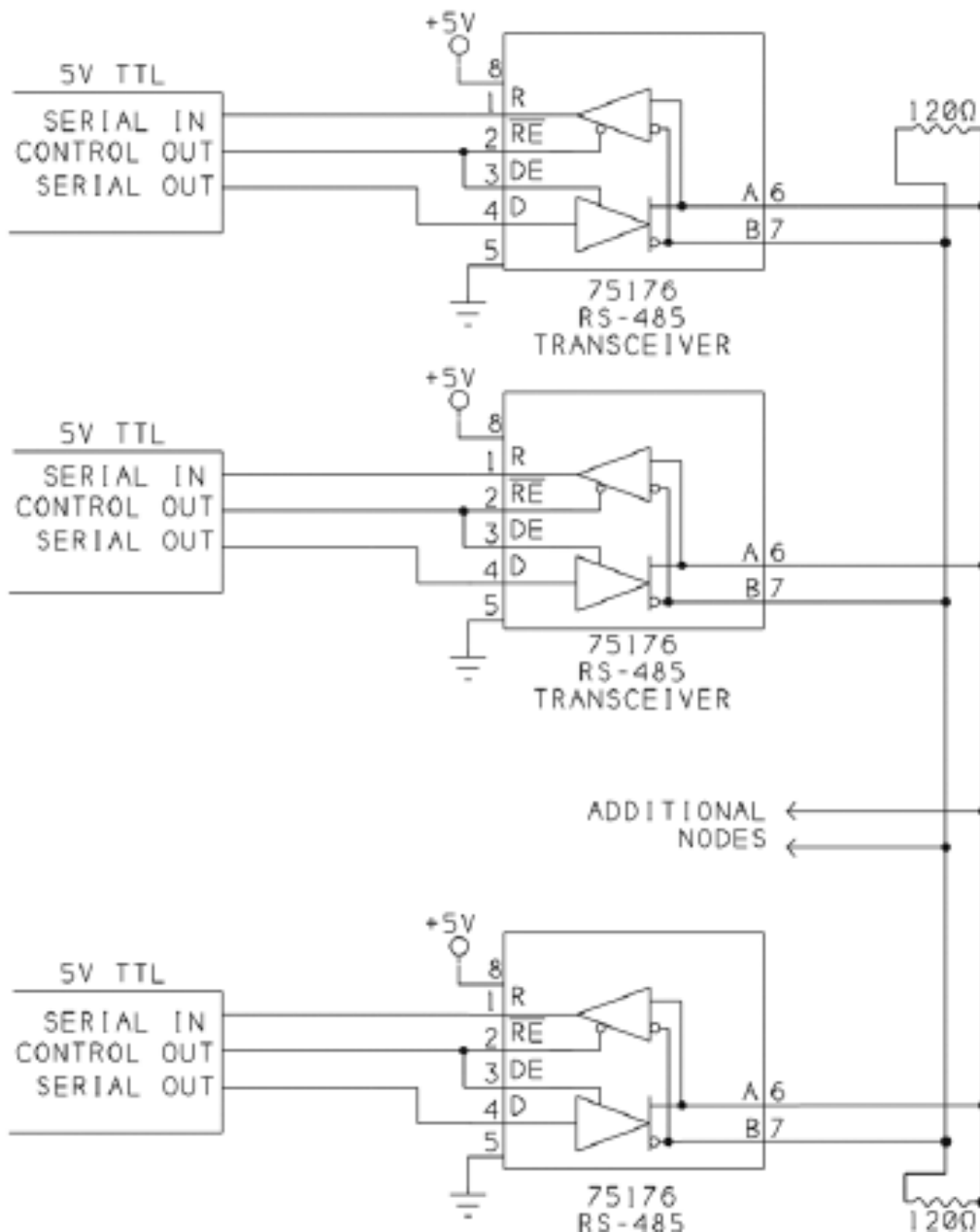# USB/RS232 to RS485 converters
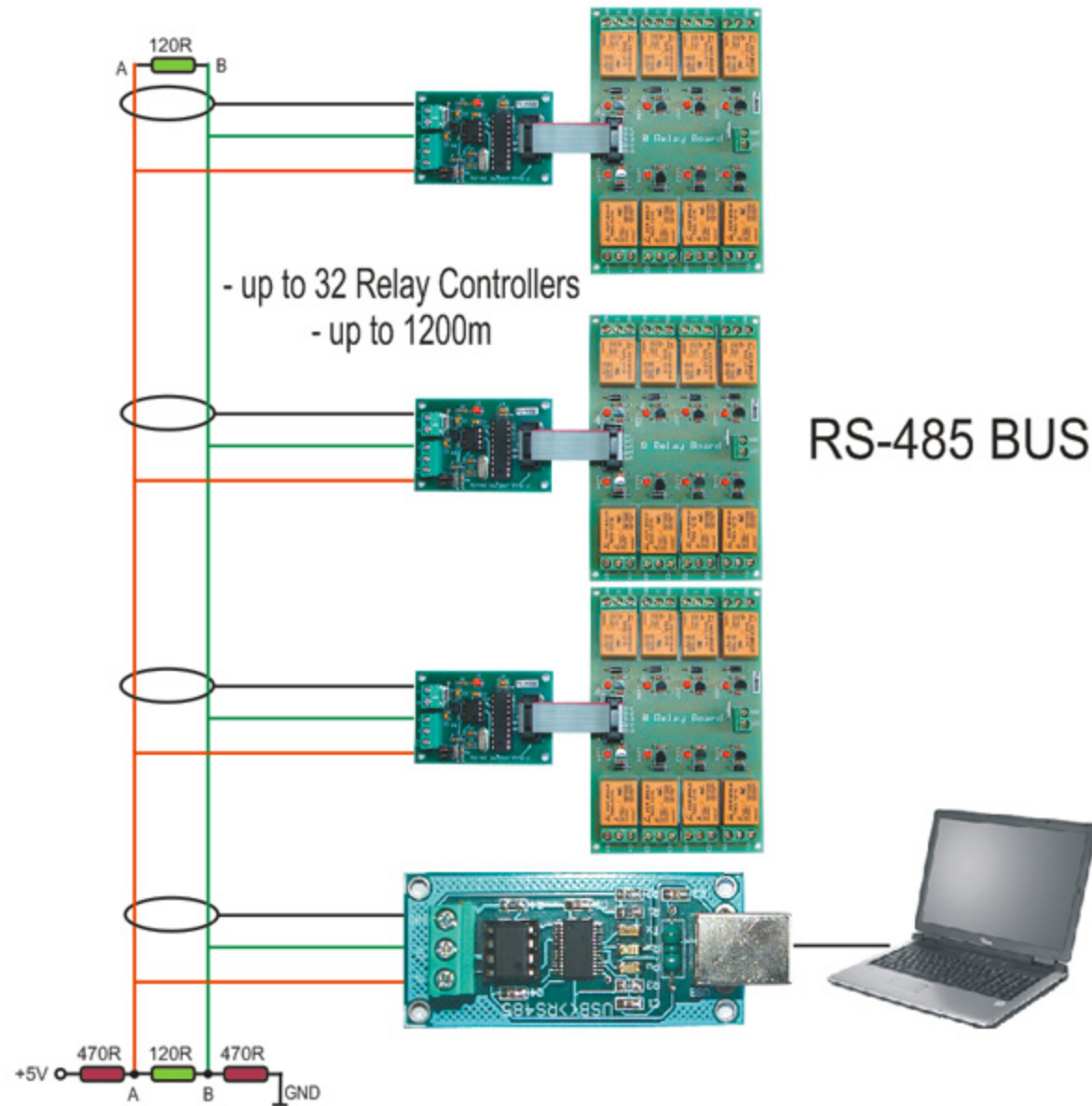
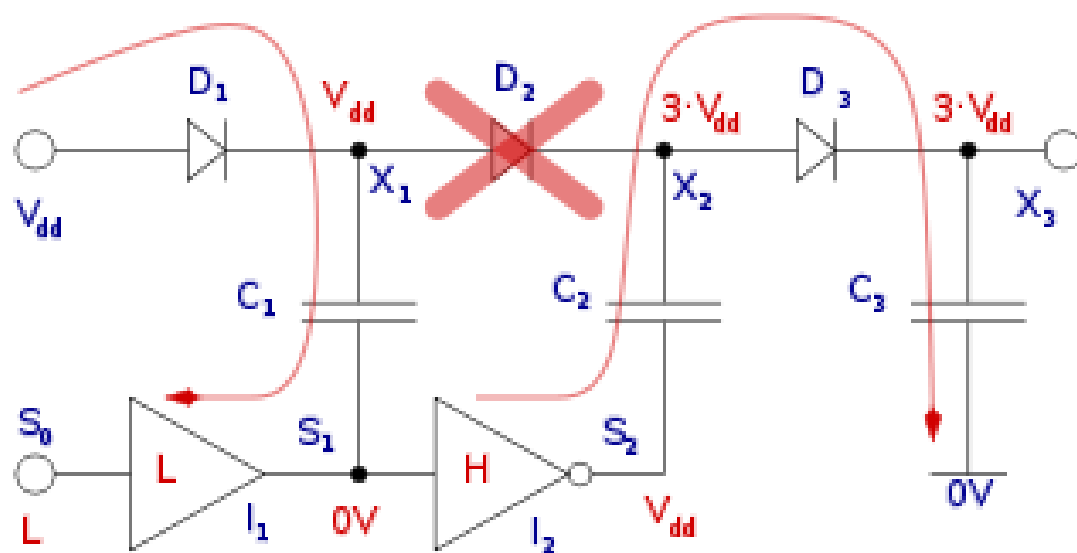# Plug into main bus ISA or PCI

Full Duplex

Full duplex multidrop

Half Duplex

120R

A B

- up to 32 Relay Controllers
- up to 1200m

RS-485 BUS

+5V

470R 120R 470R

A B GND