@meGanesha

Project Proposal - Digital Building Blocks

Team Members

- Irfan Nurhakim Hilmi <@irfannhlm:matrix.org>
- Randy Revaldo Pratama
- Nur Dawam Abdan Syakuro
- Avila Khadhibyan

Team Background

- Academic Experience
 All members just finished 3rd year in Electrical Engineering, Institut Teknologi Bandung (ITB), Indonesia
- Work Experience
 All members have worked with SkyWater 130 nm PDK using IIC-OSIC-TOOLS and perform basic schematic design, simulation, and layout

Project Information

Goal

Create efficient pass transistor logic (PTL)-based multiplexers as standard cells. Provide full characterization for open-source library integration.

Design

The plan is to design 4-1 MUX using transmission gates. The target is less area with similar (or better) characteristics than standard multiplexers. The target drive strength is X3 and X4.

Application

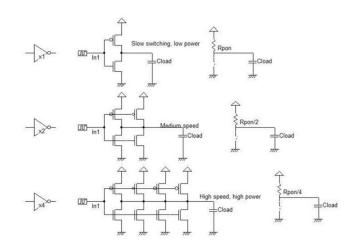
Original idea is to use these cells for area-efficient barrel shifters, but can definitely be used for other macro cells.

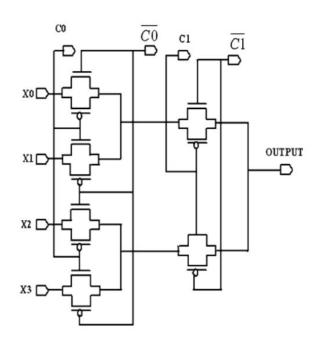
References

M. Mishra and S. Akashe, "High performance, low power 200 Gb/s 4:1 MUX with TGL in 45 nm technology," *Appl. Nanosci.*, vol. 4, no. 8, pp. 889–895, Dec. 2014, doi: 10.1007/s13204-013-0206-0

Preliminary Research

The circuit schematic can be seen on the right. The variation in drive strength can be achieved by enlarging the transistor sizes.





Timeline

Task	July 2025			August 2025					September 2025			
	28	29	30	31	32	33	34	35	36	37	38	39
Proposal Review												
Schematic & Simulation												
Schematic Review												
Simulation Review (blocks)												
Simulation Review (top level)												
Layout, LVS, DRC												
Post-Layout Tasks												
Layout Review (blocks)												
Layout Review (top level)												
Verification												
Final Chip Review												

Milestones

- Schematic & Simulation
 - Deep research & experimentation
 - Final schematic decision
 - Functional & timing analysis
- Physical Implementation
 - Layout creation
 - o DRC & LVS
- Post-Layout Tasks
 - Parasitic extraction
 - Simulation with the extracted parasitics
 - Characterization
 - Integration

Task Distribution

- Schematic & Simulation: Randy
- Physical Implementation
 - Layout creation: Avila
 - DRC & LVS: Irfan
- Post-Layout Tasks
 - Parasitic extraction: Irfan
 - Simulation with the extracted parasitics: Avila
 - Characterization: Dawam
 - o Integration: Dawam

Questions, Suggestions, Doubts

- Any suggestions on effective task allocation?
- Is it better if each person work on different variations, or stay with 4 people for one cell?
- Possibility of adding demux design if too simple?