IT 451: Computer Organization and Architecture (Sessional)

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Assignment 1

1.) Design and simulate the behavioral models of basic gates (AND, OR, NOT), universal gates, XOR, XNOR gates.

VHDL MODULE :

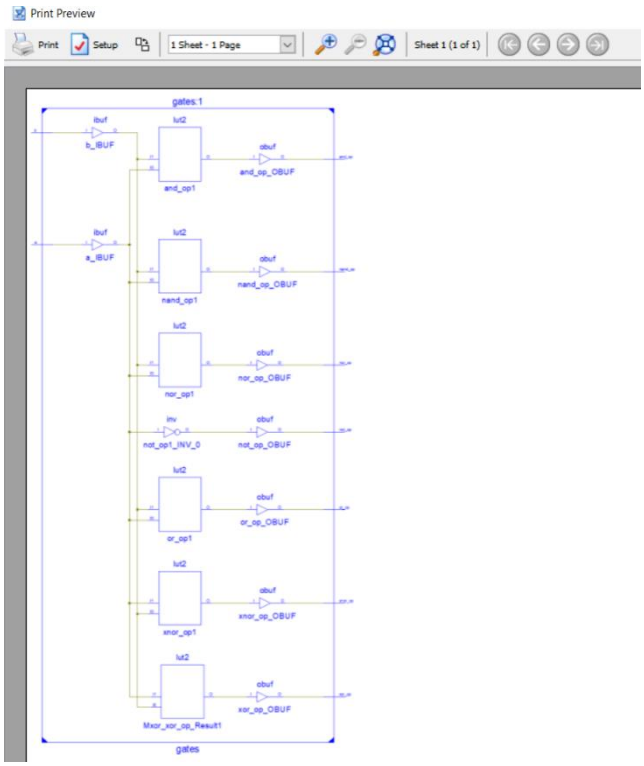
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Q1 is
    Port ( a : in  STD_LOGIC;
           b : in  STD_LOGIC;
           or_op : out  STD_LOGIC;
           and_op : out  STD_LOGIC;
           not_op : out  STD_LOGIC;
           nand_op : out  STD_LOGIC;
           nor_op : out  STD_LOGIC;
           xor_op : out  STD_LOGIC;
           xnor_op : out  STD_LOGIC);
end Q1;

architecture Behavioral of Q1 is

begin
 or_op<=a or b;
 and_op<=a and b;
 not_op<=not a;
 nand_op<=a nand b;
 nor_op<=a nor b;
 xor_op<=a xor b;
 xor_op<=a xnor b;


end Behavioral;
```

TEST BENCH :

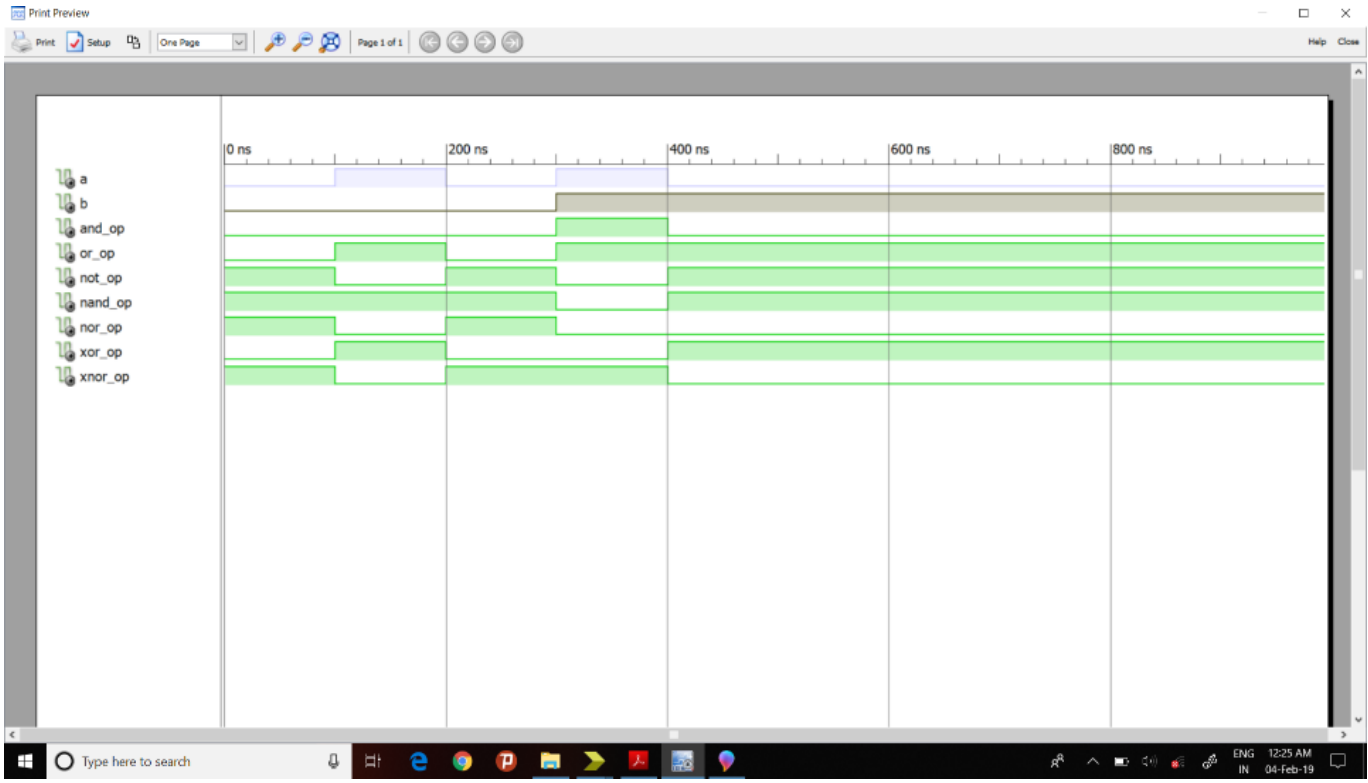
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY test IS
END test;

ARCHITECTURE behavior OF test IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT gates
    PORT(
         a : IN  std_logic;
         b : IN  std_logic;
         and_op : OUT  std_logic;
         or_op : OUT  std_logic;
         not_op : OUT  std_logic;
         nand_op : OUT  std_logic;
         nor_op : OUT  std_logic;
         xor_op : OUT  std_logic;
         xnor_op : OUT  std_logic
        );
    END COMPONENT;


   --Inputs
   signal a : std_logic := '0';
   signal b : std_logic := '0';

            --Outputs
   signal and_op : std_logic;
   signal or_op : std_logic;
   signal not_op : std_logic;
   signal nand_op : std_logic;
   signal nor_op : std_logic;
   signal xor_op : std_logic;
   signal xnor_op : std_logic;
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name

  -- constant <clock>_period : time := 10 ns;

BEGIN

            -- Instantiate the Unit Under Test (UUT)
   uut: gates PORT MAP (
         a => a,
         b => b,
         and_op => and_op,
         or_op => or_op,
         not_op => not_op,
         nand_op => nand_op,
         nor_op => nor_op,
         xor_op => xor_op,
         xnor_op => xnor_op
        );

   -- Clock process definitions
  -- <clock>_process :process
   --begin
                        --<clock> <= '0';
                        --wait for <clock>_period/2;
                        --<clock> <= '1';
                        --wait for <clock>_period/2;
   --end process;
```

```
  -- Stimulus process
  stim_proc: process
  begin
          wait for 100ns;
                  a<='1';
                  b<='0';
                  wait for 100ns;
                  a<='0';
                  b<='0';
                  wait for 100ns;
                  a<='1';
                  b<='1';
                  wait for 100ns;
                  a<='0';
                  b<='1';
                  wait for 100ns;
     -- hold reset state for 100 ns.
     --wait for 100 ns;

     --wait for <clock>_period*10;

     -- insert stimulus here

     wait;
  end process;

END;
```

RTL Schematic –



Simulation -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or_op
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nor_op
xor_op
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2.) Design and simulate the behavioral model of a 1-bit magnitude comparator. It should accept two input bits and give three output lines (greater, less, equal).

VHDL MODULE:

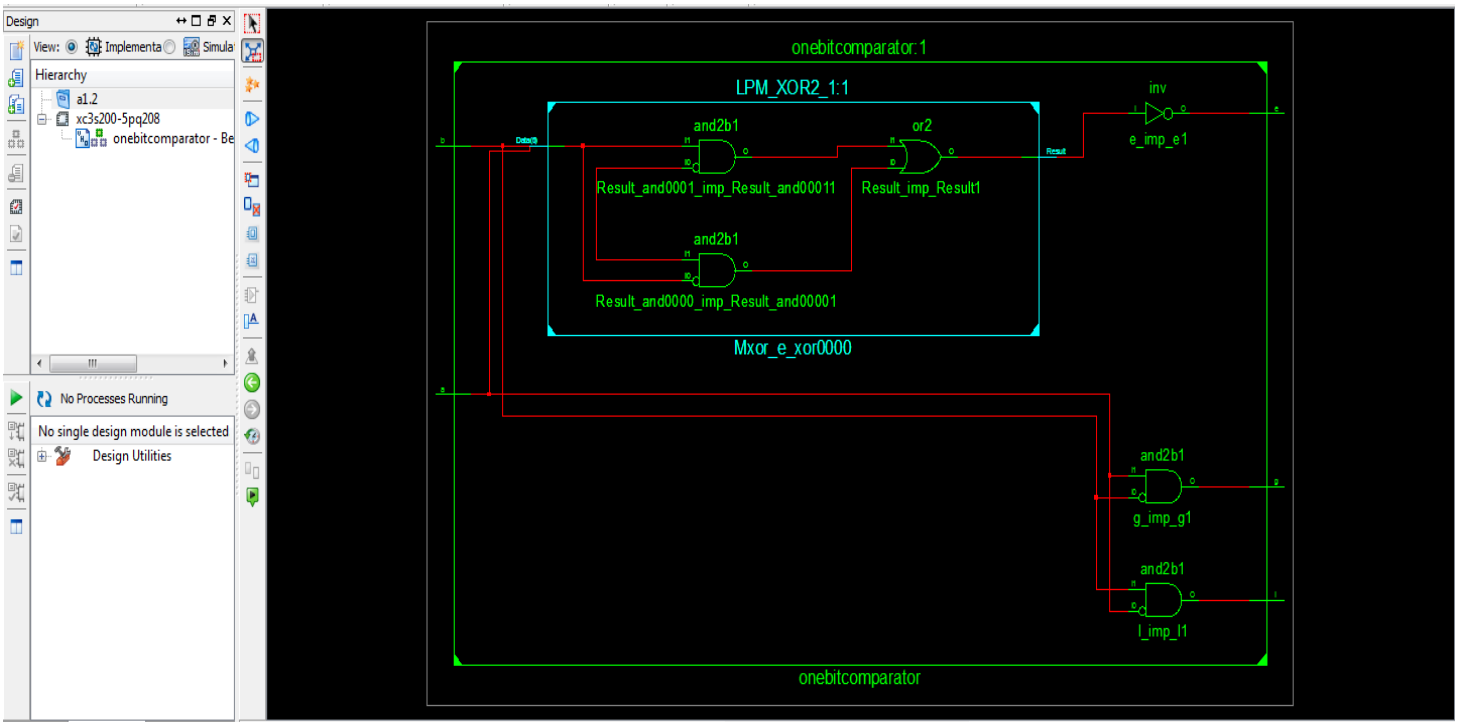
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity onebitcomparator is
    Port ( a,b : in  STD_LOGIC;
           g,l,e : out  STD_LOGIC);
end onebitcomparator;

architecture Behavioral of onebitcomparator is

begin
g<=a and not b;
l<= not a and b;
e<=a xnor b;


end Behavioral;
```

TEST BENCH:

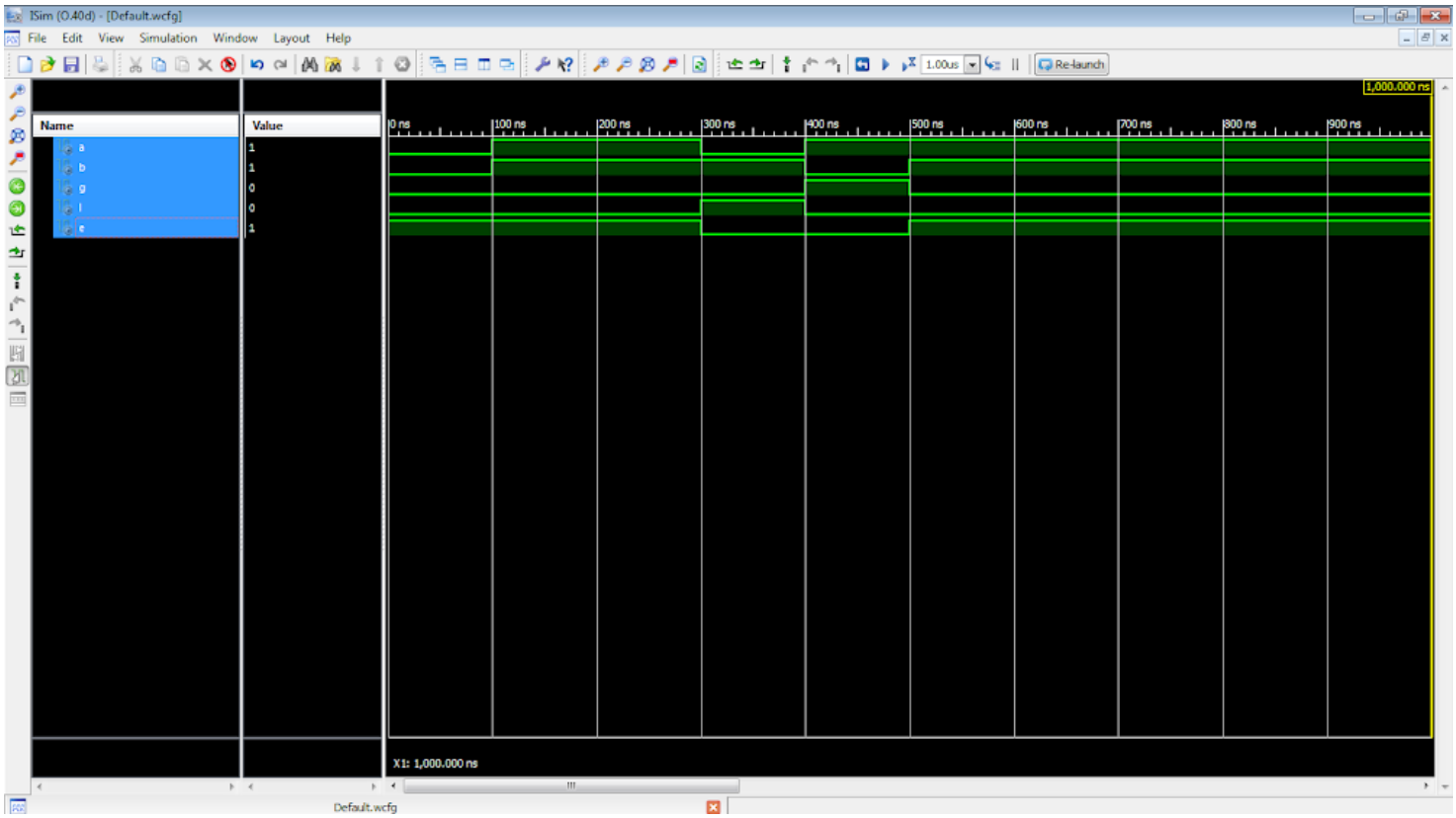
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY onebitcomp IS
END onebitcomp;

ARCHITECTURE behavior OF onebitcomp IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT onebitcomparator
    PORT(
         a : IN  std_logic;
         b : IN  std_logic;
         g : OUT  std_logic;
         l : OUT  std_logic;
         e : OUT  std_logic
        );
    END COMPONENT;
```

```
   --Inputs
   signal a : std_logic := '0';
   signal b : std_logic := '0';

  --Outputs
   signal g : std_logic;
   signal l : std_logic;
   signal e : std_logic;
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name

   --constant <clock>_period : time := 10 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)
   uut: onebitcomparator PORT MAP (
          a => a,
          b => b,
          g => g,
          l => l,
          e => e
        );

   -- Clock process definitions
   --<clock>_process :process
   --begin
--<clock> <= '0';
--wait for <clock>_period/2;
--<clock> <= '1';
--wait for <clock>_period/2;
   --end process;


   -- Stimulus process
   stim_proc: process
   begin
      -- hold reset state for 100 ns.
      --wait for 100 ns;

      --wait for <clock>_period*10;

      -- insert stimulus here
      a<='0','1' after 100 ns, '1' after 200 ns, '0' after 300 ns,'1' after 400 ns;
b<='0','1' after 100 ns, '1' after 150 ns, '0' after 400 ns,'1' after 500 ns;
      wait;
   end process;

END;
```

RTL Schematic -



Simulation -



3.)Design the behavioral model (with process statement) of a 4-bit magnitude comparator and simulate.

VHDL MODULE:

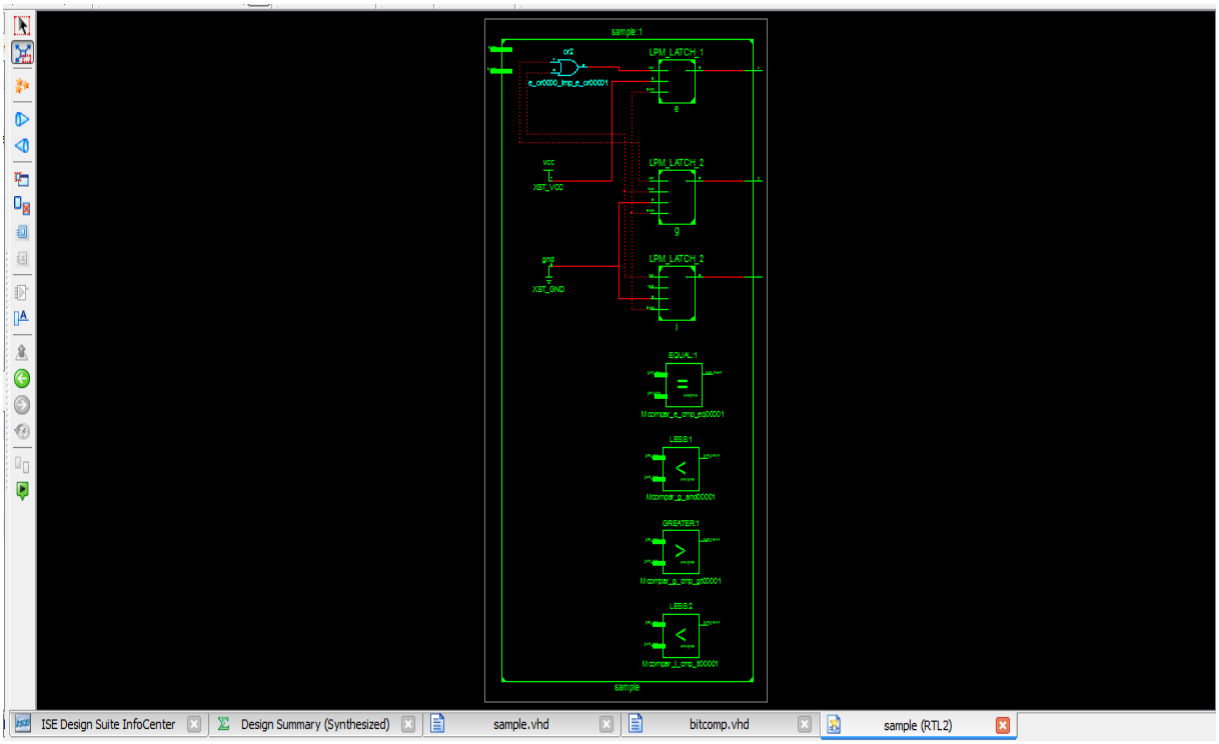
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity sample is
    Port ( a,b : in  STD_LOGIC_VECTOR (3 downto 0);
           g,l,e : out  STD_LOGIC);
end sample;

architecture Behavioral of sample is
begin
process(a,b) is
begin
if(a>b) then
 e<='0';
 g<='1';
 l<='0';
elsif(a<b) then
 e <='0';
 g<='0';
 l<='1';
elsif(a=b) then
e<='1';
g<='0';
l<='0';
end if;
end process;
end Behavioral;
```

TEST BENCH:

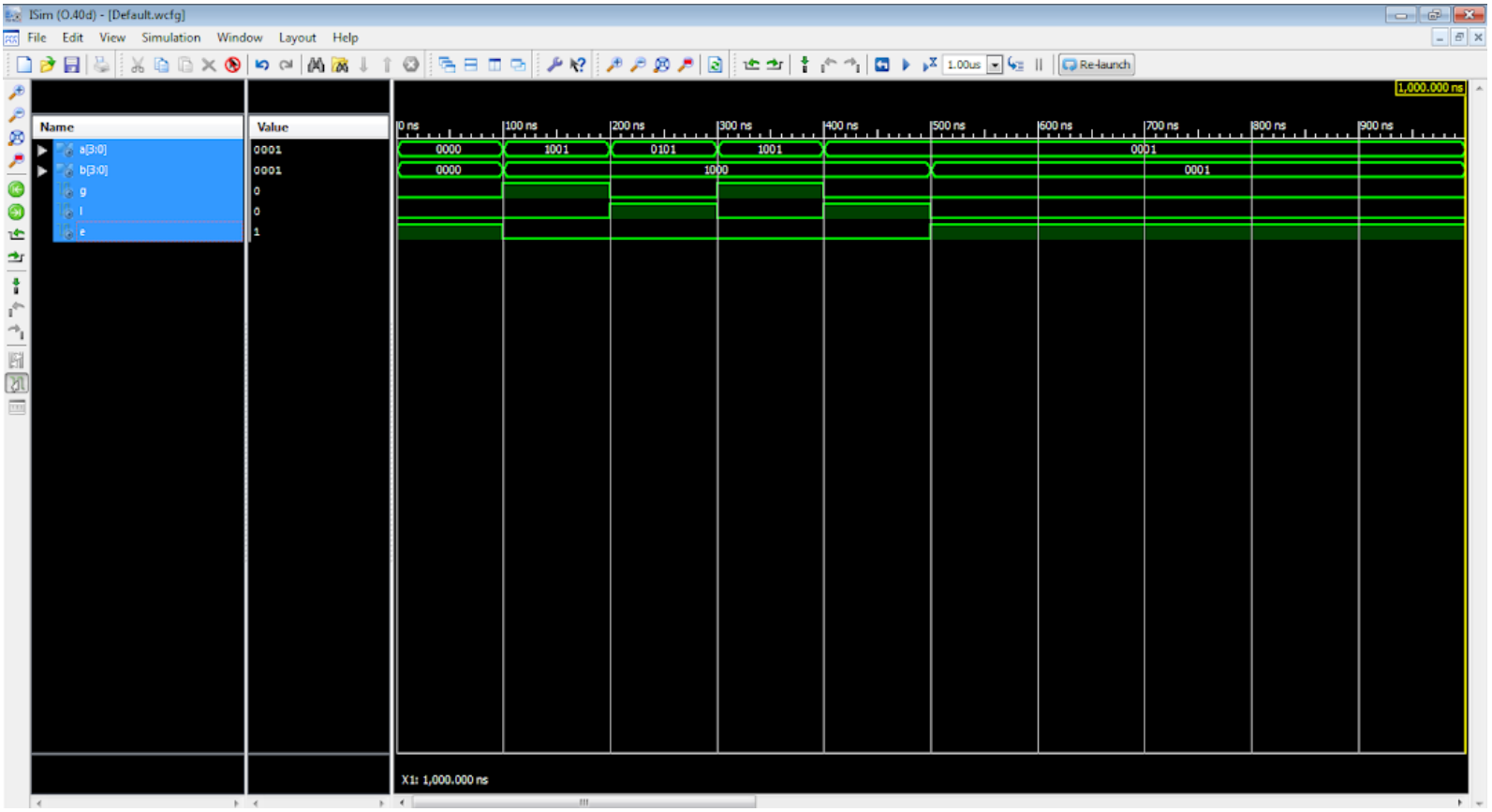
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY bitcomp IS
END bitcomp;

ARCHITECTURE behavior OF bitcomp IS
```

```
    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT sample
    PORT(
         a : IN  std_logic_vector(3 downto 0);
         b : IN  std_logic_vector(3 downto 0);
         g : OUT  std_logic;
         l : OUT  std_logic;
         e : OUT  std_logic
        );
    END COMPONENT;


   --Inputs
   signal a : std_logic_vector(3 downto 0) := (others => '0');
   signal b : std_logic_vector(3 downto 0) := (others => '0');

  --Outputs
   signal g : std_logic;
   signal l : std_logic;
   signal e : std_logic;
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name

   --constant <clock>_period : time := 10 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)
   uut: sample PORT MAP (
          a => a,
          b => b,
          g => g,
          l => l,
          e => e
        );

   -- Clock process definitions
   --<clock>_process :process
   --begin
--<clock> <= '0';
--wait for <clock>_period/2;
--<clock> <= '1';
--wait for <clock>_period/2;
   --end process;


   -- Stimulus process
   stim_proc: process
   begin
      -- hold reset state for 100 ns.
      --wait for 100 ns;

      --wait for <clock>_period*10;

      -- insert stimulus here
a<="0000","1001" after 100 ns, "0101" after 200 ns, "1001" after 300 ns,"0001" after 400 ns;
b<="0000","1000" after 100 ns, "1000" after 150 ns, "1000" after 400 ns,"0001" after 500 ns;

      wait;
   end process;

END;
```

RTL Schematic -



Simulation –



4.) Design and simulate the behavioral model of a 1-bit full adder .

VHDL MODULE:

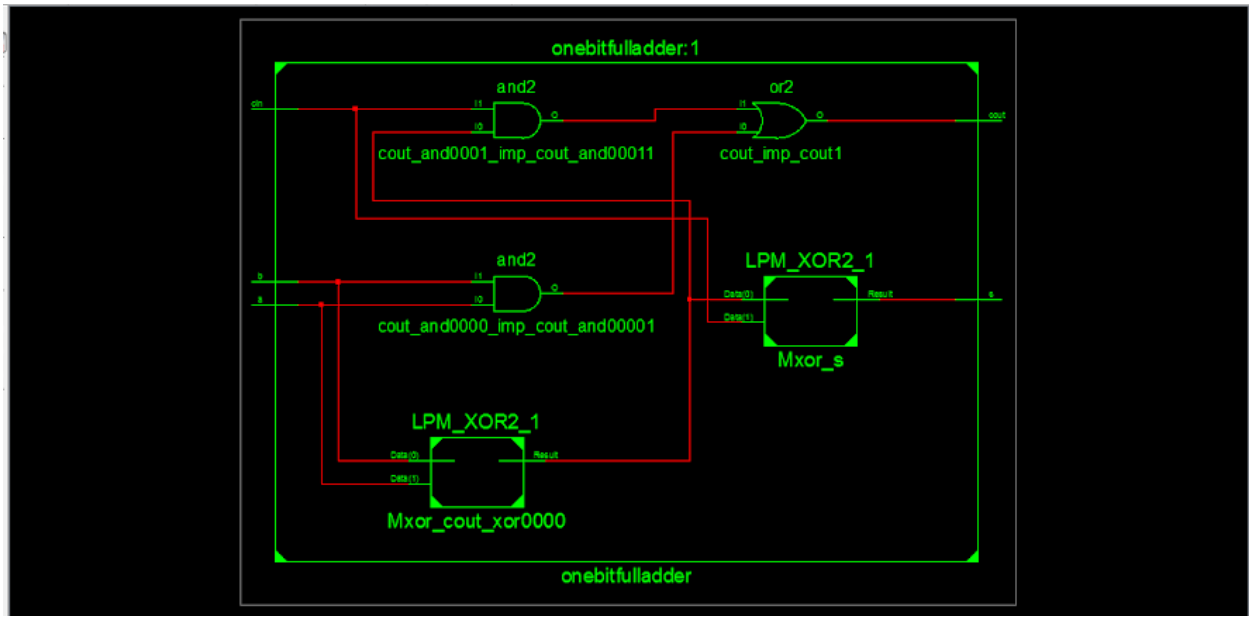
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity onebitfulladder is
    Port ( a,b,cin : in  STD_LOGIC;
           s,cout : out  STD_LOGIC);
end onebitfulladder;

architecture Behavioral of onebitfulladder is

begin
s<= a xor b xor cin;
cout<= (a and b) or ((a xor b )and cin);


end Behavioral;
```

TEST BENCH:

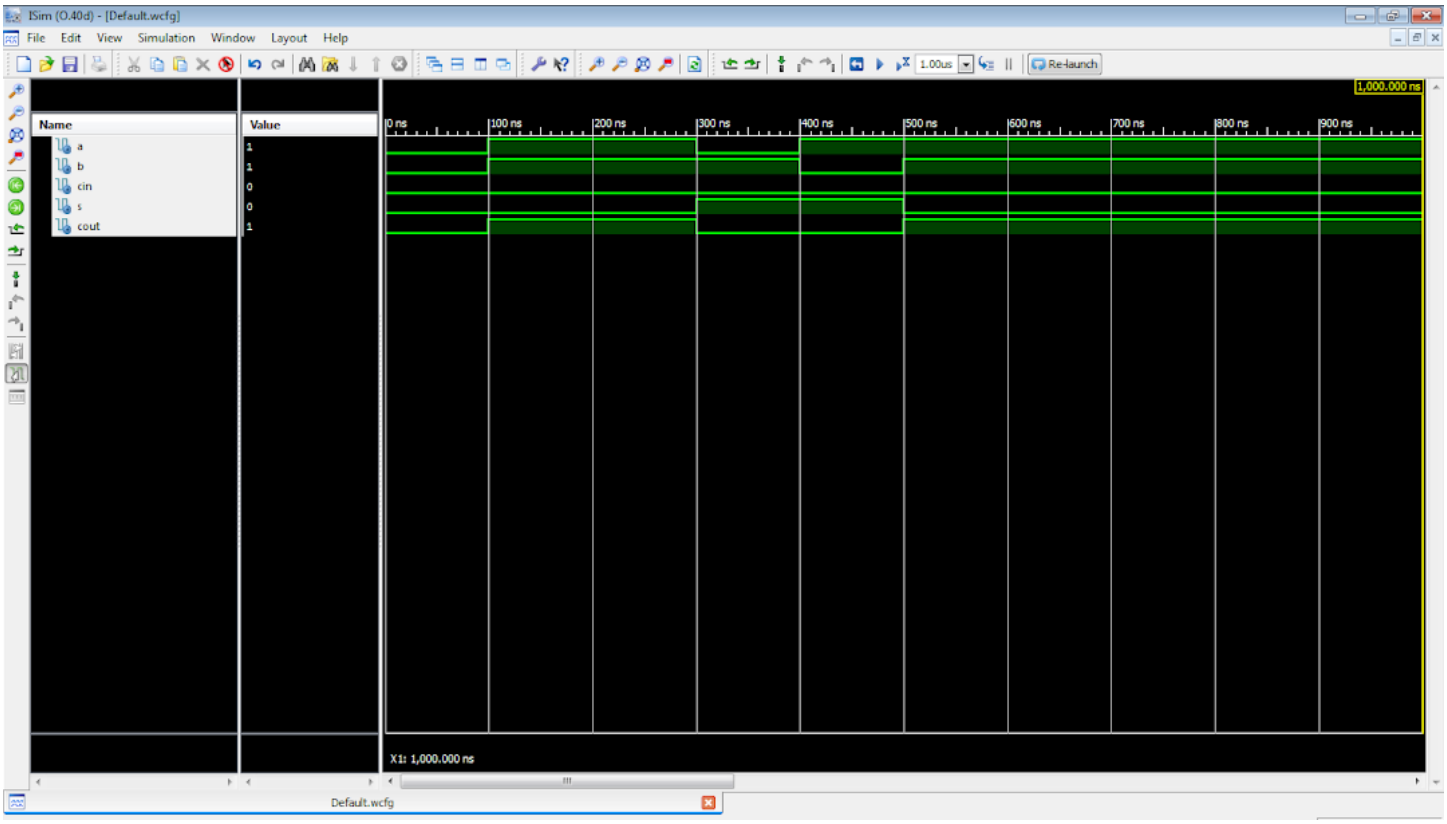
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY onebitadd IS
END onebitadd;

ARCHITECTURE behavior OF onebitadd IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT onebitfulladder
    PORT(
         a : IN  std_logic;
         b : IN  std_logic;
         cin : IN  std_logic;
         s : OUT  std_logic;
         cout : OUT  std_logic
        );
    END COMPONENT;


   --Inputs
```

```
   signal a : std_logic := '0';
   signal b : std_logic := '0';
   signal cin : std_logic := '0';

  --Outputs
   signal s : std_logic;
   signal cout : std_logic;
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name

   --constant <clock>_period : time := 10 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)
   uut: onebitfulladder PORT MAP (
          a => a,
          b => b,
          cin => cin,
          s => s,
          cout => cout
        );

   -- Clock process definitions
   --<clock>_process :process
   --begin
-- <clock> <= '0';
-- wait for <clock>_period/2;
-- <clock> <= '1';
-- wait for <clock>_period/2;
  -- end process;


   -- Stimulus process
   stim_proc: process
   begin
      -- hold reset state for 100 ns.
   --   wait for 100 ns;

    --  wait for <clock>_period*10;

      -- insert stimulus here
     a<='0','1' after 100 ns, '1' after 200 ns, '0' after 300 ns,'1' after 400 ns;
b<='0','1' after 100 ns, '1' after 150 ns, '0' after 400 ns,'1' after 500 ns;
wait;
   end process;

END;
```

RTL Schematic –



Simulation –



5.) Design the structural model of a full adder using half adder as a component .

VHDL MODULE:

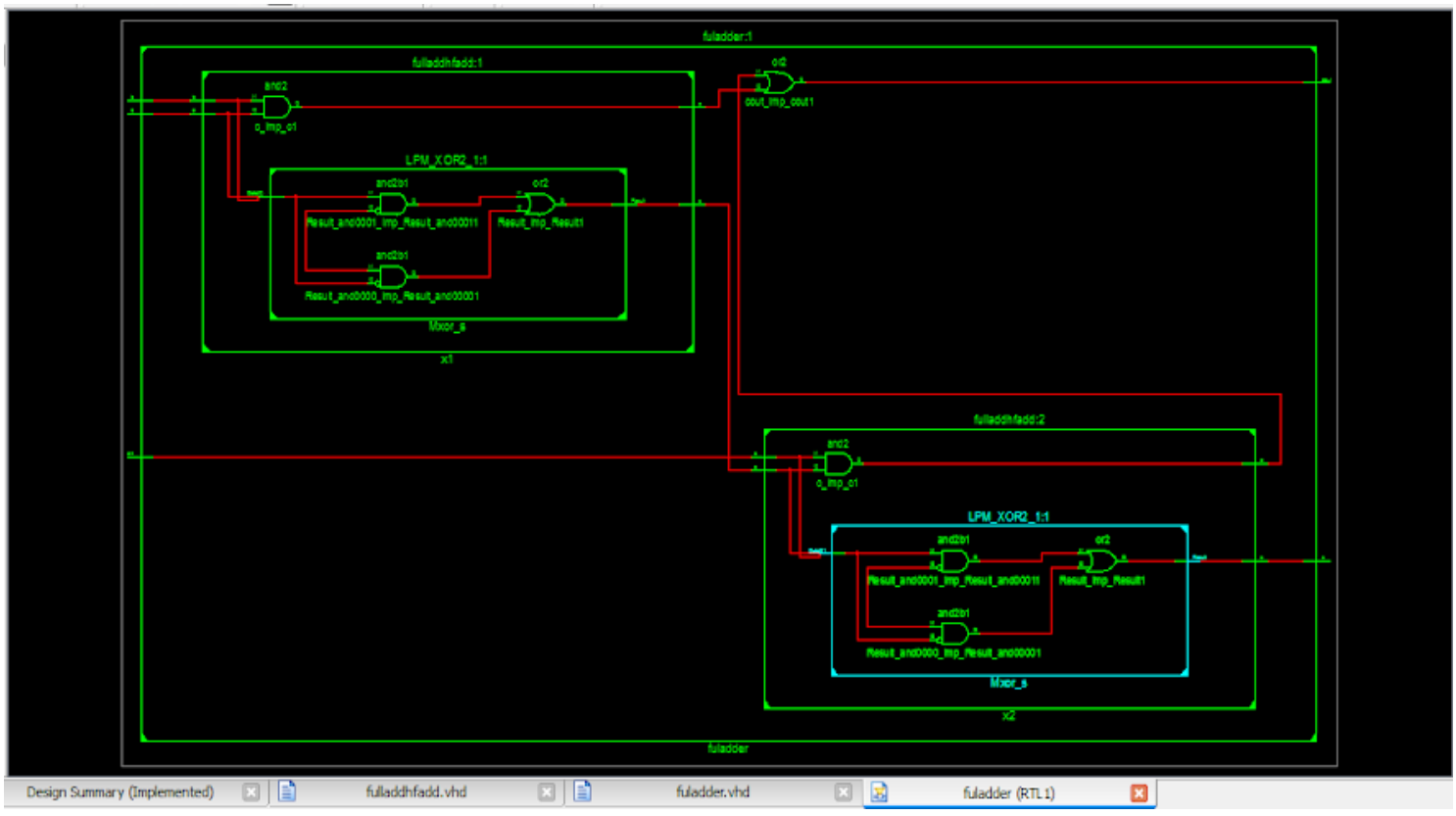
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity fuladder is
    Port ( a,b,cin : in  STD_LOGIC;
           s,cout : out  STD_LOGIC);
end fuladder;

architecture Behavioral of fuladder is
signal p,q,r: std_logic;
component fulladdhfadd is
Port ( a,b : in  STD_LOGIC;
           s,c : out  STD_LOGIC);
end component fulladdhfadd;

begin

x1: fulladdhfadd port map (a,b,p,r);
x2: fulladdhfadd port map (p,cin,s,q);
cout<=r or q;

end Behavioral;
```

TEST BENCH:

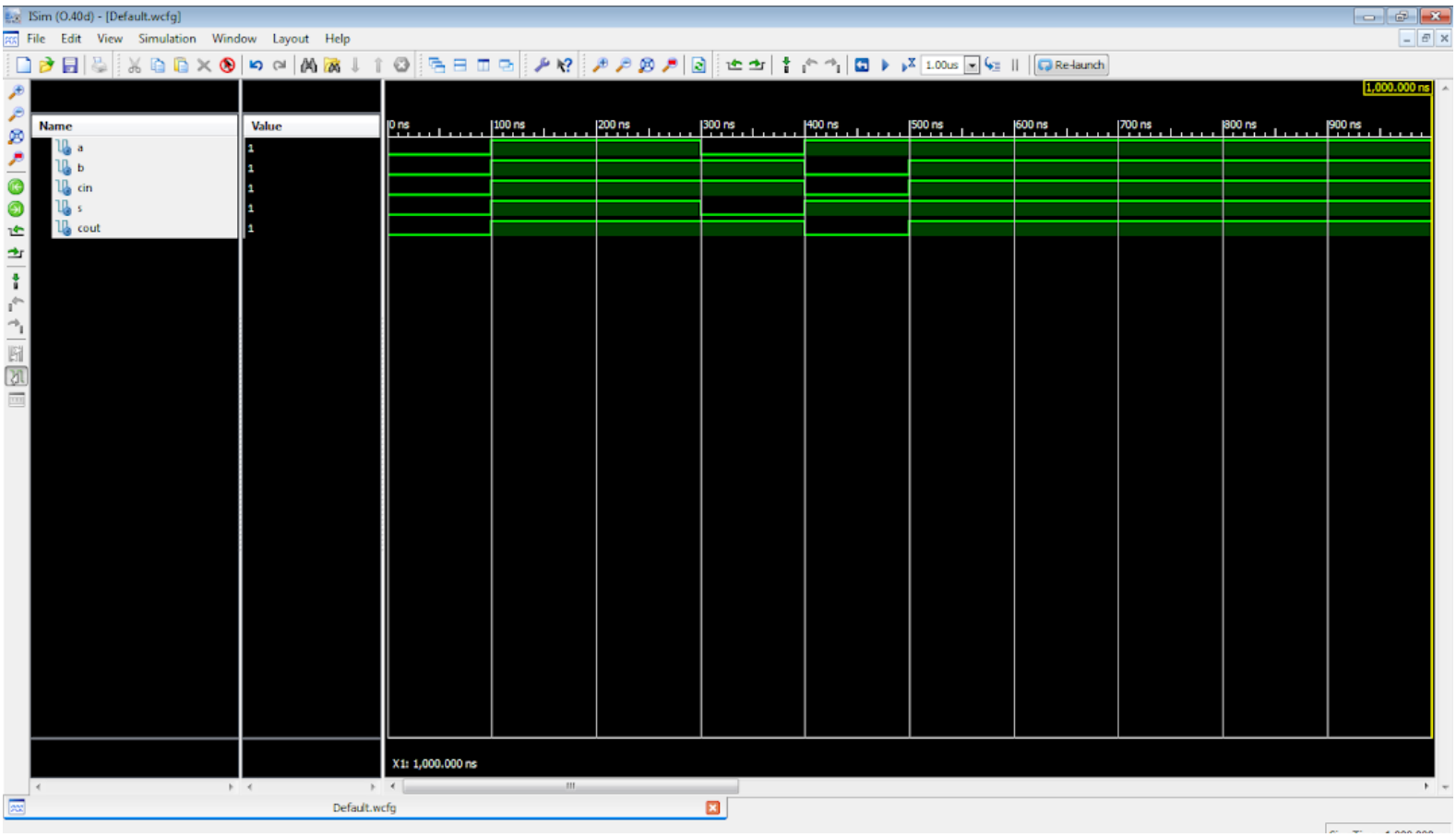
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY fulladder IS
END fulladder;

ARCHITECTURE behavior OF fulladder IS
    COMPONENT fuladder
    PORT(
         a : IN  std_logic;
         b : IN  std_logic;
         cin : IN  std_logic;
         s : OUT  std_logic;
         cout : OUT  std_logic
        );
    END COMPONENT;
   signal a : std_logic := '0';
   signal b : std_logic := '0';
   signal cin : std_logic := '0';

  --Outputs
   signal s : std_logic;
   signal cout : std_logic;
BEGIN
```

```
-- Instantiate the Unit Under Test (UUT)
   uut: fuladder PORT MAP (
          a => a,
          b => b,
          cin => cin,
          s => s,
          cout => cout
        );
    a<='0','1' after 100 ns, '1' after 200 ns, '0' after 300 ns,'1' after 400 ns;
b<='0','1' after 100 ns, '1' after 150 ns, '0' after 400 ns,'1' after 500 ns;
cin<='0','1' after 100 ns, '1' after 150 ns, '0' after 400 ns,'1' after 500 ns;

   -- Stimulus process
   stim_proc: process
   begin
      -- hold reset state for 100 ns.
     -- wait for 100 ns;

      --wait for <clock>_period*10;

      -- insert stimulus here      wait;
   end process;

END;
```

RTL Schematic –



Simulation –



6.) Design a 4-bit BPA using structural design flow hierarchically .

VHDL MODULE:

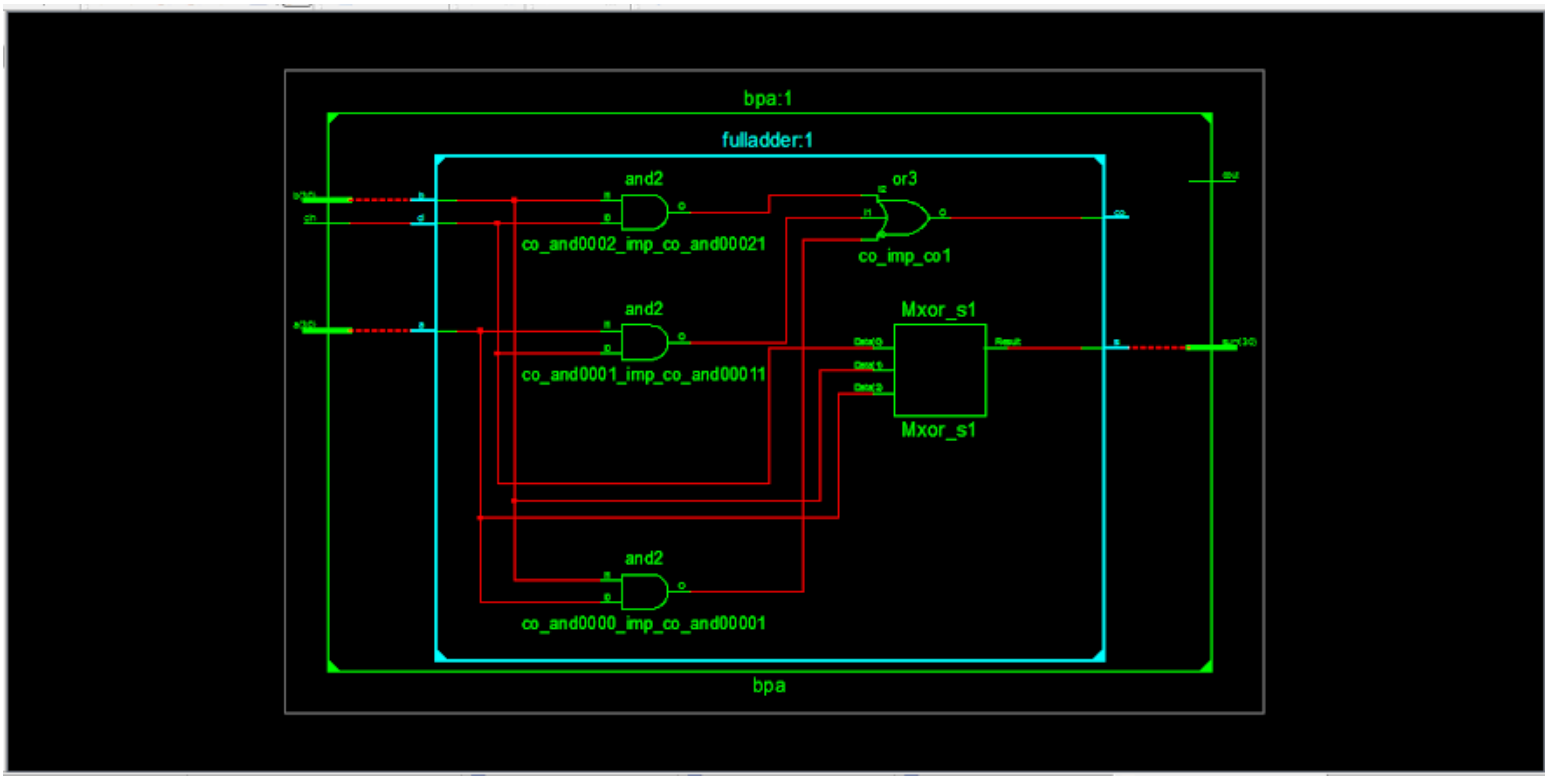
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity bpa is
    Port ( a,b : in  STD_LOGIC_VECTOR (3 downto 0);
           cin : in  STD_LOGIC;
           cout : out  STD_LOGIC;
           sum : out  STD_LOGIC_VECTOR (3 downto 0));
end bpa;

architecture Behavioral of bpa is
signal p,q,r: std_logic;
component fulladder is
port(  a,b,ci : in  STD_LOGIC;
           s,co : out  STD_LOGIC);
end component fulladder;

begin
x1: fulladder port map(a(0),b(0),cin,sum(0),p);
x2: fulladder port map(a(1),b(1),p,sum(1),q);
```

```
x3: fulladder port map(a(2),b(2),q,sum(2),r);
x4: fulladder port map(a(3),b(3),r,sum(3),cout);
end Behavioral;
```

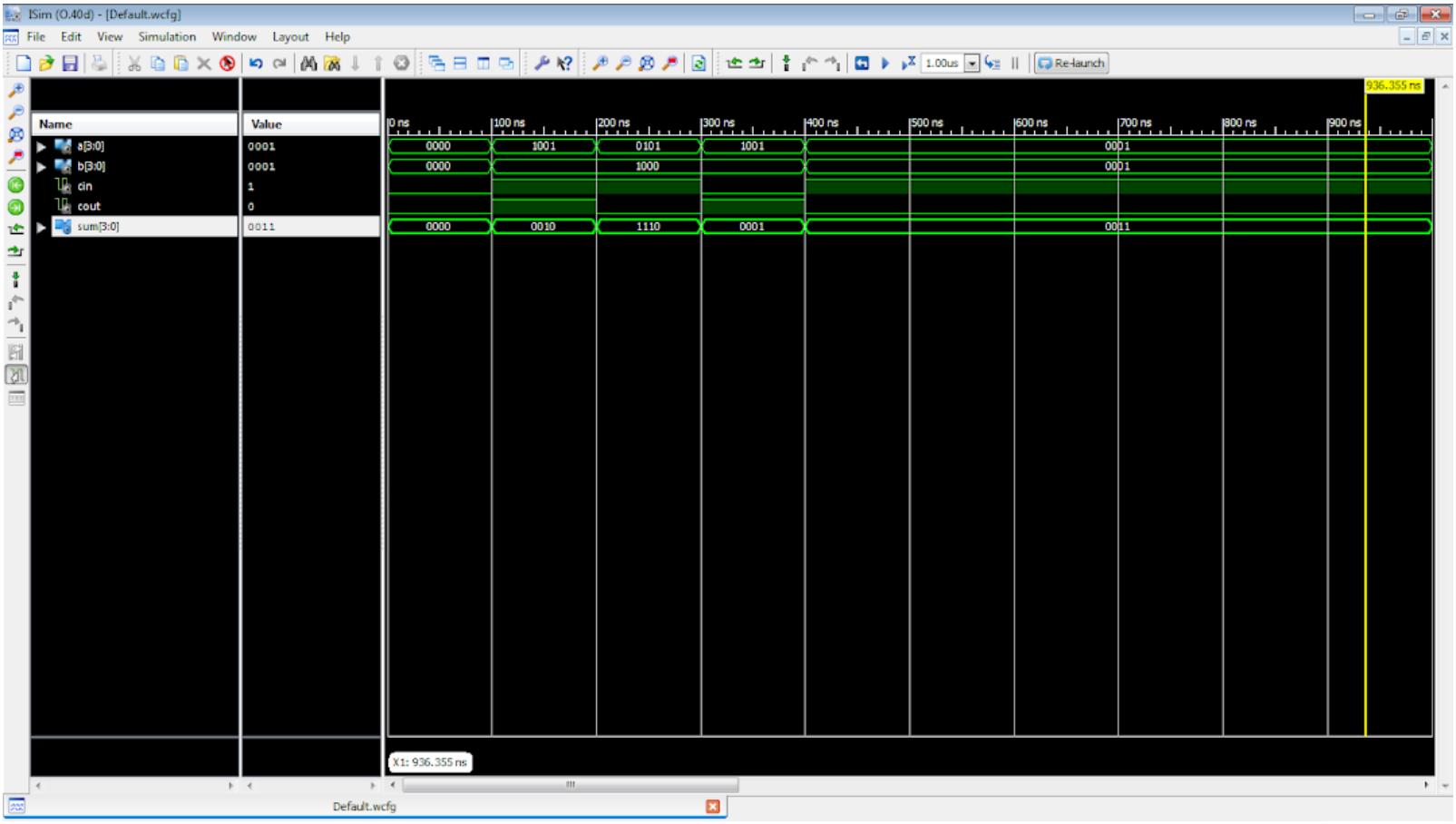
TEST BENCH:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY bpa4bit IS
END bpa4bit;

ARCHITECTURE behavior OF bpa4bit IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT bpa
    PORT(
         a : IN  std_logic_vector(3 downto 0);
         b : IN  std_logic_vector(3 downto 0);
         cin : IN  std_logic;
         cout : OUT  std_logic;
         sum : OUT  std_logic_vector(3 downto 0)
        );
    END COMPONENT;


   --Inputs
   signal a : std_logic_vector(3 downto 0) := (others => '0');
   signal b : std_logic_vector(3 downto 0) := (others => '0');
   signal cin : std_logic := '0';

  --Outputs
   signal cout : std_logic;
   signal sum : std_logic_vector(3 downto 0);
   -- No clocks detected in port list. Replace <clock> below with
   -- appropriate port name

   --constant <clock>_period : time := 10 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)
   uut: bpa PORT MAP (
          a => a,
          b => b,
          cin => cin,
          cout => cout,
          sum => sum
        );

   -- Stimulus process
   stim_proc: process
   begin
      a<="0000","1001" after 100 ns, "0101" after 200 ns, "1001" after 300 ns,"0001" after 400 ns;
b<="0000","1000" after 100 ns, "1000" after 200 ns, "1000" after 300 ns,"0001" after 400 ns;
cin<='0','1' after 100 ns, '1' after 200 ns, '0' after 300 ns,'1' after 400 ns;
      wait;
   end process;
```

RTL Schematic –



Simulation –



7.) a. Design the structural model of a BCD adder using previously designed BPA model as a component.

VHDL MODULE:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity bcd is
    Port ( abcd,bbcd : in  STD_LOGIC_VECTOR (3 downto 0);
           s : out  STD_LOGIC_VECTOR (3 downto 0);
           cinbcd : in  STD_LOGIC;
           coutbcd : out  STD_LOGIC);
end bcd;

architecture Behavioral of bcd is
component bpa is
    Port ( ad : in  STD_LOGIC_VECTOR (3 downto 0);
           bd : in  STD_LOGIC_VECTOR (3 downto 0);
           out1 : out  STD_LOGIC_VECTOR (3 downto 0);
           cind : in  STD_LOGIC;
           coutd : out  STD_LOGIC);
end component;
signal sout,him:std_logic_vector(3 downto 0);
signal cout1,cout2,him1:std_logic;
begin
BADD1 : bpa port map(abcd,bbcd,sout,cinbcd,cout1);

 coutbcd<= cout1;
him1 <= (cout1 or  (sout(3)and sout(2)) or (sout(3) and sout(1)));

   with him1 select
      him <= "0110" when '1',
             "0000" when others;
BADD2 : bpa port map(him,sout,s,'0',cout2);


end Behavioral;
```

7.)b. Also, design the BCD adder without using BPA (behavioral model to be used).

VHDL MODULE:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity bcd_adder is
    port( a,b  : in  unsigned(3 downto 0);
       carry_in : in std_logic;
        sum  : out  unsigned(3 downto 0);
        carry : out std_logic
    );
end bcd_adder;

architecture arch of bcd_adder is
```

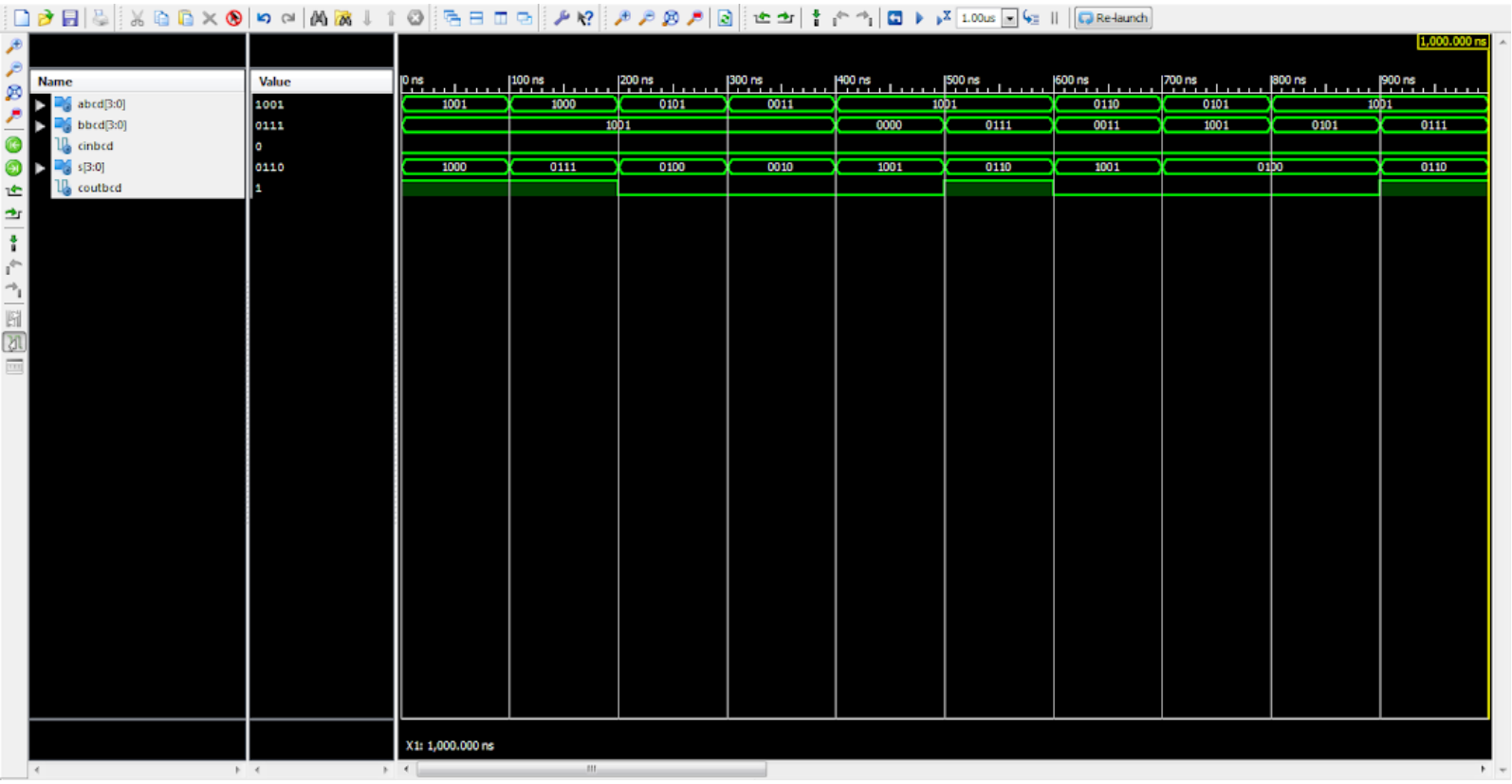
```
begin

process(a,b)
variable sum_temp : unsigned(4 downto 0);
begin
    sum_temp := ('0' & a) + ('0' & b) + ("0000" & carry_in);
    if(sum_temp > 9) then
        carry <= '1';
        sum <= resize((sum_temp + "00110"),4);
    else
        carry <= '0';
        sum <= sum_temp(3 downto 0);
    end if;
end process;

end architecture;
```

TEST BENCH:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY bcd1 IS
END bcd1;

ARCHITECTURE behavior OF bcd1 IS

    -- Component Declaration for the Unit Under Test (UUT)

    COMPONENT bcd
    PORT(
         abcd : IN  std_logic_vector(3 downto 0);
         bbcd : IN  std_logic_vector(3 downto 0);
         s : OUT  std_logic_vector(3 downto 0);
         cinbcd : IN  std_logic;
         coutbcd : OUT  std_logic
        );
    END COMPONENT;

   --Inputs
   signal abcd : std_logic_vector(3 downto 0) := (others => '0');
   signal bbcd : std_logic_vector(3 downto 0) := (others => '0');
   signal cinbcd : std_logic := '0';

  --Outputs
   signal s : std_logic_vector(3 downto 0);
   signal coutbcd : std_logic;
BEGIN

-- Instantiate the Unit Under Test (UUT)
   uut: bcd PORT MAP (
          abcd => abcd,
          bbcd => bbcd,
          s => s,
          cinbcd => cinbcd,
          coutbcd => coutbcd
        );
   stim_proc: process
   begin
 abcd <= "1001"; bbcd <= "1001"; cinbcd <= '0'; wait for 100 ns;
        abcd <= "1000"; bbcd <= "1001"; wait for 100 ns;
        abcd <= "0101"; bbcd <= "1001"; wait for 100 ns;
        abcd <= "0011"; bbcd <= "1001"; wait for 100 ns;
        abcd <= "1001"; bbcd <= "0000";  wait for 100 ns;
        abcd <= "1001"; bbcd <= "0111"; wait for 100 ns;
        abcd <= "0110"; bbcd <= "0011"; wait for 100 ns;
  abcd <= "0101"; bbcd <= "1001"; wait for 100 ns;
        abcd <= "1001"; bbcd <= "0101"; wait for 100 ns;
```

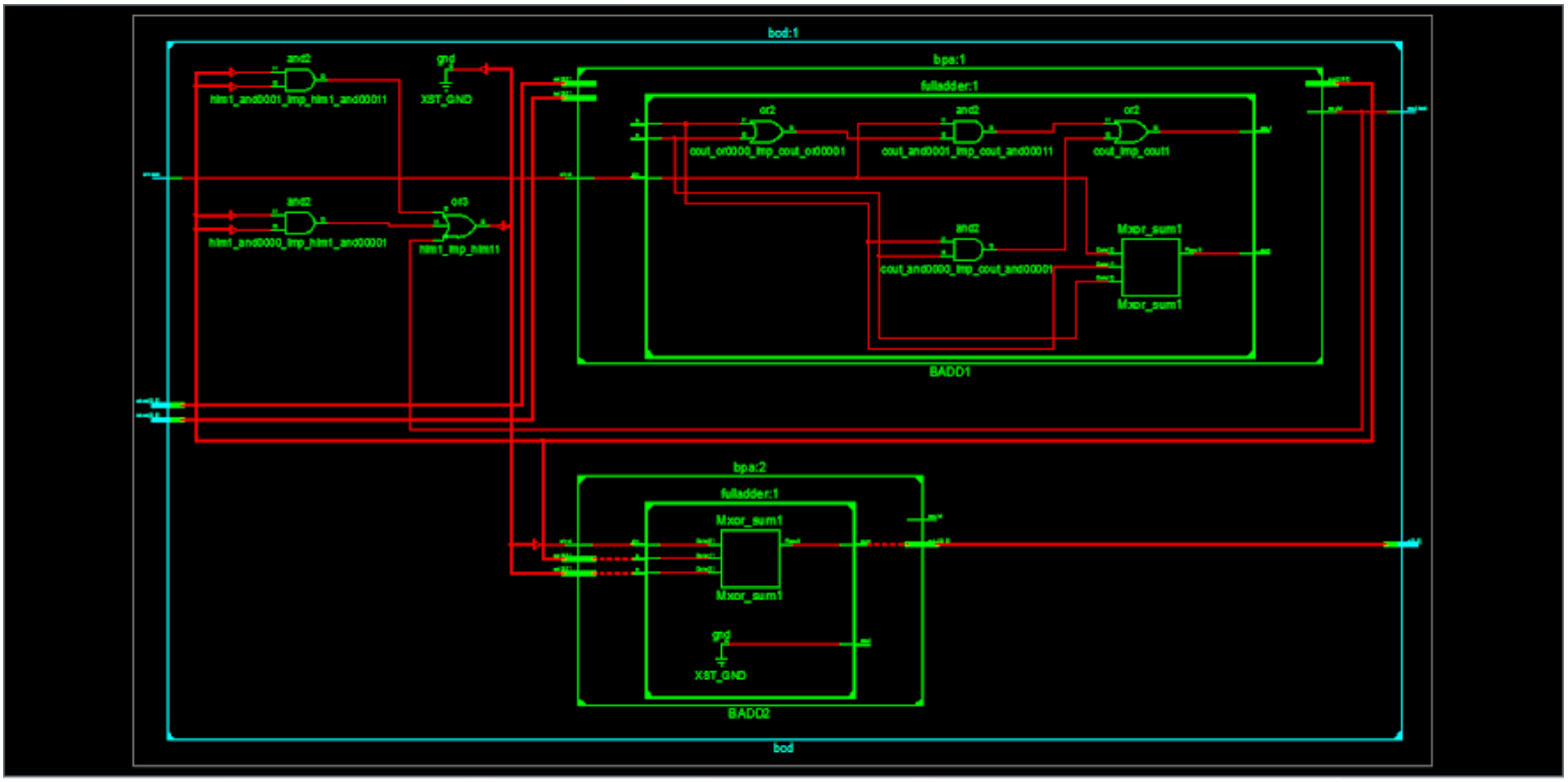
```
        abcd <= "1001"; bbcd <= "0111"; wait for 100 ns;

      wait;
   end process;

END;
```

Simulation –

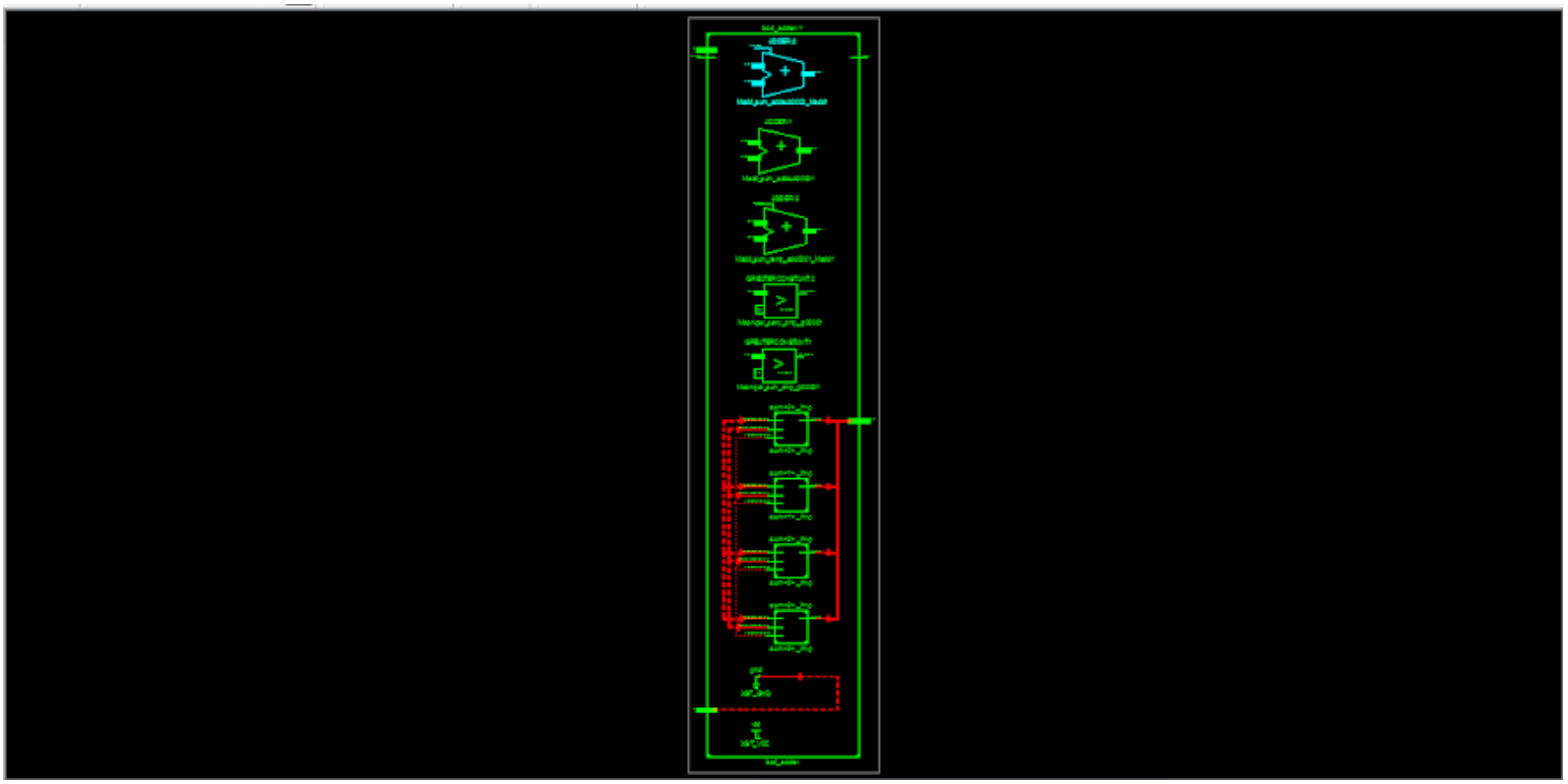


7.)c. Compare between the generated circuits after synthesis. Note down your observations.

RTL SCHEMATIC OF BCD adder using BPA:



RTL SHECMATIC OF BCD ADDER WITHOUT USING BPA:



8.) Design and simulate the behavioral model of a T flip-flop. Simulate for all possible input combinations. Note down the synthesis report.

VHDL MODULE:

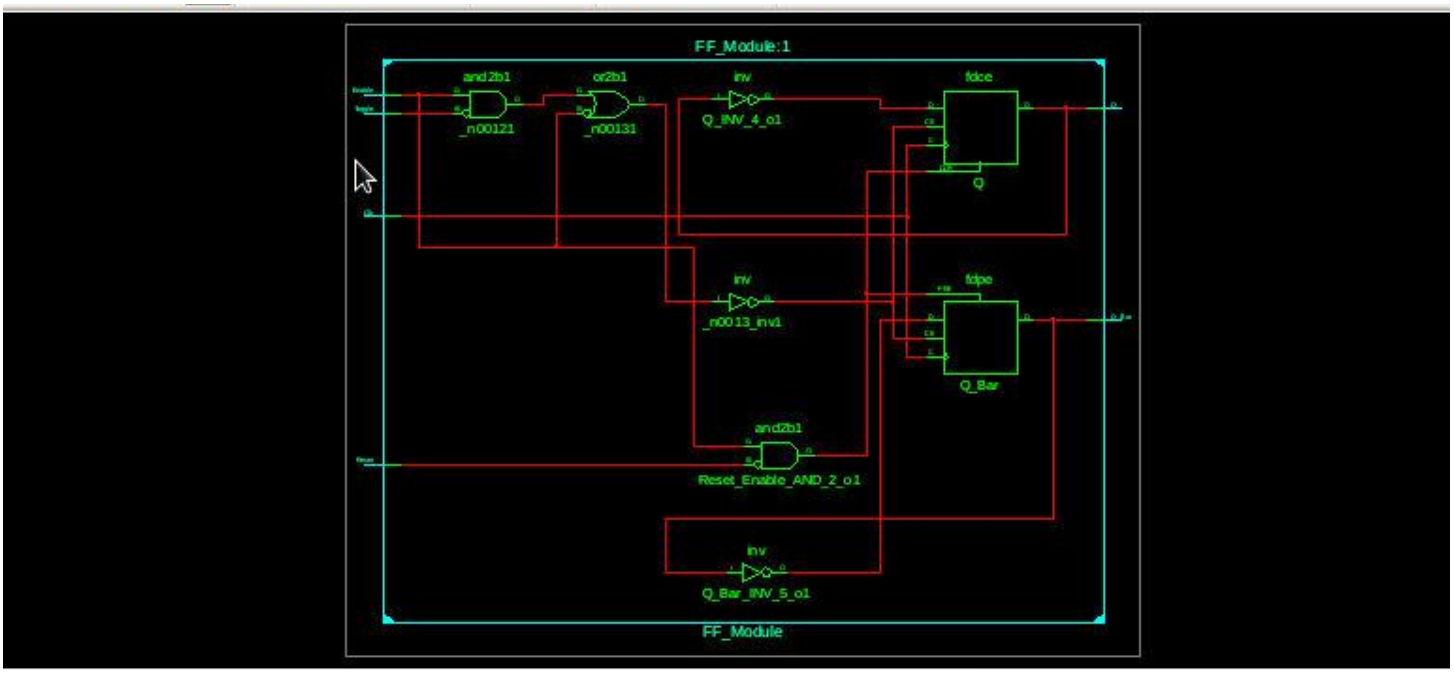
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity FF_Module is
Port ( Toggle : in STD_LOGIC;
Q : inout STD_LOGIC;
Q_Bar : inout STD_LOGIC;
Clk : in STD_LOGIC;
Enable : in STD_LOGIC;
Reset : in STD_LOGIC);
end FF_Module;
architecture Behavioral of FF_Module is
begin
process(Toggle,Clk,Enable,Enable,Reset)
begin
if (Enable='1')
then
if (Reset='0')
then
Q <= '0';
Q_Bar <= '1';
elsif(rising_edge(Clk))
then
if(Toggle='1')
then
Q <= not Q;
Q_Bar <= not Q_Bar;
end if;
end if;
end if;
end process;
end Behavioral;
```

TEST BENCH:

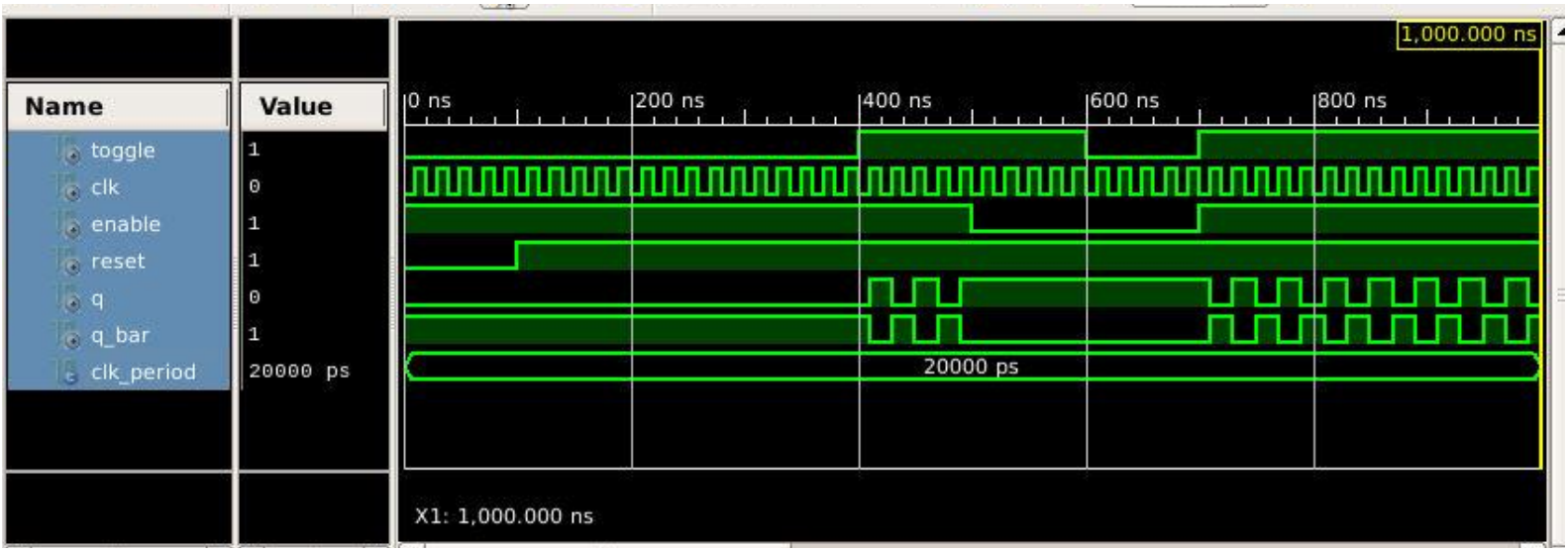
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY T_FF_Impl IS
END T_FF_Impl;
ARCHITECTURE behavior OF T_FF_Impl IS
-- Component Declaration for the Unit Under Test (UUT)
COMPONENT FF_Module
PORT(
Toggle : IN std_logic;
Q : INOUT std_logic;
Q_Bar : INOUT std_logic;
Clk : IN std_logic;
Enable : IN std_logic;
Reset : IN std_logic
);
END COMPONENT;
--Inputs
signal Toggle : std_logic := '0';
```

```
signal Clk : std_logic := '0';
signal Enable : std_logic := '0';
signal Reset : std_logic := '0';
--BiDirs
signal Q : std_logic;
signal Q_Bar : std_logic;
-- Clock period definitio
constant Clk_period : time := 20 ns;
BEGIN
-- Instantiate the Unit Under Test (UUT)
uut: FF_Module PORT MAP (
Toggle => Toggle,
Q => Q,
Q_Bar => Q_Bar,
Clk => Clk,
Enable => Enable,
Reset => Reset
);
-- Clock process definitions
Clk_process :process
begin
Clk <= '0';
wait for Clk_period/2;
Clk <= '1';
wait for Clk_period/2;
end process;
-- Stimulus process
stim_proc: process
begin
-- hold reset state for 100 ns.
Enable<='1';
Reset <= '0';
wait for 100 ns;
Reset<='1';
wait for Clk_period*10;
Toggle <= '0';
wait for 100 ns;
Toggle <= '1';
wait for 100 ns;
Enable <= '0';
Toggle <= '1';
wait for 100 ns;
Toggle <= '0';
wait for 100 ns;
Enable <= '1';
Toggle <= '1';
-- insert stimulus here
wait;
end process;
END;
```

RTL Schematic –



Simulation –



Synthesis Report:

Release 14.7 - xst P.20160913 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.04 secs
-->
Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.04 secs
-->
Reading design: FF_Module.prj
TABLE OF CONTENTS
1) Synthesis Options Summary
2) HDL Parsing

==========
* Synthesis Options Summary *
==========
---- Source Parameters
Input File Name : "FF_Module.prj"
Ignore Synthesis Constraint File : NO
---- Target Parameters
Output File Name : "FF_Module"
Output Format : NGC
Target Device : xc6slx4-3-tqg144
---- Source Options
Top Module Name : FF_Module
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No
---- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES
---- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO

```
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5
=========================================================================
=========================================================================
* HDL Parsing *
=========================================================================
Parsing VHDL file "/home/ise/Xilinx_ISE_Mera/T_FF/FF_Module.vhd" into library work
Parsing entity <FF_Module>.
Parsing architecture <Behavioral> of entity <ff_module>.
=========================================================================
* HDL Elaboration *
=========================================================================
Elaborating entity <FF_Module> (architecture <Behavioral>) from library <work>.
=========================================================================
* HDL Synthesis *
=========================================================================
Synthesizing Unit <FF_Module>.
Related source file is "/home/ise/Xilinx_ISE_Mera/T_FF/FF_Module.vhd".
Found 1-bit register for signal <Q>.
Found 1-bit register for signal <Q_Bar>.
Summary:
inferred 2 Dtype
flip-flop(s).
Unit <FF_Module> synthesized.
=========================================================================
HDL Synthesis Report
Macro Statistics
# Registers : 2
1-bit register : 2
=========================================================================
=========================================================================
* Advanced HDL Synthesis *
=========================================================================
=========================================================================
Advanced HDL Synthesis Report
Macro Statistics
# Registers : 2
Flip-Flops : 2
=========================================================================
=========================================================================
* Low Level Synthesis *
=========================================================================
Optimizing unit <FF_Module> ...
INFO:Xst:3203 - The FF/Latch <Q> in Unit <FF_Module> is the opposite to the following
FF/Latch, which will be removed : <Q_Bar>
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block FF_Module, actual ratio is 0.
Final Macro Processing ...
=========================================================================
Final Register Report
Macro Statistics
# Registers : 1
Flip-Flops : 1
=========================================================================
=========================================================================
* Partition Report *
=========================================================================
Partition Implementation Status
-------------------------------
No Partitions were found in this design.
```

==========
* Design Summary *
==========
Top Level Output File Name : FF_Module.ngc
Primitive and Black Box Usage:

BELS : 3
INV : 1
LUT2 : 2
FlipFlops/Latches : 1
FDCE : 1
Clock Buffers : 1
BUFGP : 1
IO Buffers : 5
IBUF : 3
OBUF : 2
Device utilization summary:

Selected Device : 6slx4tqg144-3
Slice Logic Utilization:
Number of Slice Registers: 1 out of 4800 0%
Number of Slice LUTs: 3 out of 2400 0%
Number used as Logic: 3 out of 2400 0%
Slice Logic Distribution:
Number of LUT Flip Flop pairs used: 4
Number with an unused Flip Flop: 3 out of 4 75%
Number with an unused LUT: 1 out of 4 25%
Number of fully used LUT-FF pairs: 0 out of 4 0%
Number of unique control sets: 1
IO Utilization:
Number of IOs: 6
Number of bonded IOBs: 6 out of 102 5%
Specific Feature Utilization:
Number of BUFG/BUFGCTRLs: 1 out of 16 6%

Partition Resource Summary:

No Partitions were found in this design.

==========
Timing Report
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.
Clock Information:

---+---+---+
Clock Signal | Clock buffer(FF name) | Load |
---+---+---+
Clk | BUFGP | 1 |
---+---+---+
Asynchronous Control Signals Information:

No asynchronous control signals found in this design
Timing Summary:

Speed Grade: -3
Minimum period: 1.988ns (Maximum Frequency: 503.145MHz)
Minimum input arrival time before clock: 3.118ns
Maximum output required time after clock: 4.457ns
Maximum combinational path delay: No path found
Timing Details:

All values displayed in nanoseconds (ns)
==========
Timing constraint: Default period analysis for Clock 'Clk'

Clock period: 1.988ns (frequency: 503.145MHz)
Total number of paths / destination ports: 1 / 1

Delay: 1.988ns (Levels of Logic = 1)
Source: Q (FF)
Destination: Q (FF)
Source Clock: Clk rising
Destination Clock: Clk rising
Data Path: Q to Q
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)

FDCE:C->Q 2 0.447 0.616 Q (Q_OBUF)
INV:I->O 2 0.206 0.616 Q_INV_4_o1_INV_0 (Q_Bar_OBUF)
FDCE:D 0.102 Q

Total 1.988ns (0.755ns logic, 1.233ns route)
(38.0% logic, 62.0% route)
==========
Timing constraint: Default OFFSET IN BEFORE for Clock 'Clk'
Total number of paths / destination ports: 4 / 2

Offset: 3.118ns (Levels of Logic = 2)
Source: Reset (PAD)
Destination: Q (FF)
Destination Clock: Clk rising
Data Path: Reset to Q
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O 1 1.222 0.684 Reset_IBUF (Reset_IBUF)
LUT2:I0->O 1 0.203 0.579 Reset_Enable_AND_2_o1 (Reset_Enable_AND_2_o)
FDCE:CLR 0.430 Q

Total 3.118ns (1.855ns logic, 1.263ns route)
(59.5% logic, 40.5% route)
==========
Timing constraint: Default OFFSET OUT AFTER for Clock 'Clk'
Total number of paths / destination ports: 2 / 2

Offset: 4.457ns (Levels of Logic = 2)
Source: Q (FF)
Destination: Q_Bar (PAD)
Source Clock: Clk rising
Data Path: Q to Q_Bar
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)

FDCE:C->Q 2 0.447 0.616 Q (Q_OBUF)
INV:I->O 2 0.206 0.616 Q_INV_4_o1_INV_0 (Q_Bar_OBUF)
OBUF:I->O 2.571 Q_Bar_OBUF (Q_Bar)

Total 4.457ns (3.224ns logic, 1.233ns route)
(72.3% logic, 27.7% route)
==========
Cross Clock Domains Report:

Clock to Setup on destination clock Clk

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

Clk | 1.988| | | |

==========
Total REAL time to Xst completion: 7.00 secs
Total CPU time to Xst completion: 6.64 secs

-->
Total memory usage is 384420 kilobytes
Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 1 (0 filtered)

9.) Design and simulate the behavioral model of a D flip-flop. Simulate for all possible input combinations. Note down the synthesis report.

VHDL MODULE:

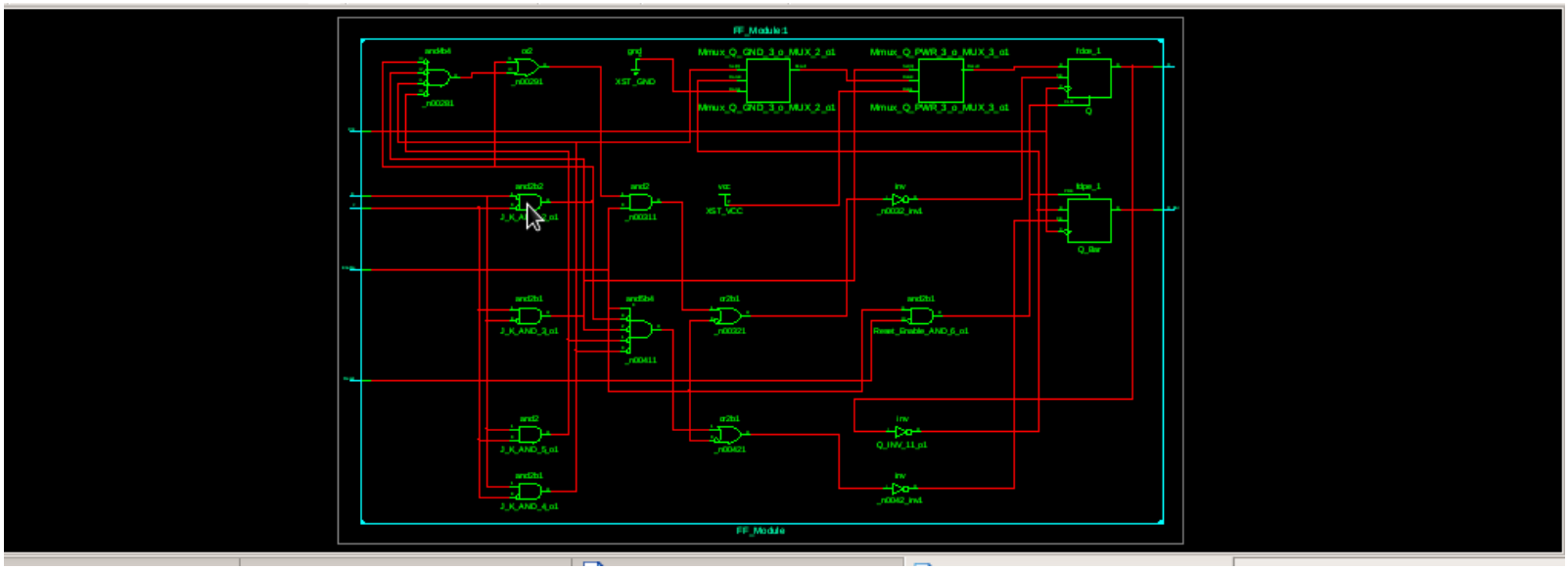
```
use IEEE.STD_LOGIC_1164.ALL;
entity FF_Module is
Port ( Enable : in STD_LOGIC;
Data : in STD_LOGIC;
Clk : in STD_LOGIC;
Reset : in STD_LOGIC;
Q : inout STD_LOGIC;
Q_Bar : inout STD_LOGIC);
end FF_Module;
architecture Behavioral of FF_Module is
begin
process(Enable,Data,Clk,Reset)
begin
if (Enable='1')
then
if (Reset='0')
then
Q <= '0';
Q_Bar <= '1';
elsif (falling_edge(Clk))
then
if (Data='0')
then
Q <= '0';
Q_Bar <= '1';
elsif (Data='1')
then
Q <= '1';
Q_Bar <= '0';
end if;
end if;
end if;
end process;
end Behavioral;
```

TEST BENCH:

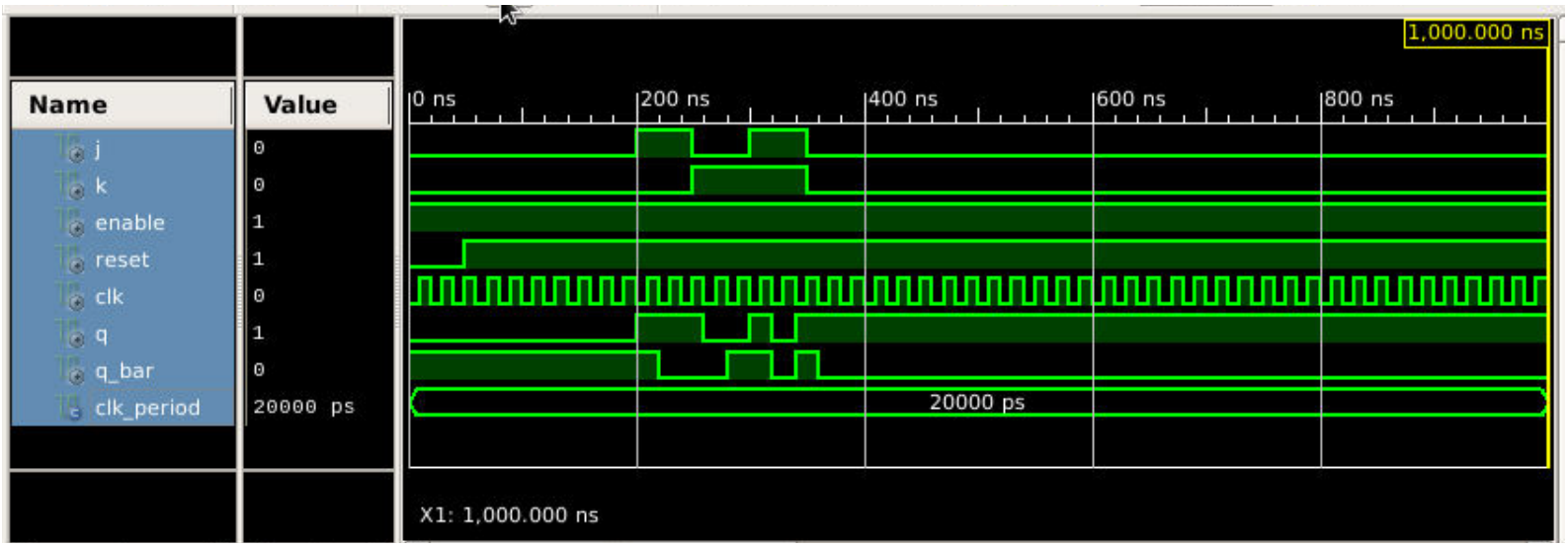
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY JK_FF_Impl IS
END JK_FF_Impl;
ARCHITECTURE behavior OF JK_FF_Impl IS
-- Component Declaration for the Unit Under Test (UUT)
```

```
COMPONENT FF_Module
PORT(
J : IN std_logic;
K : IN std_logic;
Enable : IN std_logic;
Reset : IN std_logic;
Clk : IN std_logic;
Q : INOUT std_logic;
Q_Bar : INOUT std_logic
);
END COMPONENT;
--Inputs
signal J : std_logic := '0';
signal K : std_logic := '0';
signal Enable : std_logic := '0';
signal Reset : std_logic := '0';
signal Clk : std_logic := '0';
--BiDirs
signal Q : std_logic;
signal Q_Bar : std_logic;
-- Clock period definitions
constant Clk_period : time := 20 ns;
BEGIN
-- Instantiate the Unit Under Test (UUT)
uut: FF_Module PORT MAP (
J => J,
K => K,
Enable => Enable,
Reset => Reset,
Clk => Clk,
Q => Q,
Q_Bar => Q_Bar
);
-- Clock process definitions
Clk_process :process
begin
Clk <= '0';
wait for Clk_period/2;
Clk <= '1';
wait for Clk_period/2;
end process;
-- Stimulus process
stim_proc: process
begin
Enable <='1';
Reset <='0';
-- hold reset state for 100 ns.
wait for 50 ns;
Reset <='1';
wait for Clk_period*5;
J<='0';K<='0'; wait for 50 ns;
J<='1';K<='0'; wait for 50 ns;
J<='0';K<='1'; wait for 50 ns;
J<='1';K<='1'; wait for 50 ns;
J<='0';K<='0'; wait for 50 ns;
-- insert stimulus here
wait;
end process;
END;
```

RTL Schematic –



Simulation –



Synthesis Report:

Release 14.7 - xst P.20160913 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.04 secs
-->
Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.04 secs
-->
Reading design: FF_Module.prj

TABLE OF CONTENTS

==========
* Synthesis Options Summary *
==========
---- Source Parameters
Input File Name : "FF_Module.prj"
Ignore Synthesis Constraint File : NO
---- Target Parameters
Output File Name : "FF_Module"
Output Format : NGC
Target Device : xc6slx4-3-tqg144
---- Source Options
Top Module Name : FF_Module
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No
---- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES
---- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets

Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5
===
===
* HDL Parsing *
===
Parsing VHDL file "/home/ise/Xilinx_ISE_Mera/D_FF/FF_Module.vhd" into library work
Parsing entity <FF_Module>.
Parsing architecture <Behavioral> of entity <ff_module>.
===
* HDL Elaboration *
===
Elaborating entity <FF_Module> (architecture <Behavioral>) from library <work>.
===
* HDL Synthesis *
===
Synthesizing Unit <FF_Module>.
Related source file is "/home/ise/Xilinx_ISE_Mera/D_FF/FF_Module.vhd".
Found 1-bit register for signal <Q>.
Found 1-bit register for signal <Q_Bar>.
Summary:
inferred 2 Dtype
flip-flop(s).
Unit <FF_Module> synthesized.
===
HDL Synthesis Report
Macro Statistics
Registers : 2
1-bit register : 2
===
===
* Advanced HDL Synthesis *
===
===
Advanced HDL Synthesis Report
Macro Statistics
Registers : 2
Flip-Flops : 2
===
===
* Low Level Synthesis *
===
Optimizing unit <FF_Module> ...
INFO:Xst:3203 - The FF/Latch <Q> in Unit <FF_Module> is the opposite to the following
FF/Latch, which will be removed : <Q_Bar>
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block FF_Module, actual ratio is 0.
FlipFlop Q has been replicated 1 time(s) to handle iob=true attribute.
Final Macro Processing ...
===
Final Register Report
Macro Statistics
Registers : 2
Flip-Flops : 2
===
===
* Partition Report *

```
=========================================================================
Partition Implementation Status
-------------------------------
No Partitions were found in this design.
-------------------------------
=========================================================================
* Design Summary *
=========================================================================
Top Level Output File Name : FF_Module.ngc
Primitive and Black Box Usage:
------------------------------
# BELS : 2
# INV : 1
# LUT2 : 1
# FlipFlops/Latches : 2
# FDCE_1 : 2
# Clock Buffers : 1
# BUFGP : 1
# IO Buffers : 5
# IBUF : 3
# OBUF : 2
Device utilization summary:
---------------------------
Selected Device : 6slx4tqg144-3
Slice Logic Utilization:
Number of Slice LUTs: 2 out of 2400 0%
Number used as Logic: 2 out of 2400 0%
Slice Logic Distribution:
Number of LUT Flip Flop pairs used: 2
Number with an unused Flip Flop: 2 out of 2 100%
Number with an unused LUT: 0 out of 2 0%
Number of fully used LUT-FF pairs: 0 out of 2 0%
Number of unique control sets: 1
IO Utilization:
Number of IOs: 6
Number of bonded IOBs: 6 out of 102 5%
IOB Flip Flops/Latches: 2
Specific Feature Utilization:
Number of BUFG/BUFGCTRLs: 1 out of 16 6%
---------------------------
Partition Resource Summary:
---------------------------
No Partitions were found in this design.
---------------------------
=========================================================================
Timing Report
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.
Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal | Clock buffer(FF name) | Load |
-----------------------------------+------------------------+-------+
Clk | BUFGP | 2 |
-----------------------------------+------------------------+-------+
Asynchronous Control Signals Information:
-----------------------------------------
No asynchronous control signals found in this design
Timing Summary:
---------------
Speed Grade: -3
Minimum period: No path found
Minimum input arrival time before clock: 3.155ns
Maximum output required time after clock: 4.382ns
Maximum combinational path delay: No path found
Timing Details:
```

All values displayed in nanoseconds (ns)
===
Timing constraint: Default OFFSET IN BEFORE for Clock 'Clk'
Total number of paths / destination ports: 8 / 6

Offset: 3.155ns (Levels of Logic = 2)
Source: Reset (PAD)
Destination: Q (FF)
Destination Clock: Clk falling
Data Path: Reset to Q
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-- ------------
IBUF:I->O 1 1.222 0.684 Reset_IBUF (Reset_IBUF)
LUT2:I0->O 2 0.203 0.616 Reset_Enable_AND_2_o1 (Reset_Enable_AND_2_o)
FDCE_1:CLR 0.430 Q

Total 3.155ns (1.855ns logic, 1.300ns route)
(58.8% logic, 41.2% route)
===
Timing constraint: Default OFFSET OUT AFTER for Clock 'Clk'
Total number of paths / destination ports: 2 / 2

Offset: 4.382ns (Levels of Logic = 2)
Source: Q (FF)
Destination: Q_Bar (PAD)
Source Clock: Clk falling
Data Path: Q to Q_Bar
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
-- ------------
FDCE_1:C->Q 1 0.447 0.579 Q (Q_OBUF)
INV:I->O 1 0.206 0.579 Q_inv1_INV_0 (Q_Bar_OBUF)
OBUF:I->O 2.571 Q_Bar_OBUF (Q_Bar)

Total 4.382ns (3.224ns logic, 1.158ns route)
(73.6% logic, 26.4% route)
===
Cross Clock Domains Report:

===
Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 7.41 secs
-->
Total memory usage is 482028 kilobytes
Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 1 (0 filtered)

10.) Design and simulate the behavioral model of a JK flip-flop. Simulate for all possible input combinations. Note down the synthesis report .

VHDL MODULE:

library IEEE;

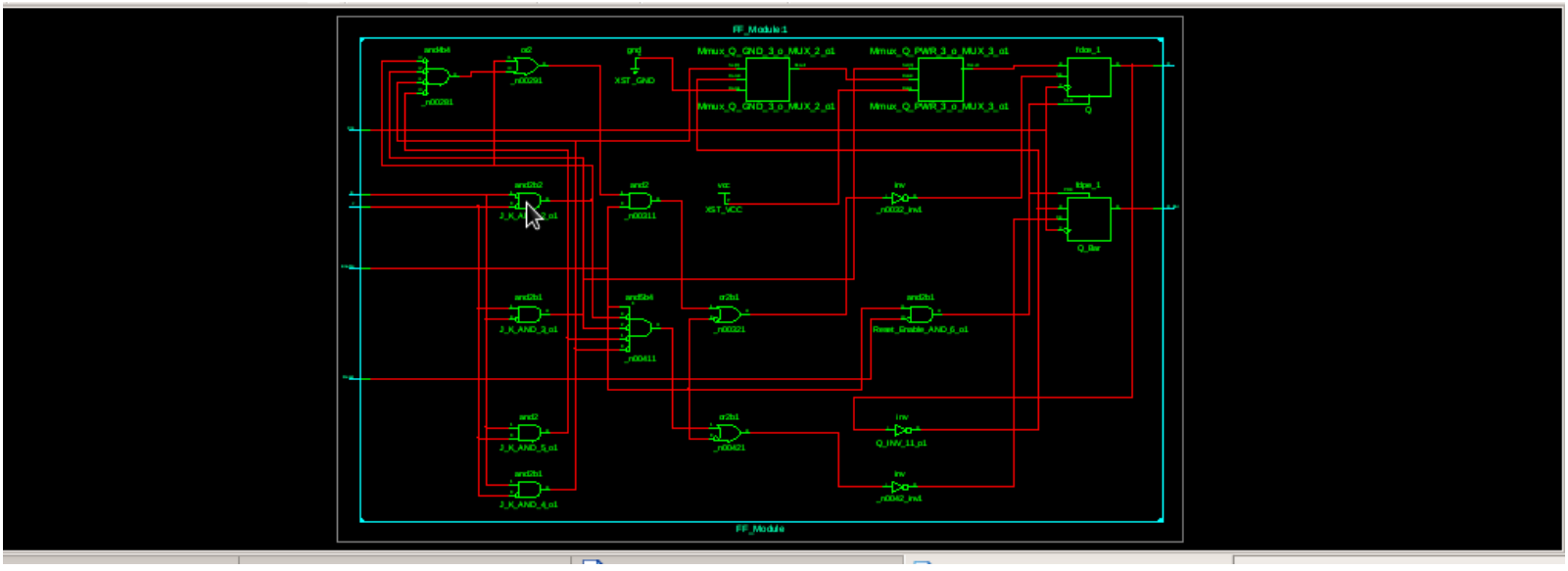
```
use IEEE.STD_LOGIC_1164.ALL;
entity FF_Module is
Port ( J,K,Enable,Reset,Clk : in STD_LOGIC;
Q,Q_Bar : inout STD_LOGIC);
end FF_Module;
architecture Behavioral of FF_Module is
begin
process(J,K,Enable,Reset,Clk)
begin
if (Enable = '1')
then
if(Reset = '0')
then
Q <= '0';
Q_Bar <= '1';
elsif(falling_edge(Clk))
then
if (J='0' and K='0')
then
Q <= Q;
Q_Bar <= not Q;
elsif(J='1' and K='0')
then
Q <= '1';
Q_Bar <= not Q;
elsif(J='0' and K='1')
then
Q <= '0';
Q_Bar <= not Q;
elsif(J='1' and K='1')
then
Q <= not Q;
Q_Bar <= not Q;
end if;
end if;
end if;
end process;
end Behavioral;
```

TEST BENCH:

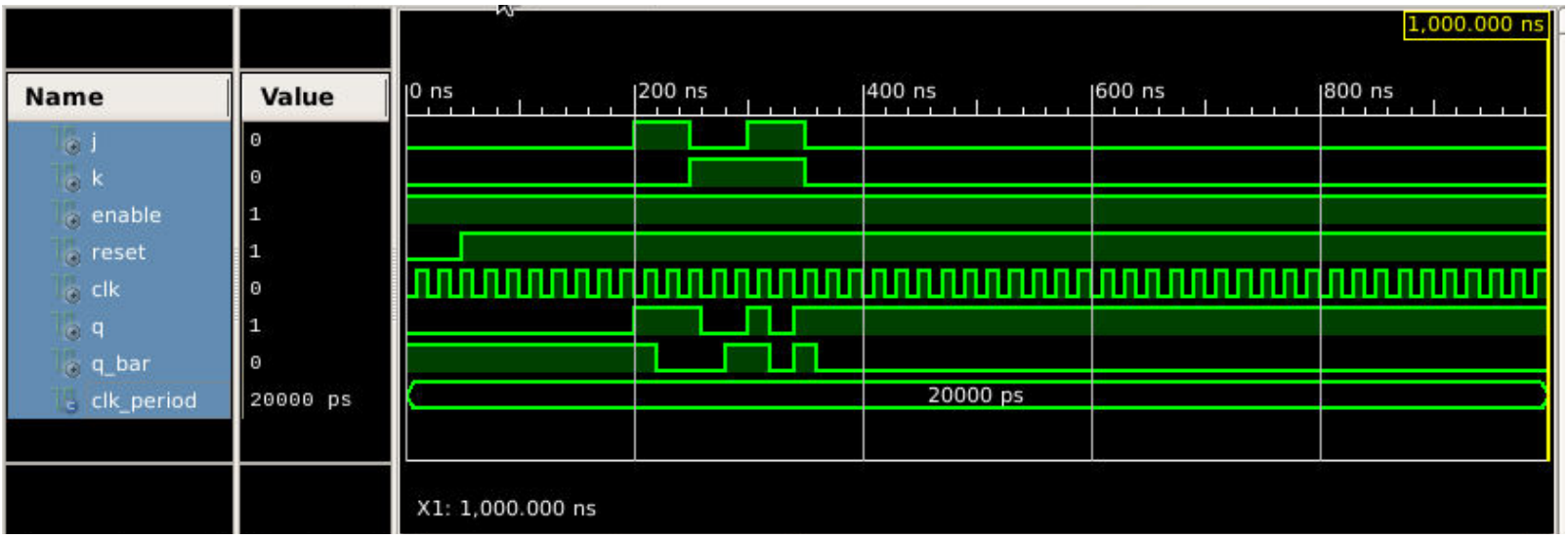
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY JK_FF_Impl IS
END JK_FF_Impl;
ARCHITECTURE behavior OF JK_FF_Impl IS
-- Component Declaration for the Unit Under Test (UUT)
COMPONENT FF_Module
PORT(
J : IN std_logic;
K : IN std_logic;
Enable : IN std_logic;
Reset : IN std_logic;
Clk : IN std_logic;
Q : INOUT std_logic;
Q_Bar : INOUT std_logic
);
END COMPONENT;
--Inputs
signal J : std_logic := '0';
signal K : std_logic := '0';
signal Enable : std_logic := '0';
signal Reset : std_logic := '0';
signal Clk : std_logic := '0';
--BiDirs
```

```
signal Q : std_logic;
signal Q_Bar : std_logic;
-- Clock period definitions
constant Clk_period : time := 20 ns;
BEGIN
-- Instantiate the Unit Under Test (UUT)
uut: FF_Module PORT MAP (
J => J,
K => K,
Enable => Enable,
Reset => Reset,
Clk => Clk,
Q => Q,
Q_Bar => Q_Bar
);
-- Clock process definitions
Clk_process :process
begin
Clk <= '0';
wait for Clk_period/2;
Clk <= '1';
wait for Clk_period/2;
end process;
-- Stimulus process
stim_proc: process
begin
Enable <='1';
Reset <='0';
-- hold reset state for 100 ns.
wait for 50 ns;
Reset <='1';
wait for Clk_period*5;
J<='0';K<='0'; wait for 50 ns;
J<='1';K<='0'; wait for 50 ns;
J<='0';K<='1'; wait for 50 ns;
J<='1';K<='1'; wait for 50 ns;
J<='0';K<='0'; wait for 50 ns;
-- insert stimulus here
wait;
end process;
END;
```

RTL Schematic –



Simulation –



Synthesis Report:

Release 14.7 - xst P.20160913 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.05 secs
-->
Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.05 secs
-->
Reading design: FF_Module.prj
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8.4.2) Asynchronous Control Signals Information
8.4.3) Timing Summary
8.4.4) Timing Details
8.4.5) Cross Clock Domains Report
===
* Synthesis Options Summary *
===
---- Source Parameters
Input File Name : "FF_Module.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters
Output File Name : "FF_Module"
Output Format : NGC
Target Device : xc6slx4-3-tqg144
---- Source Options
Top Module Name : FF_Module
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No
---- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES
---- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5
===
===
* HDL Parsing *
===
Parsing VHDL file "/home/ise/Xilinx_ISE_Mera/JK_FF/FF_Module.vhd" into library work
Parsing entity <FF_Module>.
Parsing architecture <Behavioral> of entity <ff_module>.
===
* HDL Elaboration *
===
Elaborating entity <FF_Module> (architecture <Behavioral>) from library <work>.
===
* HDL Synthesis *
===
Synthesizing Unit <FF_Module>.

Related source file is "/home/ise/Xilinx_ISE_Mera/JK_FF/FF_Module.vhd".
Found 1-bit register for signal <Q>.
Found 1-bit register for signal <Q_Bar>.
Summary:
inferred 2 Dtype
flip-flop(s).
inferred 2
Multiplexer(s).
Unit <FF_Module> synthesized.
==========
HDL Synthesis Report
Macro Statistics
Registers : 2
1-bit register : 2
Multiplexers : 2
1-bit 2-to-1 multiplexer : 2
==========
==========
* Advanced HDL Synthesis *
==========
==========
Advanced HDL Synthesis Report
Macro Statistics
Registers : 2
Flip-Flops : 2
Multiplexers : 2
1-bit 2-to-1 multiplexer : 2
==========
==========
* Low Level Synthesis *
==========
Optimizing unit <FF_Module> ...
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block FF_Module, actual ratio is 0.
Final Macro Processing ...
==========
Final Register Report
Macro Statistics
Registers : 2
Flip-Flops : 2
==========
==========
* Partition Report *
==========
Partition Implementation Status

No Partitions were found in this design.

==========
* Design Summary *
==========
Top Level Output File Name : FF_Module.ngc
Primitive and Black Box Usage:

BELS : 4
INV : 1
LUT2 : 1
LUT3 : 2
FlipFlops/Latches : 2
FDCE_1 : 1
FDPE_1 : 1
Clock Buffers : 1
BUFGP : 1
IO Buffers : 6
IBUF : 4
OBUF : 2

Device utilization summary:

Selected Device : 6slx4tqg144-3
Slice Logic Utilization:
Number of Slice Registers: 2 out of 4800 0%
Number of Slice LUTs: 4 out of 2400 0%
Number used as Logic: 4 out of 2400 0%
Slice Logic Distribution:
Number of LUT Flip Flop pairs used: 6
Number with an unused Flip Flop: 4 out of 6 66%
Number with an unused LUT: 2 out of 6 33%
Number of fully used LUT-FF pairs: 0 out of 6 0%
Number of unique control sets: 2
IO Utilization:
Number of IOs: 7
Number of bonded IOBs: 7 out of 102 6%
Specific Feature Utilization:
Number of BUFG/BUFGCTRLs: 1 out of 16 6%

Partition Resource Summary:

No Partitions were found in this design.

==========
Timing Report
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.
Clock Information:

---+---+---+
Clock Signal | Clock buffer(FF name) | Load |
---+---+---+
Clk | BUFGP | 2 |
---+---+---+
Asynchronous Control Signals Information:

No asynchronous control signals found in this design
Timing Summary:

Speed Grade: -3
Minimum period: 1.984ns (Maximum Frequency: 504.007MHz)
Minimum input arrival time before clock: 3.207ns
Maximum output required time after clock: 3.668ns
Maximum combinational path delay: No path found
Timing Details:

All values displayed in nanoseconds (ns)
==========
Timing constraint: Default period analysis for Clock 'Clk'
Clock period: 1.984ns (frequency: 504.007MHz)
Total number of paths / destination ports: 2 / 2

Delay: 1.984ns (Levels of Logic = 1)
Source: Q (FF)
Destination: Q_Bar (FF)
Source Clock: Clk falling
Destination Clock: Clk falling
Data Path: Q to Q_Bar
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
--- ---
FDCE_1:C->Q 3 0.447 0.650 Q (Q_OBUF)
INV:I->O 1 0.206 0.579 Q_INV_11_o1_INV_0 (Q_INV_11_o)
FDPE_1:D 0.102 Q_Bar

Total 1.984ns (0.755ns logic, 1.229ns route)

(38.1% logic, 61.9% route)
==========
Timing constraint: Default OFFSET IN BEFORE for Clock 'Clk'
Total number of paths / destination ports: 10 / 5

Offset: 3.207ns (Levels of Logic = 2)
Source: Enable (PAD)
Destination: Q (FF)
Destination Clock: Clk falling
Data Path: Enable to Q
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)

IBUF:I->O 3 1.222 0.879 Enable_IBUF (Enable_IBUF)
LUT3:I0->O 1 0.205 0.579 _n0032_inv1 (_n0032_inv)
FDCE_1:CE 0.322 Q

Total 3.207ns (1.749ns logic, 1.458ns route)
(54.5% logic, 45.5% route)
==========
Timing constraint: Default OFFSET OUT AFTER for Clock 'Clk'
Total number of paths / destination ports: 2 / 2

Offset: 3.668ns (Levels of Logic = 1)
Source: Q (FF)
Destination: Q (PAD)
Source Clock: Clk falling
Data Path: Q to Q
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)

FDCE_1:C->Q 3 0.447 0.650 Q (Q_OBUF)
OBUF:I->O 2.571 Q_OBUF (Q)

Total 3.668ns (3.018ns logic, 0.650ns route)
(82.3% logic, 17.7% route)
==========
Cross Clock Domains Report:

Clock to Setup on destination clock Clk
---+---+---+---+---+
| Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---+---+---+---+---+
Clk | | | 1.984| |
---+---+---+---+---+
==========
Total REAL time to Xst completion: 10.00 secs
Total CPU time to Xst completion: 7.41 secs
-->
Total memory usage is 482092 kilobytes
Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)

11.) a. Design and simulate the behavioral model of a 4-bit UP/DOWN counter.

VHDL MODULE:

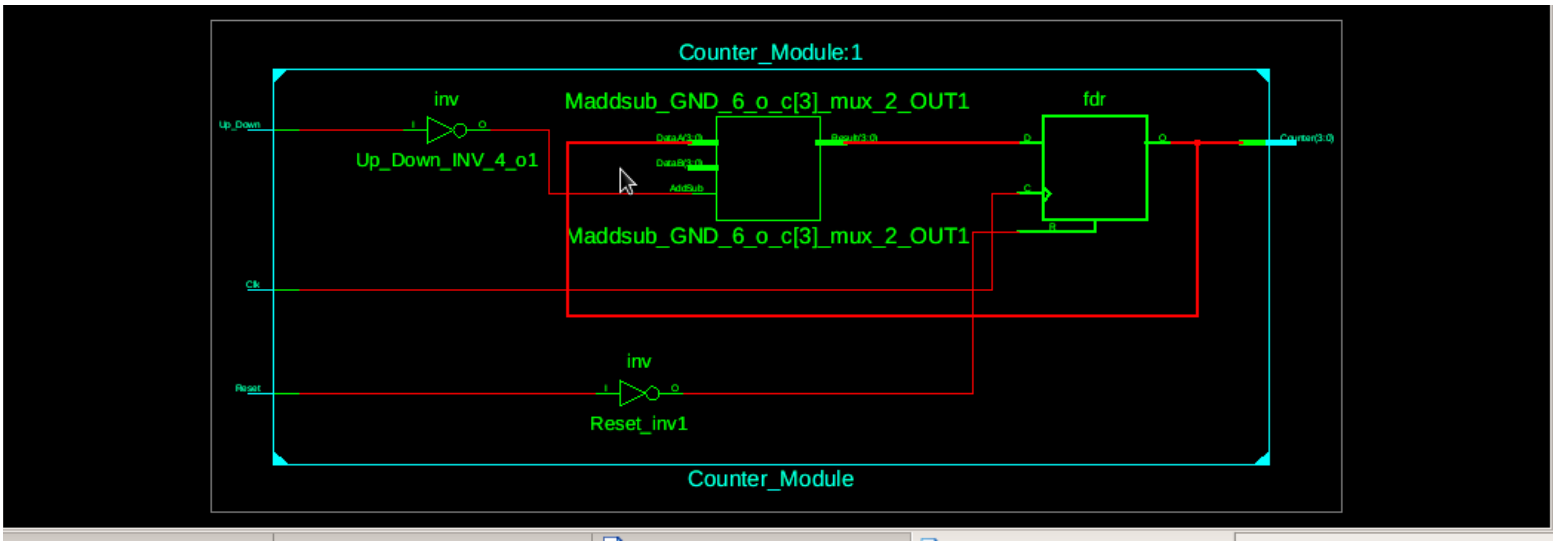
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;
entity Counter_Module is
Port ( Up_Down : in STD_LOGIC;
Clk : in STD_LOGIC;
Reset : in STD_LOGIC;
Counter : out STD_LOGIC_VECTOR (3 downto 0));
end Counter_Module;
architecture Behavioral of Counter_Module is
signal c : STD_LOGIC_VECTOR(3 downto 0);
begin
process(Up_Down,Clk,Reset)
begin
if (rising_edge(clk))
then
if (Reset='0')
then
c<=x"0";
elsif (Up_Down='0')
then
c <= c+x"1";
else
c <= c-x"1";
end if;
end if;
end process;
Counter <= c;
end Behavioral;
```

TEST BENCH:

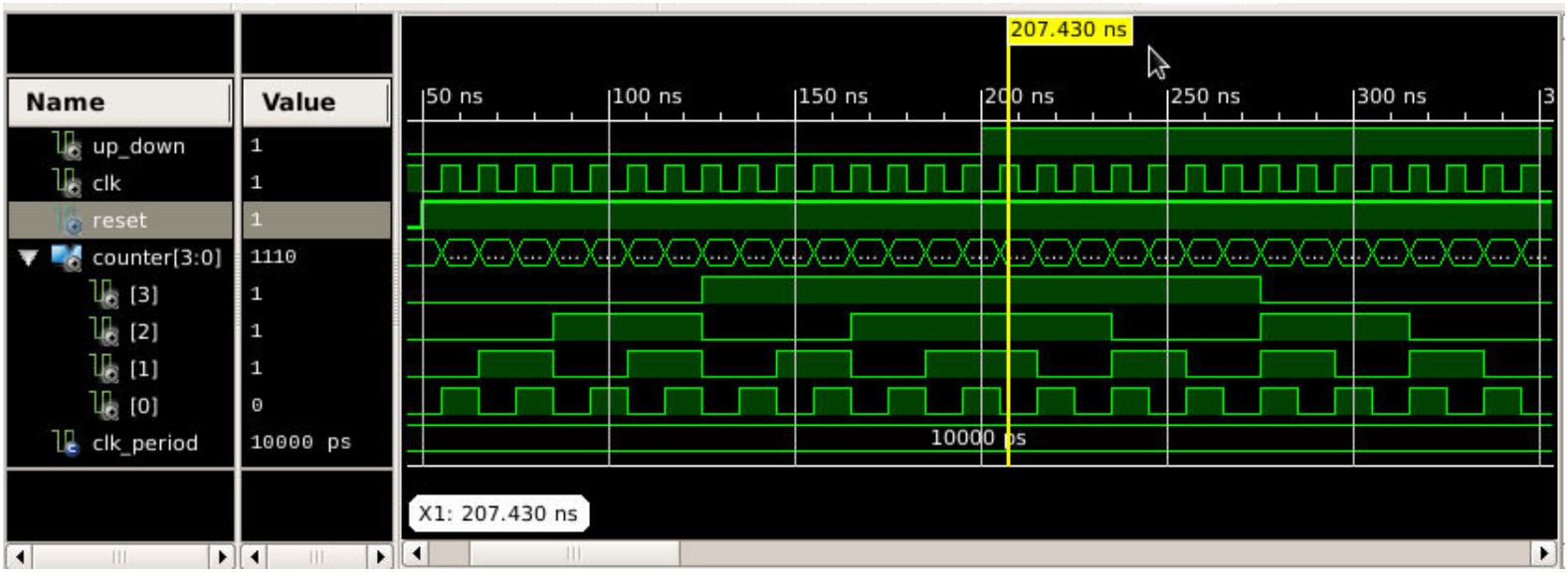
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY Counter_Impl IS
END Counter_Impl;
ARCHITECTURE behavior OF Counter_Impl IS
-- Component Declaration for the Unit Under Test (UUT)
COMPONENT Counter_Module
PORT(
Up_Down : IN std_logic;
Clk : IN std_logic;
Reset : IN std_logic;
Counter : OUT std_logic_vector(3 downto 0)
);
END COMPONENT;
--Inputs
signal Up_Down : std_logic := '0';
signal Clk : std_logic := '0';
signal Reset : std_logic := '0';
--Outputs
signal Counter : std_logic_vector(3 downto 0);
-- Clock period definitions
constant Clk_period : time := 10 ns;
BEGIN
-- Instantiate the Unit Under Test (UUT)
uut: Counter_Module PORT MAP (
Up_Down => Up_Down,
Clk => Clk,
Reset => Reset,
Counter => Counter
```

```
);
-- Clock process definitions
Clk_process :process
begin
Clk <= '0';
wait for Clk_period/2;
Clk <= '1';
wait for Clk_period/2;
end process;
-- Stimulus process
stim_proc: process
begin
Reset <= '0';
-- hold reset state for 100 ns.
wait for 50 ns;
Reset <= '1';
Up_Down <= '0';
wait for Clk_period*15;
Up_Down <= '1';
-- insert stimulus here
wait;
end process;
END;
```

RTL Schematic –



Simulation –



Synthesis Report:

Release 14.7 - xst P.20160913 (lin64)
Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.
-->
Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.05 secs
-->
Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.05 secs
-->
Reading design: Counter_Module.prj
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8.4.3) Timing Summary
8.4.4) Timing Details
8.4.5) Cross Clock Domains Report
===
* Synthesis Options Summary *
===
---- Source Parameters
Input File Name : "Counter_Module.prj"
Ignore Synthesis Constraint File : NO
---- Target Parameters
Output File Name : "Counter_Module"
Output Format : NGC
Target Device : xc6slx4-3-tqg144
---- Source Options

Top Module Name : Counter_Module
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No
---- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES
---- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5
===
===
* HDL Parsing *
===
Parsing VHDL file "/home/ise/Xilinx_ISE_Mera/Counter/Counter_Module.vhd" into library
work
Parsing entity <Counter_Module>.
Parsing architecture <Behavioral> of entity <counter_module>.
===
* HDL Elaboration *
===
Elaborating entity <Counter_Module> (architecture <Behavioral>) from library <work>.
===
* HDL Synthesis *
===
Synthesizing Unit <Counter_Module>.
Related source file is "/home/ise/Xilinx_ISE_Mera/Counter/Counter_Module.vhd".
Found 4-bit register for signal <Counter>.
Found 4-bit adder for signal <c[3]_GND_6_o_add_0_OUT> created at line 52.
Found 4-bit subtractor for signal <GND_6_o_GND_6_o_sub_2_OUT<3:0>> created at line

54.
Summary:
inferred 1
Adder/Subtractor(s).
inferred 4 Dtype
flip-flop(s).
Unit <Counter_Module> synthesized.
===
HDL Synthesis Report
Macro Statistics
Adders/Subtractors : 1
4-bit addsub : 1
Registers : 1
4-bit register : 1
===
===
* Advanced HDL Synthesis *
===
Synthesizing (advanced) Unit <Counter_Module>.
The following registers are absorbed into counter <c>: 1 register on signal <c>.
Unit <Counter_Module> synthesized (advanced).
===
Advanced HDL Synthesis Report
Macro Statistics
Counters : 1
4-bit updown counter : 1
===
===
* Low Level Synthesis *
===
Optimizing unit <Counter_Module> ...
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block Counter_Module, actual ratio is 0.
Final Macro Processing ...
===
Final Register Report
Macro Statistics
Registers : 4
Flip-Flops : 4
===
===
* Partition Report *
===
Partition Implementation Status

No Partitions were found in this design.

===
* Design Summary *
===
Top Level Output File Name : Counter_Module.ngc
Primitive and Black Box Usage:

BELS : 5
INV : 2
LUT3 : 1
LUT4 : 1
LUT5 : 1
FlipFlops/Latches : 4
FDR : 4
Clock Buffers : 1
BUFGP : 1
IO Buffers : 6
IBUF : 2
OBUF : 4
Device utilization summary:

Selected Device : 6slx4tqg144-3
Slice Logic Utilization:
Number of Slice Registers: 4 out of 4800 0%
Number of Slice LUTs: 5 out of 2400 0%
Number used as Logic: 5 out of 2400 0%
Slice Logic Distribution:
Number of LUT Flip Flop pairs used: 9
Number with an unused Flip Flop: 5 out of 9 55%
Number with an unused LUT: 4 out of 9 44%
Number of fully used LUT-FF pairs: 0 out of 9 0%
Number of unique control sets: 1
IO Utilization:
Number of IOs: 7
Number of bonded IOBs: 7 out of 102 6%
Specific Feature Utilization:
Number of BUFG/BUFGCTRLs: 1 out of 16 6%

Partition Resource Summary:

No Partitions were found in this design.

==========
Timing Report
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.
Clock Information:

---+---+---+
Clock Signal | Clock buffer(FF name) | Load |
---+---+---+
Clk | BUFGP | 4 |
---+---+---+
Asynchronous Control Signals Information:

No asynchronous control signals found in this design
Timing Summary:

Speed Grade: -3
Minimum period: 2.048ns (Maximum Frequency: 488.317MHz)
Minimum input arrival time before clock: 3.119ns
Maximum output required time after clock: 3.732ns
Maximum combinational path delay: No path found
Timing Details:

All values displayed in nanoseconds (ns)
==========
Timing constraint: Default period analysis for Clock 'Clk'
Clock period: 2.048ns (frequency: 488.317MHz)
Total number of paths / destination ports: 10 / 4

Delay: 2.048ns (Levels of Logic = 1)
Source: c_0 (FF)
Destination: c_0 (FF)
Source Clock: Clk rising
Destination Clock: Clk rising
Data Path: c_0 to c_0
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
--- ---
FDR:C->Q 5 0.447 0.714 c_0 (c_0)
INV:I->O 1 0.206 0.579 Result<0>1_INV_0 (Result<0>)
FDR:D 0.102 c_0

Total 2.048ns (0.755ns logic, 1.293ns route)
(36.9% logic, 63.1% route)

```
==========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'Clk'
Total number of paths / destination ports: 7 / 7
--------------------------------------------------------------------------
Offset: 3.119ns (Levels of Logic = 2)
Source: Reset (PAD)
Destination: c_0 (FF)
Destination Clock: Clk rising
Data Path: Reset to c_0
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
---------------------------------------- ------------
IBUF:I->O 1 1.222 0.579 Reset_IBUF (Reset_IBUF)
INV:I->O 4 0.206 0.683 Reset_inv1_INV_0 (Reset_inv)
FDR:R 0.430 c_0
----------------------------------------
Total 3.119ns (1.858ns logic, 1.261ns route)
(59.6% logic, 40.4% route)
==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'Clk'
Total number of paths / destination ports: 4 / 4
--------------------------------------------------------------------------
Offset: 3.732ns (Levels of Logic = 1)
Source: c_0 (FF)
Destination: Counter<0> (PAD)
Source Clock: Clk rising
Data Path: c_0 to Counter<0>
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
---------------------------------------- ------------
FDR:C->Q 5 0.447 0.714 c_0 (c_0)
OBUF:I->O 2.571 Counter_0_OBUF (Counter<0>)
----------------------------------------
Total 3.732ns (3.018ns logic, 0.714ns route)
(80.9% logic, 19.1% route)
==========================================================================
Cross Clock Domains Report:
--------------------------
Clock to Setup on destination clock Clk
---------------+---------+---------+---------+---------+
| Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
Clk | 2.048| | | |
---------------+---------+---------+---------+---------+
==========================================================================
Total REAL time to Xst completion: 8.00 secs
Total CPU time to Xst completion: 6.87 secs
-->
Total memory usage is 387608 kilobytes
Number of errors : 0 ( 0 filtered)
Number of warnings : 0 ( 0 filtered)
Number of infos : 0 ( 0 filtered)
```

11.)b. Modify the above counter program to make it a DECADE counter .

VHDL MODULE:

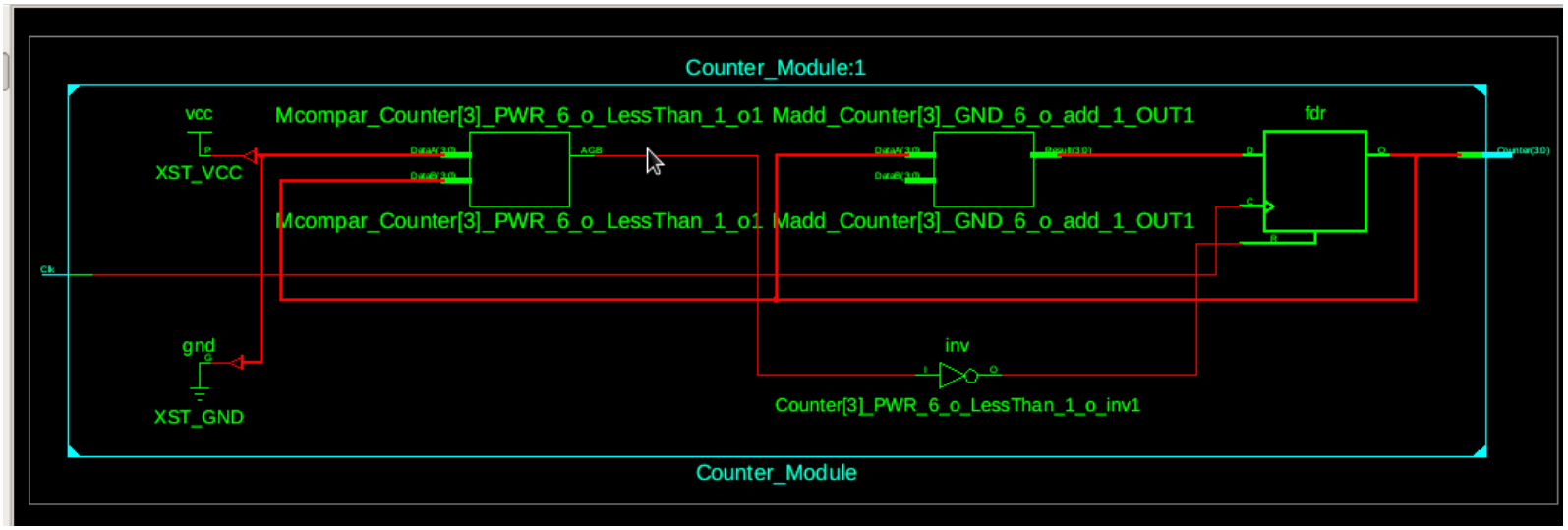
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use IEEE.NUMERIC_STD.ALL;
entity Counter_Module is
Port ( Clk : in STD_LOGIC;
Counter : inout STD_LOGIC_VECTOR (3 downto 0):="0000");
end Counter_Module;
architecture Behavioral of Counter_Module is
begin
process(Clk)
begin
if(clk'event and clk='1')
then
if (Counter<9)
then
Counter<=Counter+1;
else
Counter<="0000";
end if;
end if;
end process;
end Behavioral;
```

TEST BENCH:

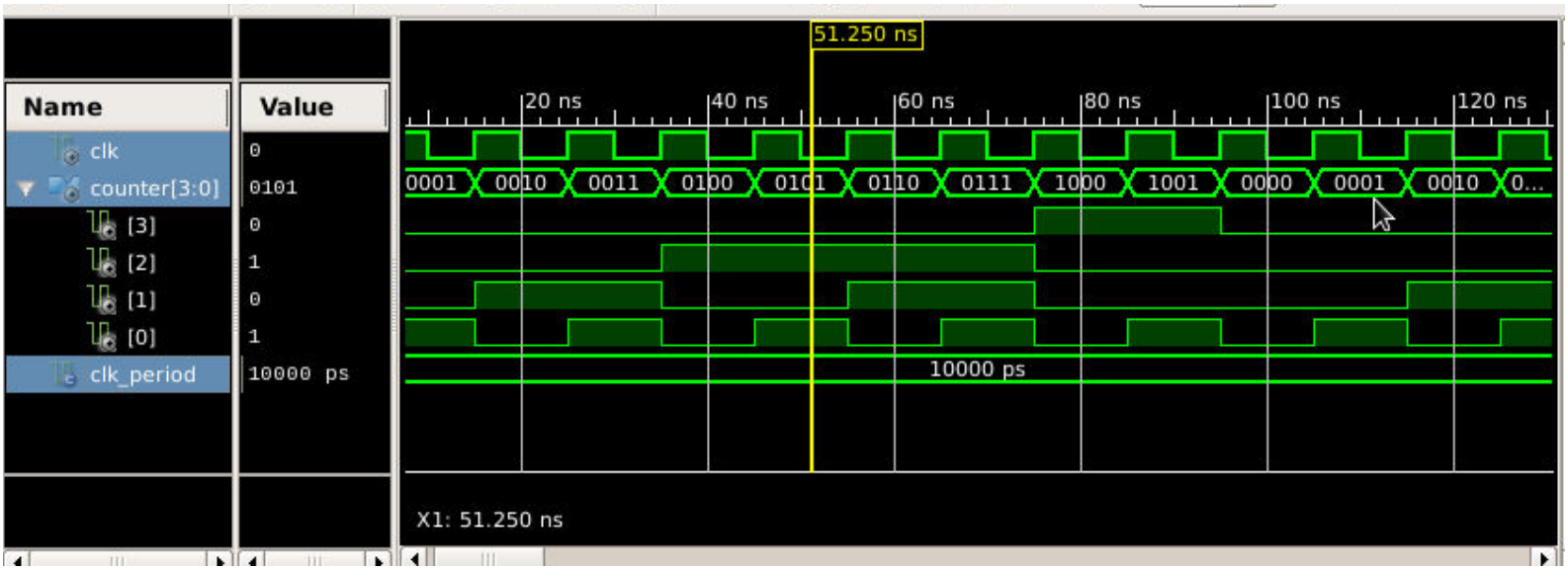
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY Counter_Impl IS
END Counter_Impl;
ARCHITECTURE behavior OF Counter_Impl IS
-- Component Declaration for the Unit Under Test (UUT)
COMPONENT Counter_Module
PORT(
Clk : IN std_logic;
Counter : INOUT std_logic_vector(3 downto 0)
);
END COMPONENT;
--Inputs
signal Clk : std_logic := '0';
--Outputs
signal Counter : std_logic_vector(3 downto 0);
-- Clock period definitions
constant Clk_period : time := 10 ns;
BEGIN
-- Instantiate the Unit Under Test (UUT)
uut: Counter_Module PORT MAP (
Clk => Clk,
Counter => Counter
```

```
);
-- Clock process definitions
Clk_process :process
begin
Clk <= '0';
wait for Clk_period/2;
Clk <= '1';
wait for Clk_period/2;
end process;
-- Stimulus process
stim_proc: process
begin
-- hold reset state for 100 ns.
wait for 20 ns;
wait for Clk_period*10;
-- insert stimulus here
wait;
end process;
END;
```

RTL Schematic –



Simulation –



Synthesis Report:

Release 14.7 - xst P.20160913 (lin64)
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-->
Parameter TMPDIR set to xst/projnav.tmp
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.05 secs
-->
Parameter xsthdpdir set to xst
Total REAL time to Xst completion: 0.00 secs
Total CPU time to Xst completion: 0.05 secs
-->
Reading design: Counter_Module.prj
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8.4.3) Timing Summary
8.4.4) Timing Details
8.4.5) Cross Clock Domains Report
===
* Synthesis Options Summary *
===
---- Source Parameters
Input File Name : "Counter_Module.prj"
Ignore Synthesis Constraint File : NO

---- Target Parameters
Output File Name : "Counter_Module"
Output Format : NGC
Target Device : xc6slx4-3-csg225
---- Source Options
Top Module Name : Counter_Module
Automatic FSM Extraction : YES
FSM Encoding Algorithm : Auto
Safe Implementation : No
FSM Style : LUT
RAM Extraction : Yes
RAM Style : Auto
ROM Extraction : Yes
Shift Register Extraction : YES
ROM Style : Auto
Resource Sharing : YES
Asynchronous To Synchronous : NO
Shift Register Minimum Size : 2
Use DSP Block : Auto
Automatic Register Balancing : No
---- Target Options
LUT Combining : Auto
Reduce Control Sets : Auto
Add IO Buffers : YES
Global Maximum Fanout : 100000
Add Generic Clock Buffer(BUFG) : 16
Register Duplication : YES
Optimize Instantiated Primitives : NO
Use Clock Enable : Auto
Use Synchronous Set : Auto
Use Synchronous Reset : Auto
Pack IO Registers into IOBs : Auto
Equivalent register Removal : YES
---- General Options
Optimization Goal : Speed
Optimization Effort : 1
Power Reduction : NO
Keep Hierarchy : No
Netlist Hierarchy : As_Optimized
RTL Output : Yes
Global Optimization : AllClockNets
Read Cores : YES
Write Timing Constraints : NO
Cross Clock Analysis : NO
Hierarchy Separator : /
Bus Delimiter : <>
Case Specifier : Maintain
Slice Utilization Ratio : 100
BRAM Utilization Ratio : 100
DSP48 Utilization Ratio : 100
Auto BRAM Packing : NO
Slice Utilization Ratio Delta : 5
===
===
* HDL Parsing *
===
Parsing VHDL file "/home/ise/Xilinx_ISE_Mera/Decade_Counter/Counter_Module.vhd" into library work
Parsing entity <Counter_Module>.
Parsing architecture <Behavioral> of entity <counter_module>.
===
* HDL Elaboration *
===
Elaborating entity <Counter_Module> (architecture <Behavioral>) from library <work>.
===
* HDL Synthesis *
===

Synthesizing Unit <Counter_Module>.
Related source file is
"/home/ise/Xilinx_ISE_Mera/Decade_Counter/Counter_Module.vhd".
Found 4-bit register for signal <Counter>.
Found 4-bit adder for signal <Counter[3]_GND_6_o_add_1_OUT> created at line 46.
Found 4-bit comparator greater for signal <Counter[3]_PWR_6_o_LessThan_1_o> created
at line 44
Summary:
inferred 1
Adder/Subtractor(s).
inferred 4 Dtype
flip-flop(s).
inferred 1
Comparator(s).
Unit <Counter_Module> synthesized.
==========
HDL Synthesis Report
Macro Statistics
Adders/Subtractors : 1
4-bit adder : 1
Registers : 1
4-bit register : 1
Comparators : 1
4-bit comparator greater : 1
==========
==========
* Advanced HDL Synthesis *
==========
Synthesizing (advanced) Unit <Counter_Module>.
The following registers are absorbed into counter <Counter>: 1 register on signal <Counter>.
Unit <Counter_Module> synthesized (advanced).
==========
Advanced HDL Synthesis Report
Macro Statistics
Counters : 1
4-bit up counter : 1
Comparators : 1
4-bit comparator greater : 1
==========
==========
* Low Level Synthesis *
==========
Optimizing unit <Counter_Module> ...
Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block Counter_Module, actual ratio is 0.
Final Macro Processing ...
==========
Final Register Report
Macro Statistics
Registers : 4
Flip-Flops : 4
==========
==========
* Partition Report *
==========
Partition Implementation Status

No Partitions were found in this design.

==========
* Design Summary *
==========
Top Level Output File Name : Counter_Module.ngc
Primitive and Black Box Usage:

BELS : 4

LUT3 : 1
LUT4 : 3
FlipFlops/Latches : 4
FD : 4
Clock Buffers : 1
BUFGP : 1
IO Buffers : 4
OBUF : 4
Device utilization summary:

Selected Device : 6slx4csg225-3
Slice Logic Utilization:
Number of Slice Registers: 4 out of 4800 0%
Number of Slice LUTs: 4 out of 2400 0%
Number used as Logic: 4 out of 2400 0%
Slice Logic Distribution:
Number of LUT Flip Flop pairs used: 8
Number with an unused Flip Flop: 4 out of 8 50%
Number with an unused LUT: 4 out of 8 50%
Number of fully used LUT-FF pairs: 0 out of 8 0%
Number of unique control sets: 1
IO Utilization:
Number of IOs: 5
Number of bonded IOBs: 5 out of 132 3%
Specific Feature Utilization:
Number of BUFG/BUFGCTRLs: 1 out of 16 6%

Partition Resource Summary:

No Partitions were found in this design.

==========
Timing Report
NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.
Clock Information:

---+---+---+
Clock Signal | Clock buffer(FF name) | Load |
---+---+---+
Clk | BUFGP | 4 |
---+---+---+
Asynchronous Control Signals Information:

No asynchronous control signals found in this design
Timing Summary:

Speed Grade: -3
Minimum period: 1.714ns (Maximum Frequency: 583.431MHz)
Minimum input arrival time before clock: No path found
Maximum output required time after clock: 3.732ns
Maximum combinational path delay: No path found
Timing Details:

All values displayed in nanoseconds (ns)
==========
Timing constraint: Default period analysis for Clock 'Clk'
Clock period: 1.714ns (frequency: 583.431MHz)
Total number of paths / destination ports: 15 / 4

Delay: 1.714ns (Levels of Logic = 1)
Source: Counter_0 (FF)
Destination: Counter_0 (FF)
Source Clock: Clk rising
Destination Clock: Clk rising
Data Path: Counter_0 to Counter_0

Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
---------- ------------
FD:C->Q 5 0.447 0.962 Counter_0 (Counter_0)
LUT4:I0->O 1 0.203 0.000 Counter_0_rstpot (Counter_0_rstpot)
FD:D 0.102 Counter_0

Total 1.714ns (0.752ns logic, 0.962ns route)
(43.9% logic, 56.1% route)
==========
Timing constraint: Default OFFSET OUT AFTER for Clock 'Clk'
Total number of paths / destination ports: 4 / 4

Offset: 3.732ns (Levels of Logic = 1)
Source: Counter_3 (FF)
Destination: Counter<3> (PAD)
Source Clock: Clk rising
Data Path: Counter_3 to Counter<3>
Gate Net
Cell:in->out fanout Delay Delay Logical Name (Net Name)
---------- ------------
FD:C->Q 5 0.447 0.714 Counter_3 (Counter_3)
OBUF:I->O 2.571 Counter_3_OBUF (Counter<3>)

Total 3.732ns (3.018ns logic, 0.714ns route)
(80.9% logic, 19.1% route)
==========
Cross Clock Domains Report:

Clock to Setup on destination clock Clk
---+---+---+---+---+
| Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---+---+---+---+---+
Clk | 1.714| | | |
---+---+---+---+---+
==========
Total REAL time to Xst completion: 7.00 secs
Total CPU time to Xst completion: 6.79 secs
-->
Total memory usage is 484536 kilobytes
Number of errors : 0 (0 filtered)
Number of warnings : 0 (0 filtered)
Number of infos : 0 (0 filtered)