IT 451: Computer Organization and Architecture (Sessional)

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Assignment 3

Question 1

VHDL MODULE :

```
library IEEE;

use IEEE.STD_LOGIC_1164.ALL;

use IEEE.NUMERIC_STD.ALL;

use ieee.std_logic_unsigned.all;

entity convertor is

Port ( ip : in  STD_LOGIC_VECTOR (3 downto 0);

sel : in  STD_LOGIC_VECTOR (2 downto 0);

op : out  STD_LOGIC_VECTOR (3 downto 0));

end convertor;

architecture Behavioral of convertor is

signal bin2ex3 : std_logic_vector(3 downto 0);

signal ex32bin : std_logic_vector(3 downto 0);

begin
```

```
bin2ex3<=ip+3;
ex32bin<=ip-3;
op(0) <= ip(0) xor ip(1)
        when sel="000" else   --binary2gray
ip(0) xor ip(1) xor ip(2) xor ip(3)
        when sel="001" else
bin2ex3(0)
        when sel="010" else
ex32bin(0)   when sel="011";     -- else


op(1) <=ip(2) xor ip(1)
        when sel="000" else
ip(2) xor ip(1) xor ip(3)
                when sel="001" else
bin2ex3(1)
        when sel="010" else
ex32bin(1)
         when sel="011" ;

op(2) <=ip(3) xor ip(2)
        when sel="000" else
 ip(3) xor ip(2)
        when sel="001" else
bin2ex3(2)
        when sel="010" else
ex32bin(2)
```

```
            when sel="011";



op(3) <=ip(3)
            when sel="000" else
 ip(3)
            when sel="001" else
bin2ex3(3)
            when sel="010" else
ex32bin(3)
            when sel="011";


end Behavioral;
```

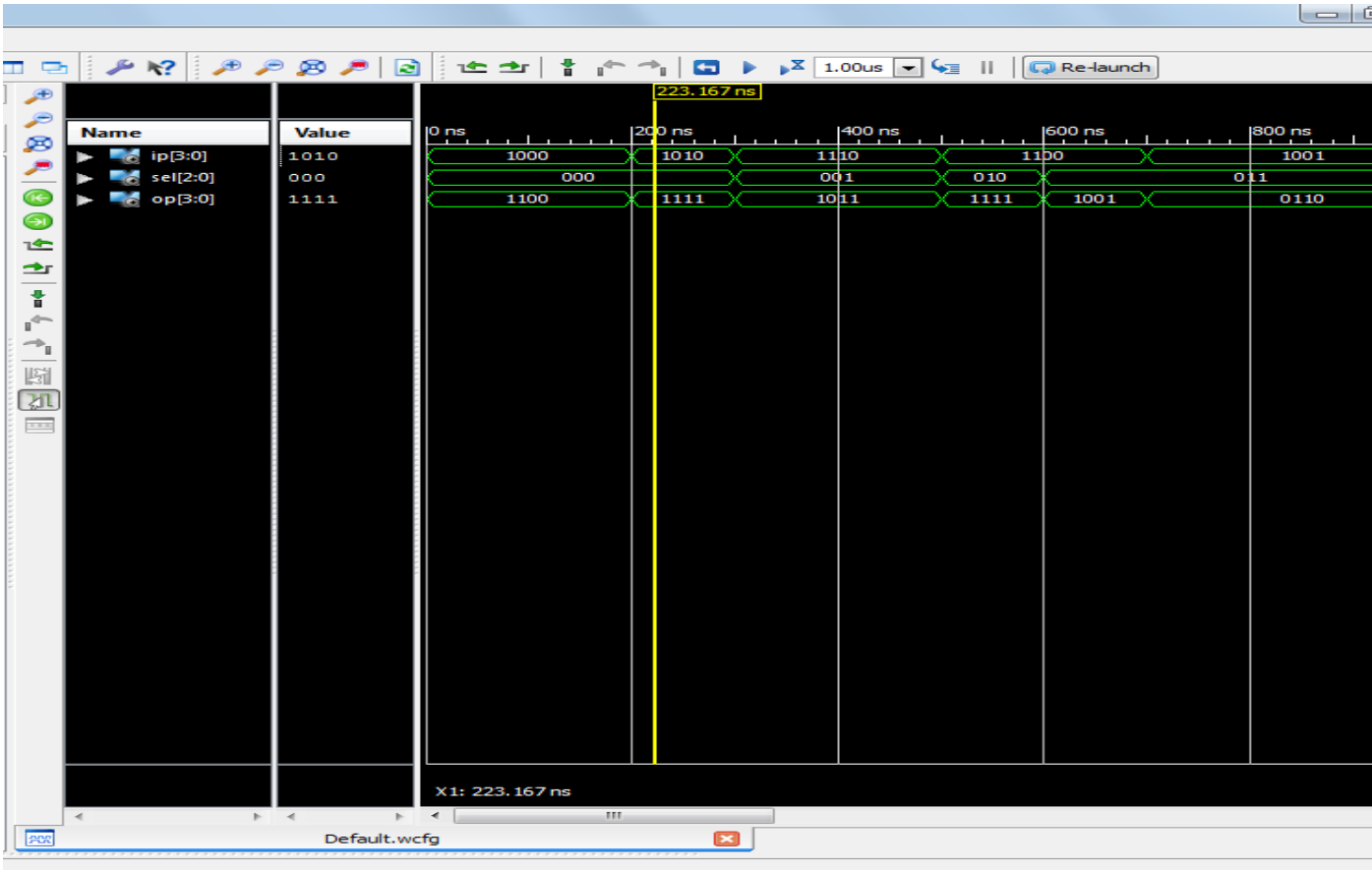
TEST BENCH :

```
LIBRARY ieee;

USE ieee.std_logic_1164.ALL;


-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--USE ieee.numeric_std.ALL;


ENTITY cnvrt_test IS

END cnvrt_test;


ARCHITECTURE behavior OF cnvrt_test IS


   -- Component Declaration for the Unit Under Test (UUT)
```

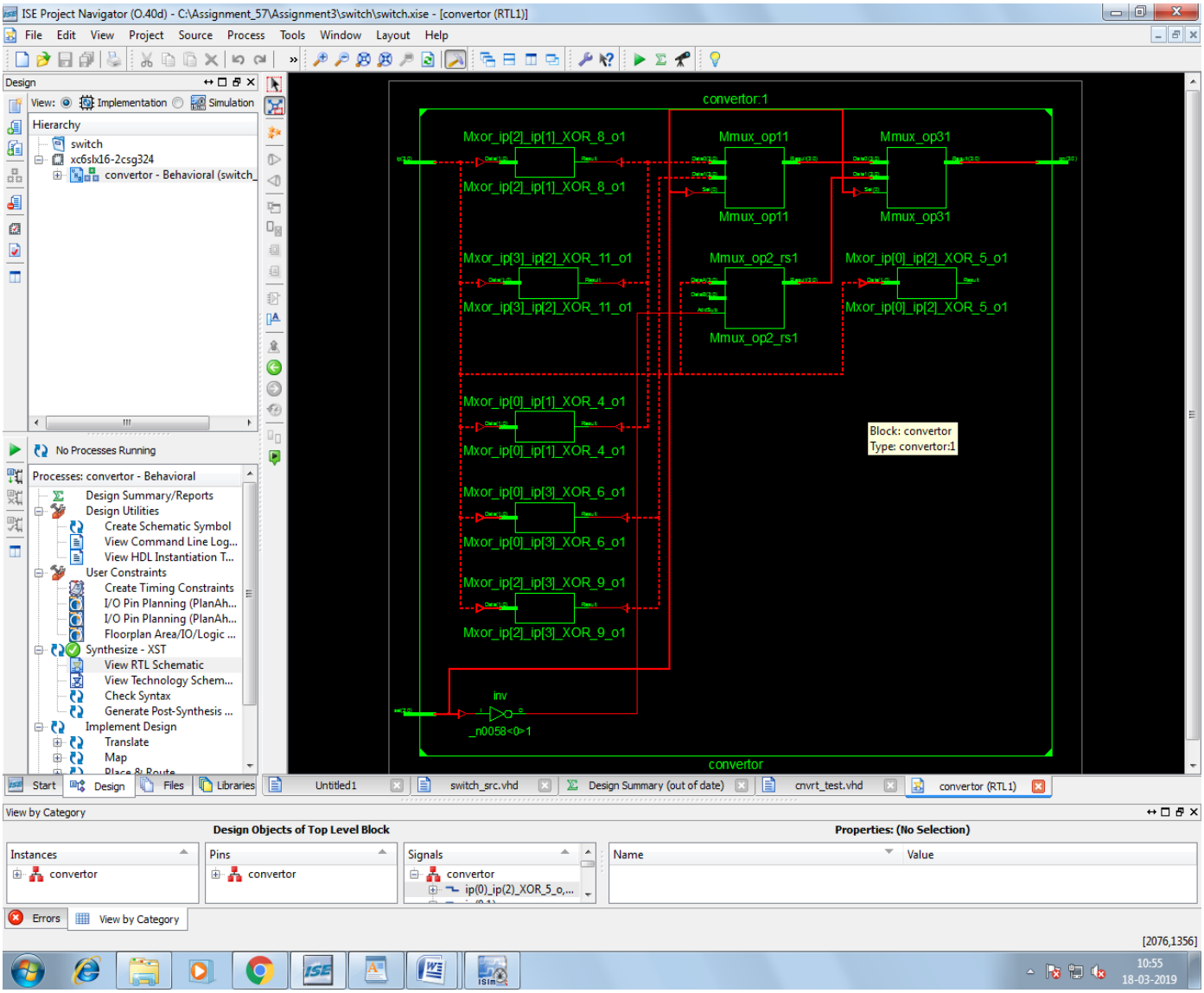
```
  COMPONENT convertor
  PORT(
      ip : IN  std_logic_vector(3 downto 0);
      sel : IN  std_logic_vector(2 downto 0);
      op : OUT  std_logic_vector(3 downto 0)
     );
  END COMPONENT;


  --Inputs
  signal ip : std_logic_vector(3 downto 0) := (others => '0');
  signal sel : std_logic_vector(2 downto 0) := (others => '0');

          --Outputs
  signal op : std_logic_vector(3 downto 0);
  -- No clocks detected in port list. Replace <clock> below with
  -- appropriate port name

  --constant <clock>_period : time := 10 ns;

BEGIN

          -- Instantiate the Unit Under Test (UUT)
  uut: convertor PORT MAP (
        ip => ip,
        sel => sel,
```

```
        op => op

       );


  -- Clock process definitions

 --




  -- Stimulus process

  stim_proc: process

  begin

     -- hold reset state for 100 ns.

    -- wait for 100 ns;


   --  wait for <clock>_period*10;


     -- insert stimulus here

            ip<= "1000","1010" after 200 ns,"1110" after 300 ns, "1100" after 500 ns,"1001" after 700
ns;

            sel <= "000", "001" after 300 ns, "010" after 500 ns,"011" after 600 ns;

     wait;

  end process;


END;
```

Simulation -


223.167 ns
Name
Value
ip[3:0]
1010
sel[2:0]
000
op[3:0]
1111
0 ns
200 ns
400 ns
600 ns
800 ns
1000
1010
1110
1100
1001
000
001
010
011
1100
1111
1011
1111
1001
0110
X1: 223.167 ns
Default.wcfg
1.00us
Re-launch

RTL Schematic –



Question 2

VHDL MODULE :

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
use ieee.STD_LOGIC_UNSIGNED.all;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity mult is
```

```
    Port ( a : in  STD_LOGIC_VECTOR (7 downto 0);
           b : in  STD_LOGIC_VECTOR (7 downto 0);
           c : out  STD_LOGIC_VECTOR (15 downto 0));
end mult;

architecture Behavioral of mult is

begin
c<=a*b;

end Behavioral;
```

TEST BENCH :

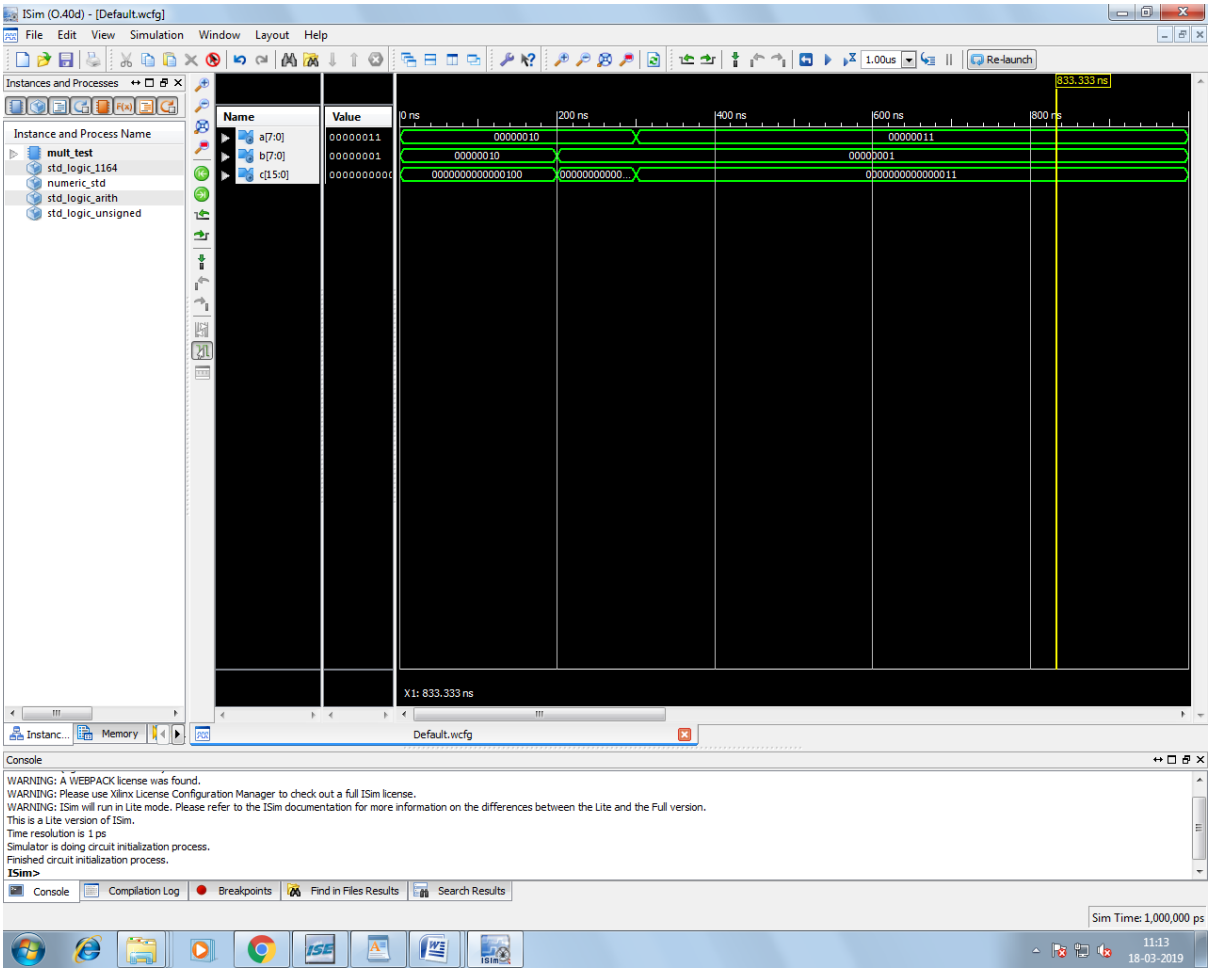
```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--USE ieee.numeric_std.ALL;

ENTITY mult_test IS
END mult_test;

ARCHITECTURE behavior OF mult_test IS

    -- Component Declaration for the Unit Under Test (UUT)
```

```
  COMPONENT mult
  PORT(
      a : IN  std_logic_vector(7 downto 0);
      b : IN  std_logic_vector(7 downto 0);
      c : OUT  std_logic_vector(15 downto 0)
     );
  END COMPONENT;



  --Inputs
  signal a : std_logic_vector(7 downto 0) := "00000010";
  signal b : std_logic_vector(7 downto 0) := "00000010";

          --Outputs
  signal c : std_logic_vector(15 downto 0);
  -- No clocks detected in port list. Replace <clock> below with
  -- appropriate port name

  --constant <clock>_period : time := 10 ns;

BEGIN

          -- Instantiate the Unit Under Test (UUT)
  uut: mult PORT MAP (
       a => a,
       b => b,
       c => c
```

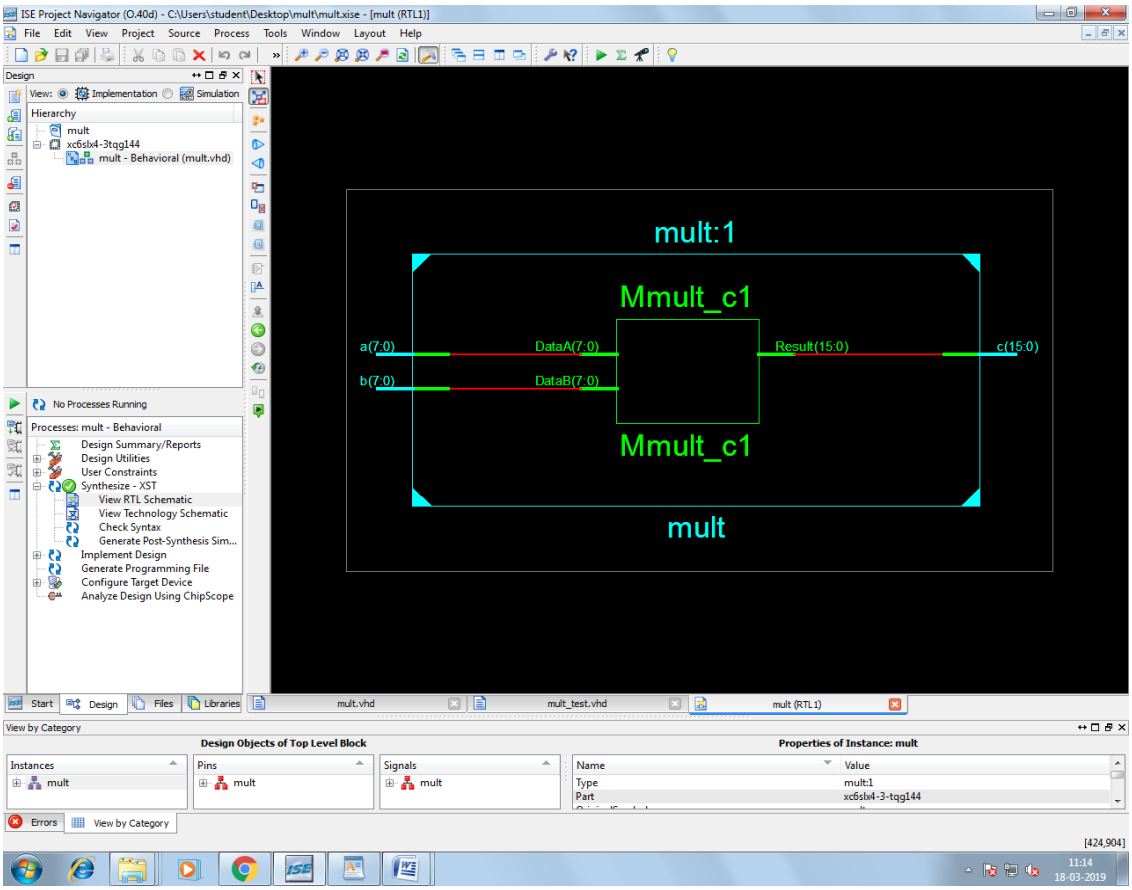
```
      );


  -- Clock process definitions
 -- <clock>_process :process
 --  begin
                    --<clock> <= '0';
          --        wait for <clock>_period/2;
          --        <clock> <= '1';
          --        wait for <clock>_period/2;
--   end process;



  -- Stimulus process
  stim_proc: process
  begin
    -- hold reset state for 100 ns.
    wait for 100 ns;
                    a<="00000011" after 200 ns;
                    b<="00000001" after 100 ns;

   -- wait for <clock>_period*10;

    -- insert stimulus here

    wait;
  end process;
```

END;

Simulation -



RTL Schematic –



Question 3

VHDL MODULE :

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity divider is
   Port ( dividend : in  STD_LOGIC_VECTOR (31 downto 0);
          divisor : in  STD_LOGIC_VECTOR (15 downto 0);
          quotient : out  STD_LOGIC_VECTOR (31 downto 0));
end divider;

architecture Behavioral of divider is

begin
quotient <= std_logic_vector(to_signed(to_integer(signed(dividend) / signed(divisor)),32));

end Behavioral;
```

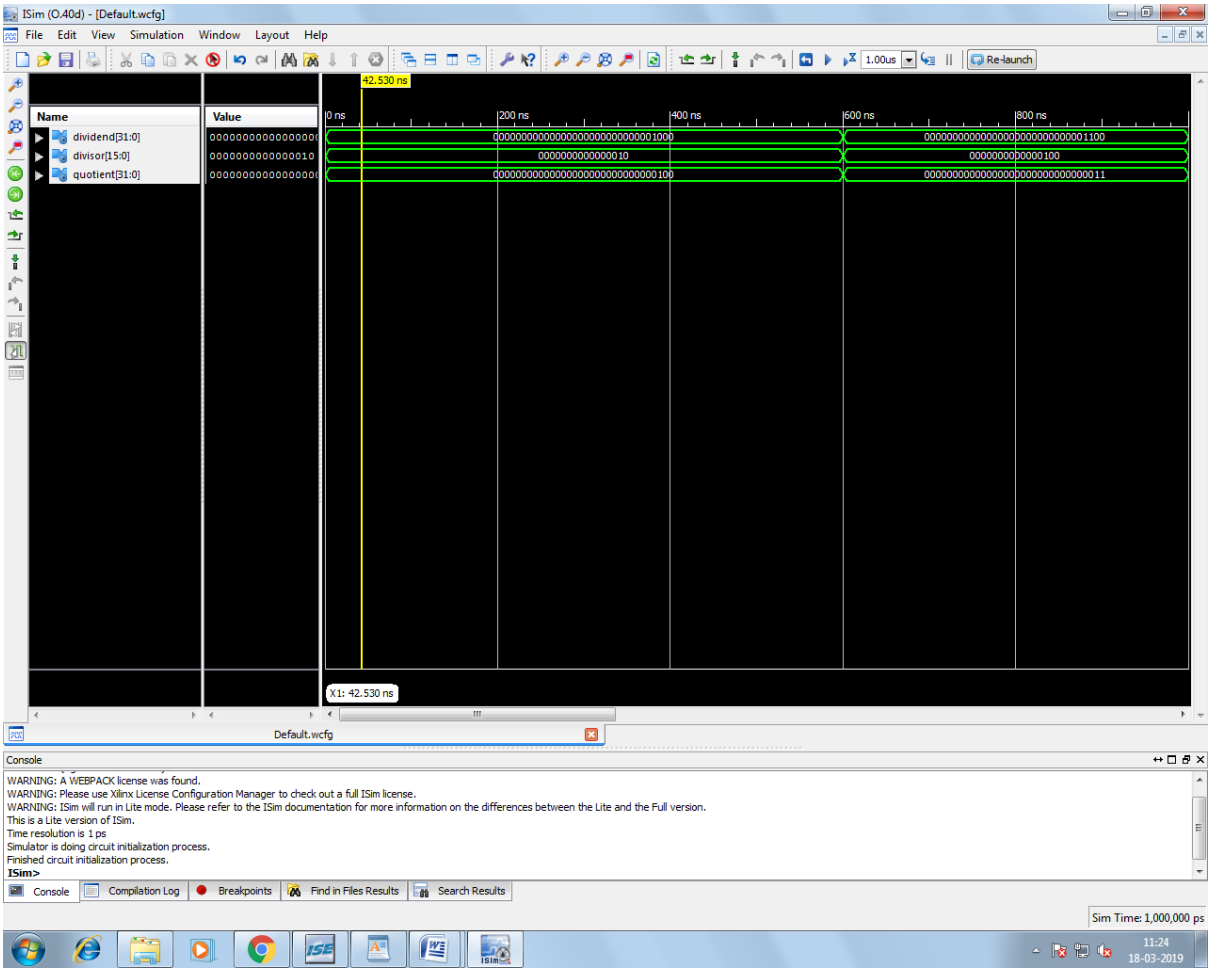
TEST BENCH :

```
LIBRARY ieee;

USE ieee.std_logic_1164.ALL;


-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--USE ieee.numeric_std.ALL;


ENTITY divider_test IS

END divider_test;


ARCHITECTURE behavior OF divider_test IS


   -- Component Declaration for the Unit Under Test (UUT)


   COMPONENT divider

   PORT(

        dividend : IN  std_logic_vector(31 downto 0);

        divisor : IN  std_logic_vector(15 downto 0);

        quotient : OUT  std_logic_vector(31 downto 0)

       );

   END COMPONENT;



  --Inputs

  signal dividend : std_logic_vector(31 downto 0) :=  "00000000000000000000000000001000";
```

```
  signal divisor : std_logic_vector(15 downto 0) := "0000000000000010";


          --Outputs
  signal quotient : std_logic_vector(31 downto 0);
  -- No clocks detected in port list. Replace <clock> below with
  -- appropriate port name

 --  constant <clock>_period : time := 10 ns;

BEGIN

          -- Instantiate the Unit Under Test (UUT)
  uut: divider PORT MAP (
        dividend => dividend,
        divisor => divisor,
        quotient => quotient
       );

  -- Clock process definitions
--   <clock>_process :process
  -- begin
          --        <clock> <= '0';
                    --wait for <clock>_period/2;
--                  <clock> <= '1';
          --        wait for <clock>_period/2;
  -- end process;
```

```
  -- Stimulus process
  stim_proc: process
  begin
    -- hold reset state for 100 ns.
    wait for 100 ns;

   --  wait for <clock>_period*10;

    -- insert stimulus here

    wait;
  end process;

END;
```

Simulation -


ISim (O.40d) - [Default.wcfg]
File Edit View Simulation Window Layout Help
Re-launch
Name
Value
dividend[31:0]
divisor[15:0]
quotient[31:0]
42.530 ns
0 ns
200 ns
400 ns
600 ns
800 ns
X1: 42.530 ns
Default.wcfg
Console
WARNING: A WEBPACK license was found.
WARNING: Please use Xilinx License Configuration Manager to check out a full ISim license.
WARNING: ISim will run in Lite mode. Please refer to the ISim documentation for more information on the differences between the Lite and the Full version.
This is a Lite version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,000,000 ps
11:24
18-03-2019

RTL Schematic –