

STM32H743VIT6

												>					ı
						GNE	D99									5٧	l
	DCMI D3				PE1	E	98	→		DCMI D2				PE0	E	97	Γ
	I2C1 SDA			CAN1_TX	PB9	В	96	→		I2C1 SCL			CAN1_RX	PB8	В	95	ſ
	DCMI VSYNC			CAN2_TXFD_ MODE	PB7	В	93	~		QSPI BK1 NCS			CAN2_TX	PB6	В	92	l
RTM_EEV7	SPI1/3/6 MOSI	12C1/4 SMBA	TM17_BKIN/ TM3_CH2	CAN2_RX	PB5	В	91	→	HRTM_EEV6	SPI1/3 MISO/ SPI2 SS	TM16_BKIN/ TM3_CH1	TX7	NJTRST	PB4	В	90	l
RX7	SPI1 SCLK	SPI3/6 SCLK	TM2_CH2/ HRTM_FLT4	SDM2 D2	PB3	В	89	→		SPI1 MOSI				PD7	D	88	I
	SPI1 SS				PD6	D	87	→						PD5	D	86	ı
					PD4	D	85	→		DCMI D5				PD3	D	84	I
	QSPI CLK	SDM1 CMD			PD2	D	83	→						PD1	D	82	I
					PD0	D	81	→			SDM1 CK			PC12	С	80	I
		SDM1 D3			PC11	С	79	→			SDM1 D2			PC10	С	78	I
RTM_FLT1	SPI3/6 SS	TX7	TM2_CH1/ TM2_ETR		PA15	Α	77	\rightarrow	TM1_ETR/ HRTM_CHD2	SPI2 SCLK	USB1 DP	TX4	CAN1_TX	PA12	Α	71	١
CAN1_RX	SPI2 SS	USB1 DM	RX4	TM1_CH4 HRTM CHD1	PA11	Α	70	\rightarrow		CAN1_ TXED_MODE	RX1	TM1_CH3/ HRTM_CHC2		PA10	Α	69	ı
AN1_RXFD MODE	SPI2 SCLK	TX1	I2C3 SMBA	TM1_CH2/ HRTM_CHC1	PA9	Α	68	→	TM8_BKIN2	TM1_CH1/ HRTM CHR2	RX7	I2C3 SCL	RCC MCO1	PA8	Α	67	I
		SDM1 D1			PC9	С	66	→			SDM1 D0			PC8	С	65	l
	DCMI D1				PC7	С	64	→		DCMI D0				PC6	С	63	l
					PD15	D	62	→						PD14	D	61	I
	QSPI BK1 IO3				PD13	D	60	→		QSPI BK1 IO1				PD12	D	59	l
	QSPI BK1 IO0				PD11	D	58	→						PD10	D	57	l
					PD9	D	56	→						PD8	D	55	l
					PB15	В	54	\rightarrow						PB14	В	53	١
				CAN2_TX	PB13	В	52	→					CAN2_RX	PB12	В	51	I

		* *																		
Swork Swork																	•			
			• 🖬 6		GND								3V3							
			MERA E2 E3 6	←	1 E	PE2				QSPI BK1 IO2		+	2	PE3	LED BLUE					
		B9 B8 G EV	IN SEA DOMES ES O G	←	3 E	PE4				DCMI D4		-	4 E	PE5				DCMI D6		
		B7 B6 1 1 7	E6 VB	÷	5 E	PE6				DCMI D7			VBAT(6	bat ch	arge suppon					
		B5 B4	ਲ ≡ ■GI NR ● €	←	7 C	PC13	KEY1					←	14	NR	NRST					
		B3 D7	C0 C1 0	*	15 C	PC0						*	16	PC1						
		D6 D5	G 3V3 C2 C3 0	+	17 C	PC2						+	18	PC3						
		D4 D3	■ GND V+ 60 6	•	GND19	9							20		VREF+					
		D2 D1 500	A0 A1 0 6	*	22 A	PA0		TM2_CH1/TM2 ETR/	TX4	SAI2 SD-B	TM8_ETR/ TM15_BKIN	*	23 A	PA1		TM2_CH2/ TM5_CH2	RX4	SAI2 MCLK-B	TM15_CH1N	
			A2 A3 0 0	₩.	24 A	PA2		TM2_CH3/ TM5_CH3	TX2	SAI2 SCK-B	TM15_CH1	**	25 A	PA3		TM2_CH4/ TM5_CH4	RX2		TM15_CH2	
		C11C10	- I A4 A5 0 6	←	28 A	PA4		SPII SS	SPI3/6 SS	DCMI HSYNC	TM5 ETR	+	29 A	PA5		TM2_CH1/	SPI1/6 SCLK		TM8 CH1N	
		A15A12	_ I A6 A7 @ @	*	30 A	PA6	TM13_CH1	SPI1/6 MISO	TM1_BKIN/ TM3_CH1	DCMI PIXCLK	TM8_BKIN	+	_	PA7		TM2 ETR SPI1/6 MOSI	TM1_CH1N/ TM3_CH2	TM14_CH1	TM8_CH1N	
		A11A10 == 0	T C4 C5	←	32 C	PC4			IM3 CH1			←	33 C	PC5			IM3 CH2			
		A9 A8	B0 B1 6	~	34 🖪	PB0		TM1_CH2N/			TM8 CH2N	←	35 🔠	PB1		TM1_CH3N/			TM8 CH3N	
		C9 C8 SB1: DVP_PWDN	⇒ A7 B2 E7 🔘 😭	~	36 🕒	PB2	RTC OUT	SPI3 MOSI		SAI1/4 SD-A	SAI1/4 D1	+	37 🗐	PE7		TM3 CH4				
		C7 C6 SB3: SPI_Flash_0	29-> D6 F8 F9 🚳 🚳	←	38	PE8						+	39 E	PE9						
		D15D14 SB5: DVP_AF2V8	D → GND E10 E11 📵 📵		40 E	PE10		LCD LED				*	41 E	PE11		LCD CS				
		D13D12 R9 : VREF+ -> 3\	13 E12E13 @ @	←	42 E	PE12		LCD SCL				-	43	PE13		LCD WR RS				
		D11D10	E14E15 @ @	÷	44 E	PE14		LCD SDA				+	45	PE15						
_	00	D9 D8	B10 B11 @ @	÷	46 🖪	PB10						÷	47 B	PB11						
		B15 B14	3V3 5V 0 0		3V3								5V							
	00	B13 B12	CND CND		OND 46			+		+			ONID 40		-					

LEGEND CPU pin Pin name A Port A Port B Port C D Port D E Port E ← DIG IO pin (5V tol) DIG IO Hi-speed Low-voltage pin (5V tol) √ PWM pin (DIG + ANA) - IO pin with USB power option GROUND(PIN NO) DEBUG USB SDIO (microSD) SPI/I2C DCMI (camera) QSPI LCD TIMER AND CHANNEL CAN

