AG35 Reference Design

LTE Module Series

Rev. AG35_Reference_Design_Rev.A

Date: 2017-12-27

Status: Released

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About the Document

History

Revision	Date	Author	Description
A	2017-12-27	Eden LIU	Initial

Contents

1 Reference Design

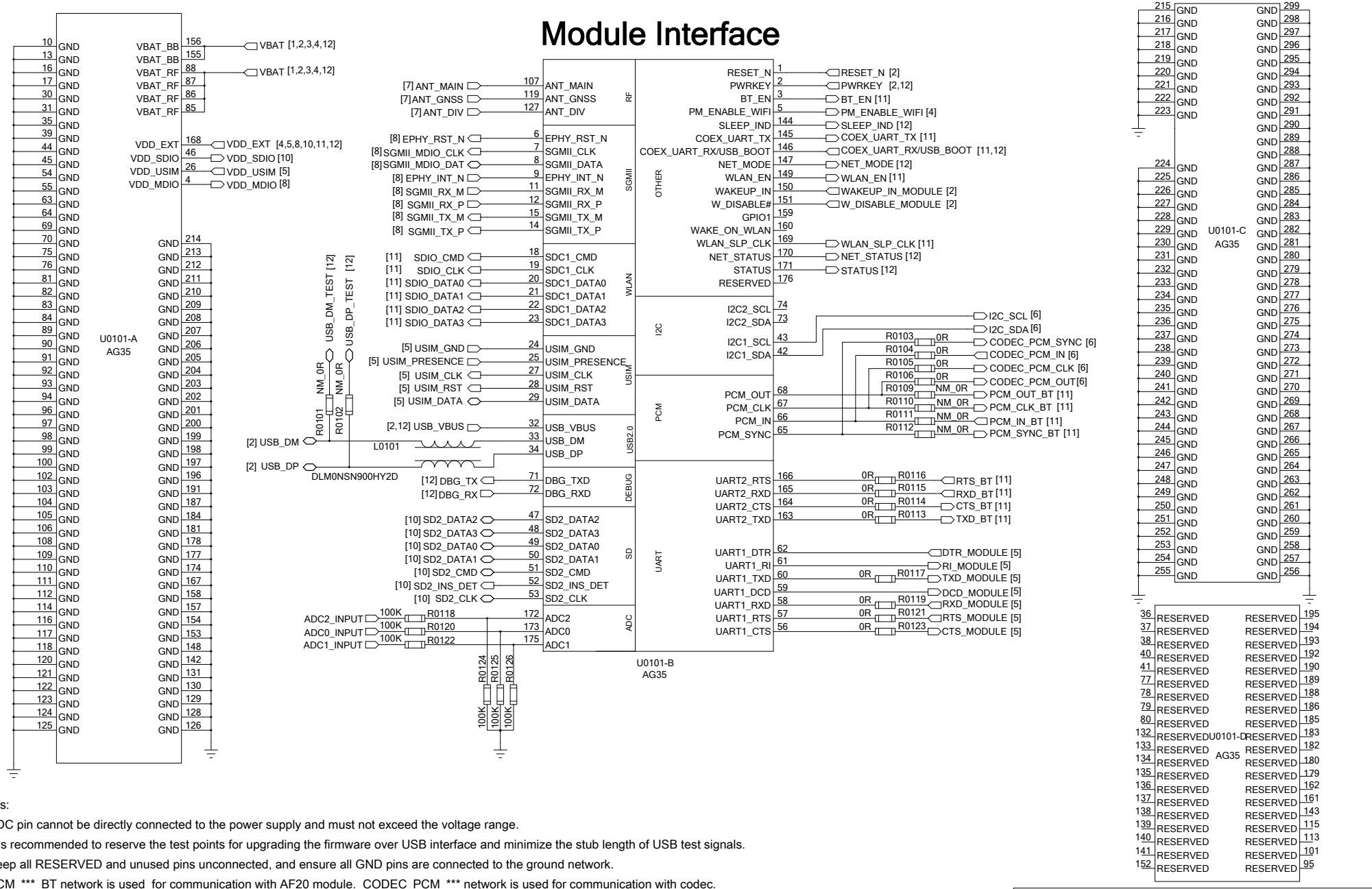
1.1. Introduction

This document provides the reference design for Quectel AG35 module.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Module Interface



Notes:

1. ADC pin cannot be directly connected to the power supply and must not exceed the voltage range.
2. It is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the stub length of USB test signals.
3. Keep all RESERVED and unused pins unconnected, and ensure all GND pins are connected to the ground network.
4. PCM_***_BT network is used for communication with AF20 module. CODEC_PCM_*** network is used for communication with codec.
   AF20 and codec cannot be connected to the same PCM interface at the same time.
5. COEX_TX, COEX_RX, NET_MODE and WLAN_EN must be at low level before the module starts up successfully.

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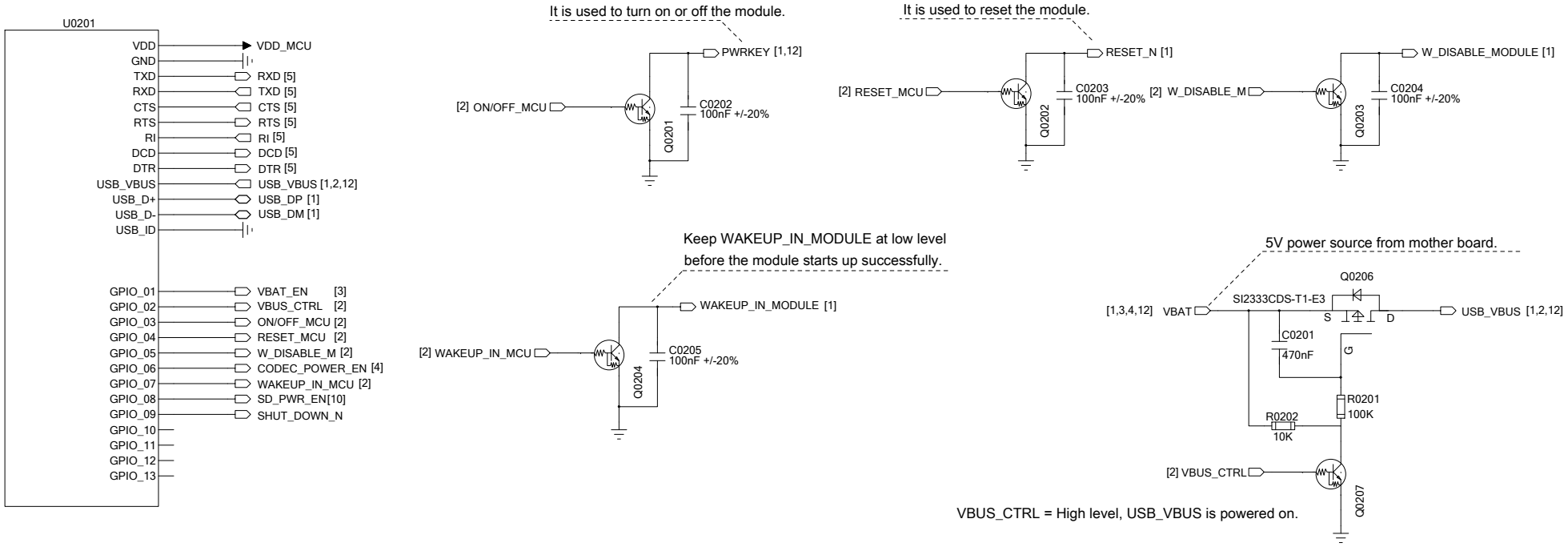
MCU Interface



Notes:

1. U0201 represents customer's MCU.
2. AG35 can only work as a USB device and supports Full Speed and High Speed modes. To communicate with USB interface, MCU needs to support USB host or OTG function. The VBUS pins of MCU and AG35 should be powered by a 5V power system for USB detection, and VBUS_CTRL is used to turn on/off VBUS power supply. When VBUS_CTRL is at high level, USB_VBUS will be powered on.
3. Transistor circuits (Q0201~Q0204) are used for level translation.

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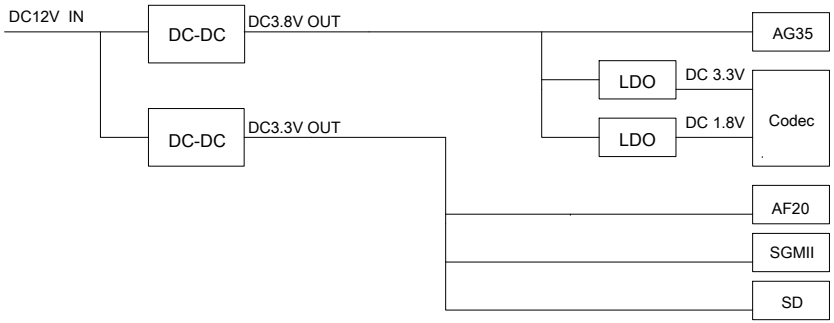
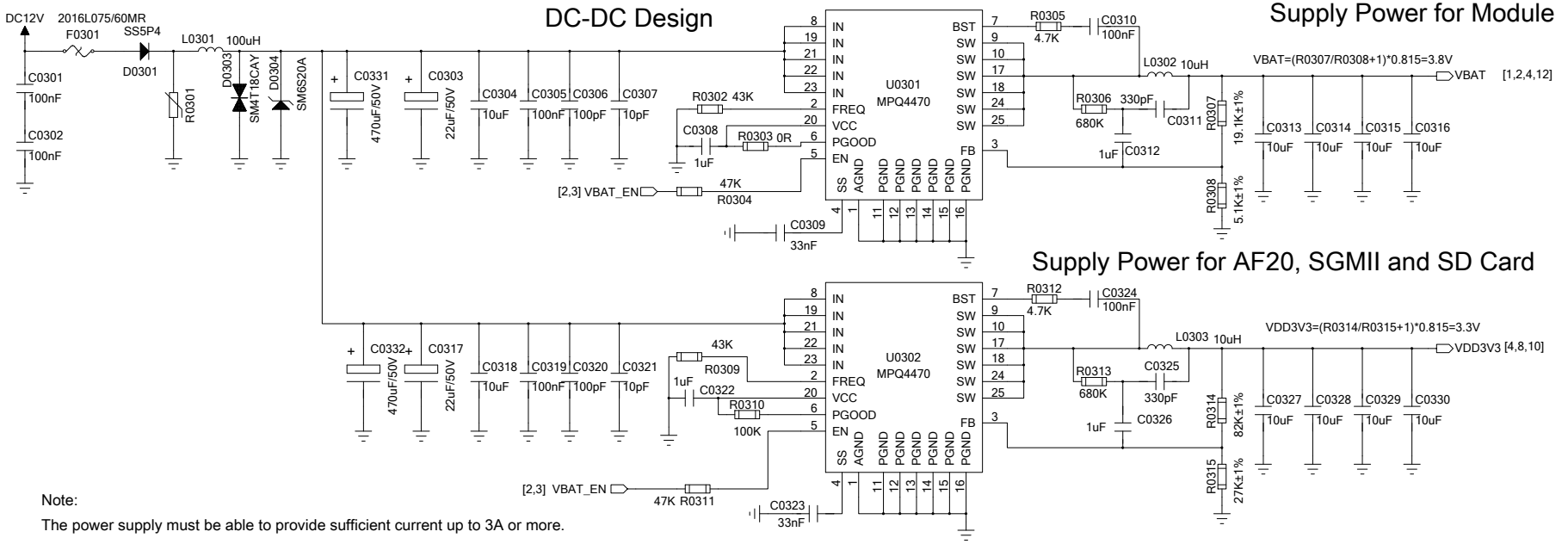
Power Supply Design

DC-DC Application Block

A DC-DC converter is used to convert a high input voltage into 3.8V and 3.3V outputs, and then the LDOs will generate 3.3V and 1.8V typical voltages.



DC-DC Design



Supply Power for Module

Supply Power for AF20, SGMII and SD Card

Note:

The power supply must be able to provide sufficient current up to 3A or more.

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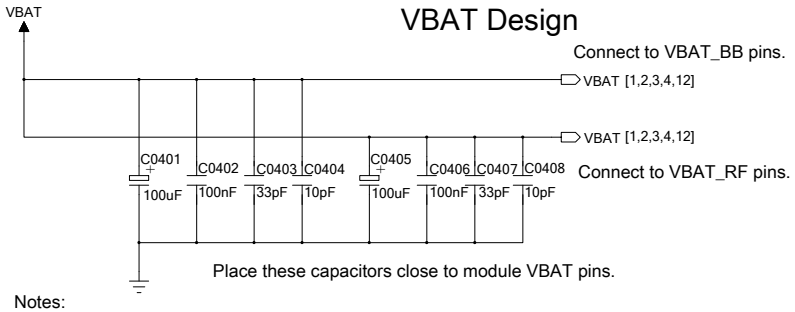
Power Supply Design

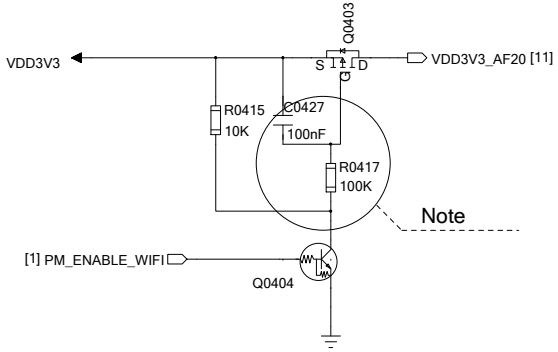
VBAT Design



Notes:

1. The power supply must be able to provide sufficient current up to 2A or more.
2. VBAT should be routed in star mode to VBAT_BB and VBAT_RF pins.
3. The recommended operating voltage of VBAT is 3.3V~4.3V.

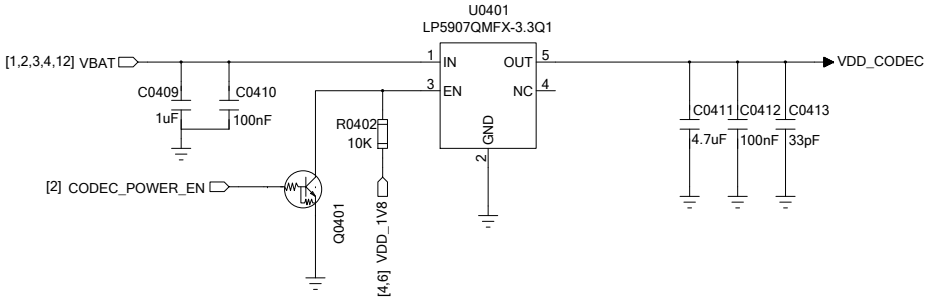
Supply Power for AF20

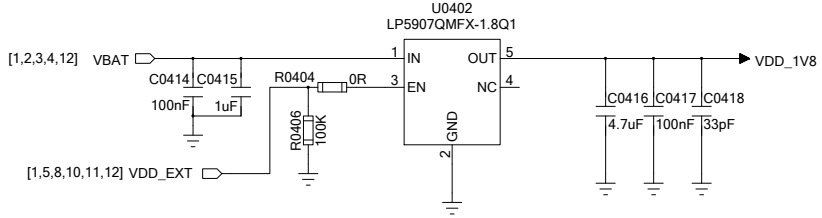


Note:

The RC circuit, which is assembled with R0417 and C0427, is used to delay the start-up of MOSFET switch circuit.

Supply Power for PCM Codec





Notes:

1. CODEC_POWER_EN must be at low level in order to ensure normal output voltage of VDD_CODEC.
   If VDD_CODEC power supply needs to be switched off, please keep CODEC_POWER_EN at high level.
2. To ensure that the audio codec works normally, please follow the power-on and power-off sequences of its power supply.
   Power-on Sequence: power on VDD_1V8 first, and then VDD_3.3V.
   Power-off Sequence: power off VDD_3.3V first, and then VDD_1V8.

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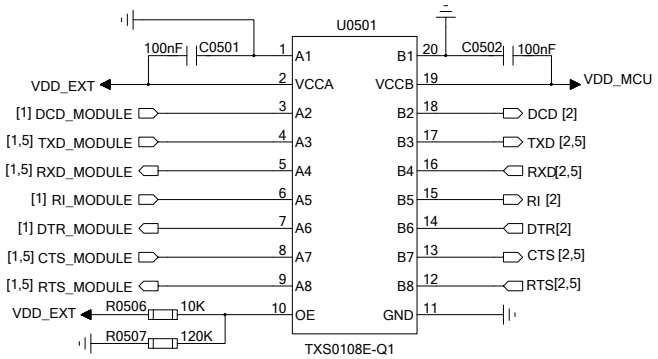
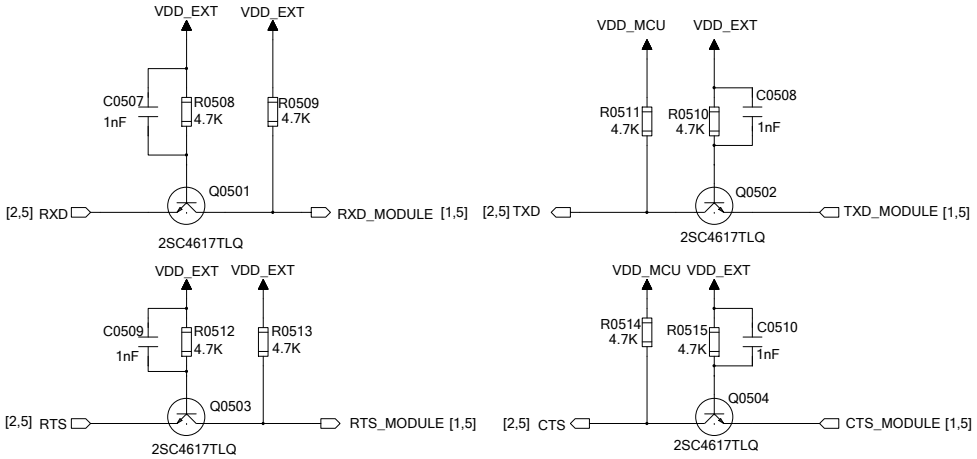
(U)SIM and UART Design

UART Level Translation - IC Solution (Recommended)



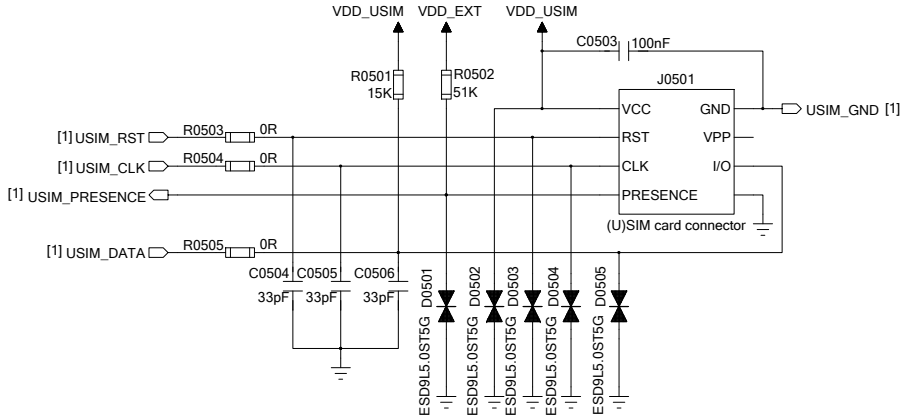
UART Level Translation - Transistor Solution



Notes:

1. It is recommended to use an IC conversion chip for UART level translation.
   The transistor circuit solution is not suitable for applications with high baud rates exceeding 460Kbps.
2. The supply voltage range of VCCA should not exceed that of VCCB. For more information about TXS0108E-Q1, please refer to the datasheet from TI.
3. If high baud rate is needed, it is highly recommended to install four 1nF capacitors (C0507/C0508/C0509/C0510) on transistor circiuts.
4. The DTR transistor circuit is similar to that of RTS interface. The RI and DCD transistor circuits are similar to that of CTS interface.

(U)SIM Interface



Notes:

1. The decouple capacitor of VDD_USIM should be less than 1uF and must be near to (U)SIM card connector.
2. AG35 module provides an input pin (USIM_PRESENCE) to detect whether the (U)SIM card exists or not. It supports both low level and high level detections. For more details, please refer to *Quectel_AG35_Hardware_Design*.
3. R0503~R0505 are applied to suppress the EMI spurious transmission and enhance the ESD protection.
4. It is recommended to take electrostatic discharge (ESD) protection measures near the (U)SIM card connector. The TVS diode with junction capacitance less than 10 pF must be placed as close as possible to the (U)SIM card connector.
5. R0501 can improve anti-jamming capability of the (U)SIM circuit and it should be placed close to the (U)SIM card connector.

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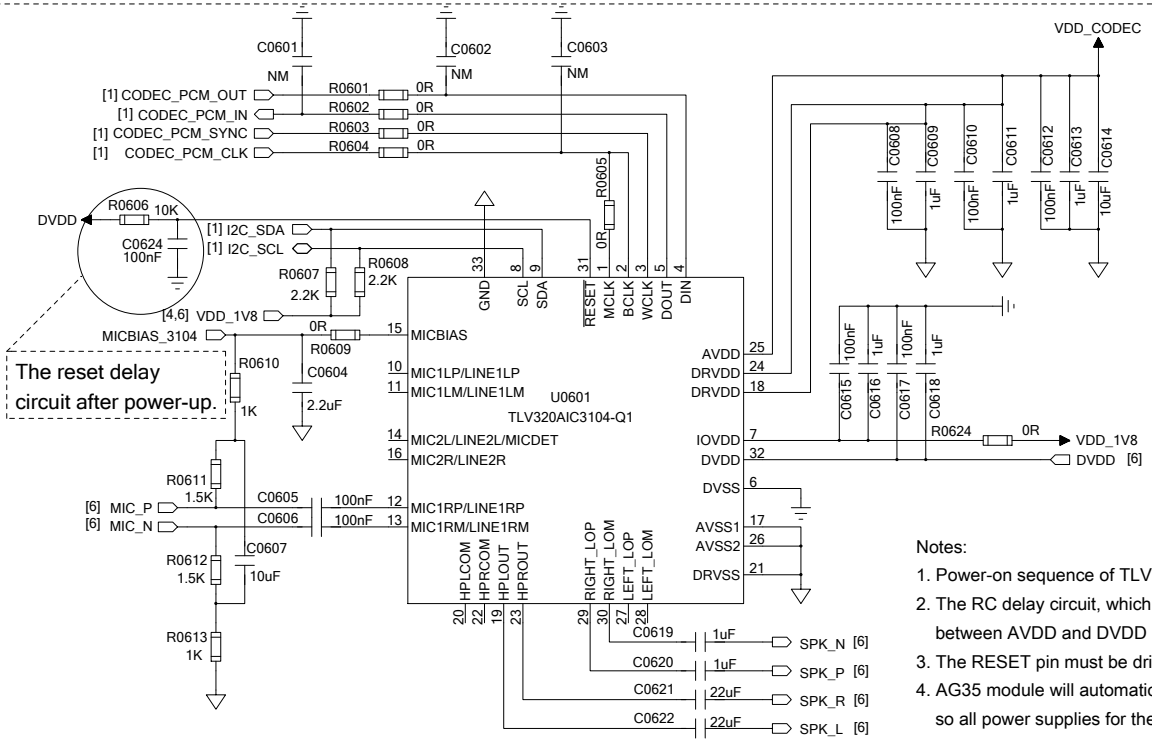
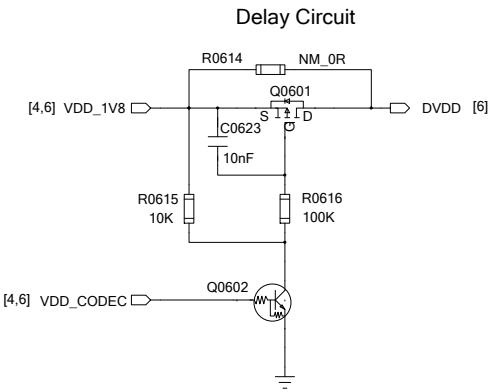
Audio Design

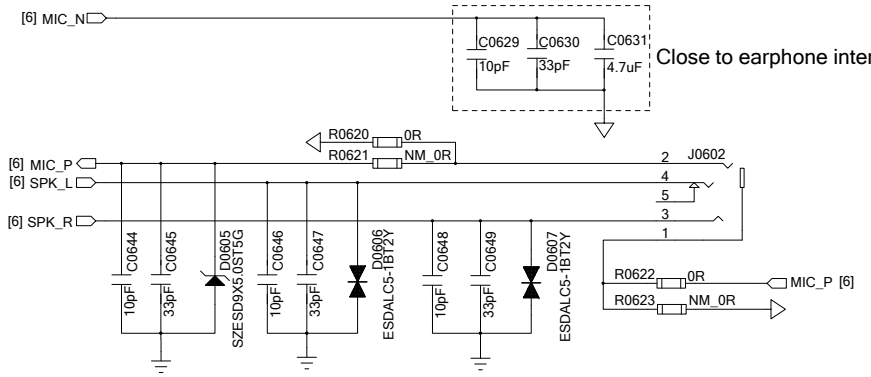


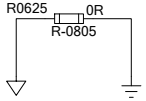


Notes:

1. Power-on sequence of TLV320AIC3104-Q1: IOVDD → AVDD/DRVDD → DVDD → Software Initialization
2. The RC delay circuit, which is assembled with C0623 and R0616, is used to ensure that the power-on time difference between AVDD and DVDD is within 5ms. For more details, please refer to TLV320AIC3104-Q1 datasheet.
3. The RESET pin must be driven at low level for at least 10ns after all power supplies for TLV320AIC3104-Q1 are at their specified values.
4. AG35 module will automatically initialize the codec via I2C interface after it is turned on successfully, so all power supplies for the codec need to be turned on before that.

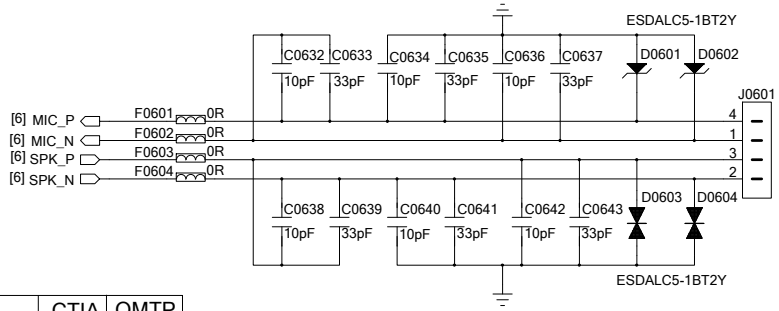
Audio - Earphone Application





	CTIA	OMTP
R0621/R0623	NM	M
R0620/R0622	M	NM

Audio - Handset Application



Notes:

1. The analog output only drives earphone and headset. For larger power loads such as speakers, the design for an audio power amplifier should be added.
2. The maximum capacitive loading for SPK is 330 pF and the maximum capacitive loading for MIC is 250 pF.

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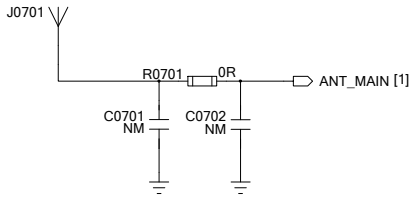
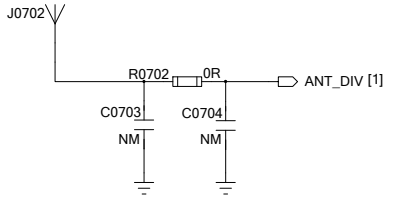
RF and GNSS Design

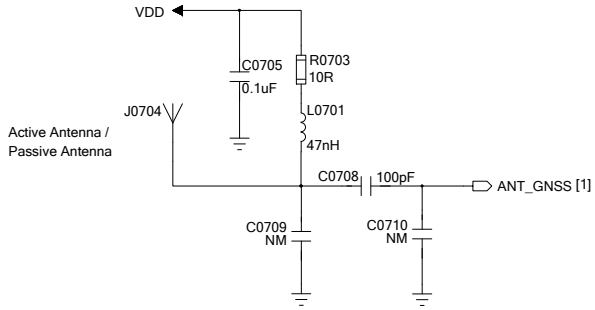
Main Antenna Interface



Rx-diversity Antenna Interface



GNSS Antenna Circuit



Notes:

1. It is recommended to use PI type main/Rx-diversity/AF20 antenna circuit, thus ensuring covenicent subsequent debugging.
2. The diversity reception function is ON by default. If diversity antenna is not used, there is a need to use AT command to turn off diversity reception.
3. An external LDO can be selected to supply power for active antenna.
4. If passive antenna is used, then R0703 and L0701 are not needed.
5. The impedance of the RF signal traces must be controlled as 50Ω when routing.

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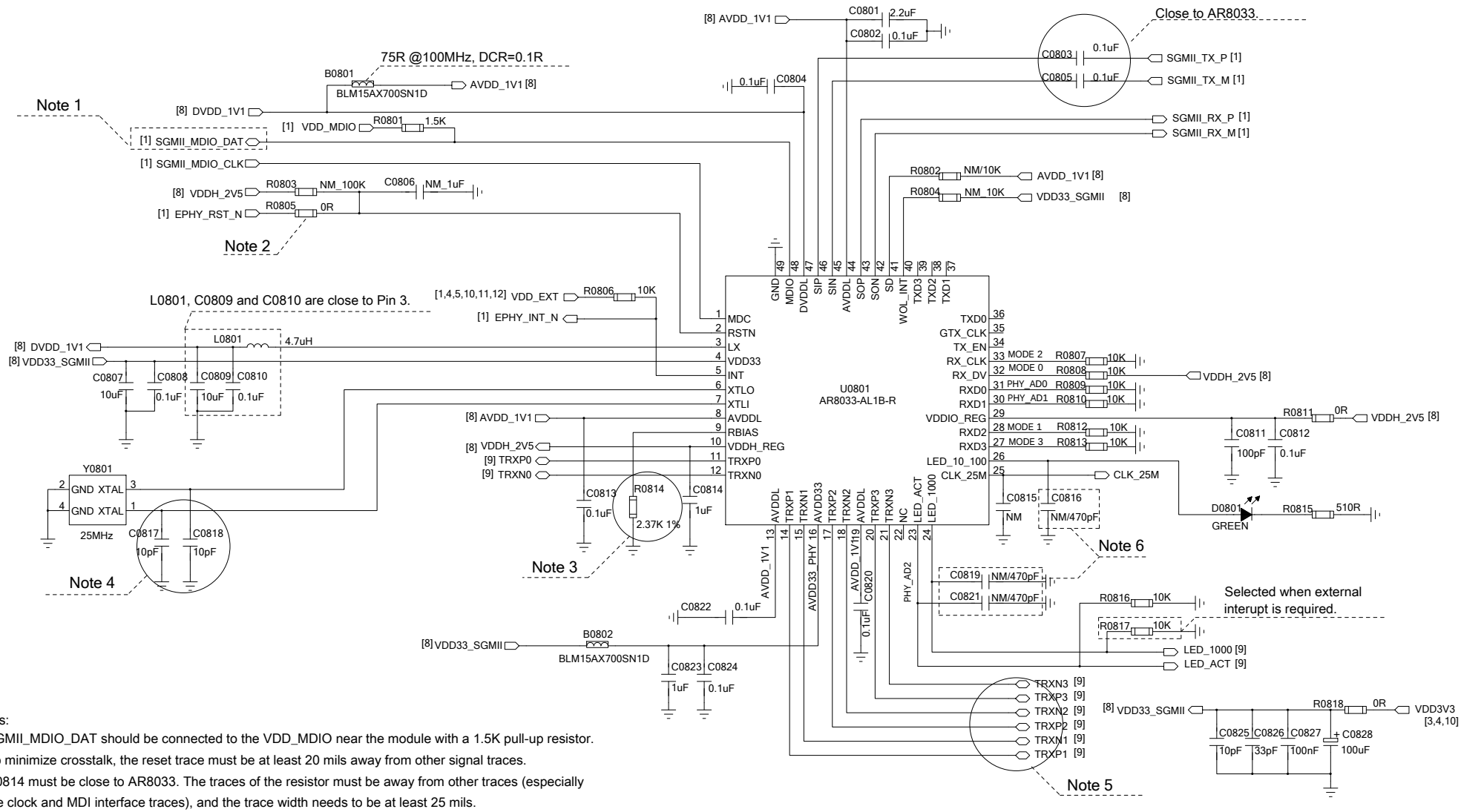
SGMII Design (Part 1)



Notes:

1. SGMII_MDIO_DAT should be connected to the VDD_MDIO near the module with a 1.5K pull-up resistor.
2. To minimize crosstalk, the reset trace must be at least 20 mils away from other signal traces.
3. R0814 must be close to AR8033. The traces of the resistor must be away from other traces (especially the clock and MDI interface traces), and the trace width needs to be at least 25 mils.
4. The capacitors can be changed according to actual crystal selection and board level test results under full application temperature and voltage ranges.
5. The differential impedance of SGMII traces must be limited to 100Ω.
6. EMI filter is reserved. If LED pins are not used, keep C0816/C0819/C0821=470pF.
7. The space between SGMII differential pair (RX and TX traces) should be 3 times of the trace width at least. Also, SGMII should keep a distance of 3 times of its trace width from other signal lines.
8. The peripheral circuit layout of Ethernet PHY chip AR8033 should be designed on a four-layer PCB.

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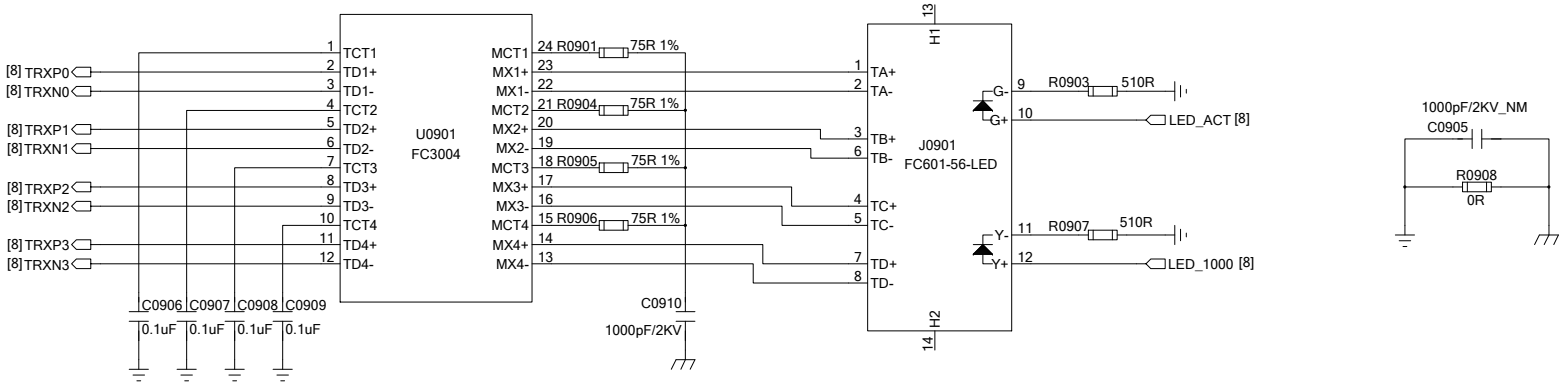
SGMII Design (Part 2)

PHY core configuration signal	Description	Default internal weak pull-up/down	Application external weak pull-up/down
PHY_AD2	PHY_AD[2:0] set the lower three bits of the physical address. The upper two bits of the physical address are set to 00.	1	0
PHY_AD1		0	0
PHY_AD0		0	0
MODE 3	Mode select bit 3	0	0
MODE 2	Mode select bit 2	0	0
MODE 1	Mode select bit 1	0	0
MODE 0	Mode select bit 0	0	1
EXT_INT_SEL	An external 10K pull-down resistor is required.	1	0
0=Pull-down, 1=Pull-up.			



Notes:

1. Differential pair P/N skew must be less than 20 mils, and the maximum trace length must be less than 10 inches.
2. Using the 100Ω±10% differential impedance with 50Ω±10% single-ended impedance for SerDes traces is recommended.
3. To minimize crosstalk, the distance between separate adjacent pairs that are on the same layer must be equal to or larger than 40 mils.
4. Copper filling around transformers is prohibited for better ESD protection performance.
5. For better EMI suppression performance, do not route on top PCB layer.

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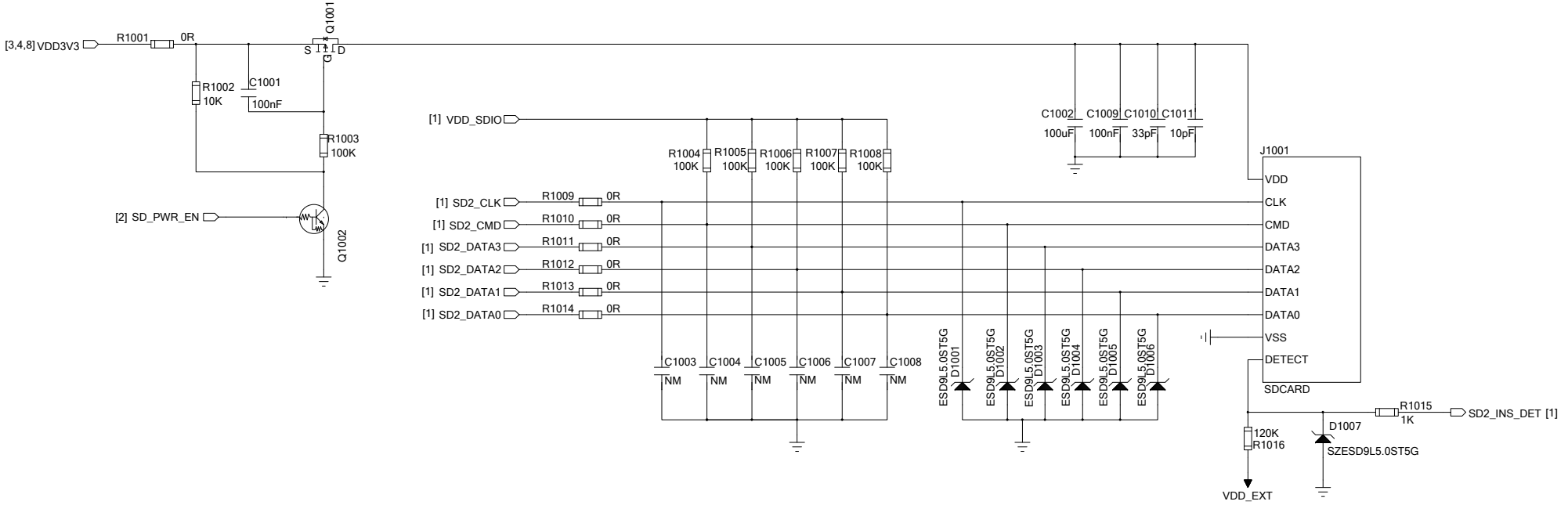
SD Card Interface Design



Notes:

1. VDD_SDIO can only be used for SDIO pull-up resistors and its maximum output current is 50mA.
2. The supply voltage range of VDD for SD card interface is 2.7V~3.6V and sufficient current up to 0.8A needs to be provided.
3. To avoid jitter of bus, resistors R1004~R1008 are needed to pull up the SDIO to VDD_SDIO. The value of these resistors is among 10kohm~100kohm and the recommended value is 100kohm.
4. In order to improve signal quality, it is recommended to add 0 ohm resistors R1009~R1014 in series between the module and the SD card connector.
   The bypass capacitors C1003~C1008 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
5. It is recommended to add ESD protection devices near the pins of SD card connector. The parasitic capacitance of ESD protection devices should be smaller than 2pF.
6. Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noise such as clock and DC-DC signals, etc.
7. Route SD card signal traces with 50Ω impedance, and it is important to route the SDIO signal traces with total grounding.
8. Make sure the adjacent trace spacing is two times of the trace width and the bus capacitance is less than 40pF.
9. It is recommended to keep the trace length difference between CLK and DATA/CMD less than 1mm and the exterior total trace length should be less than 23mm.
10. The pin DETECT of SD card connector must be connected to the module when SD card function is used.

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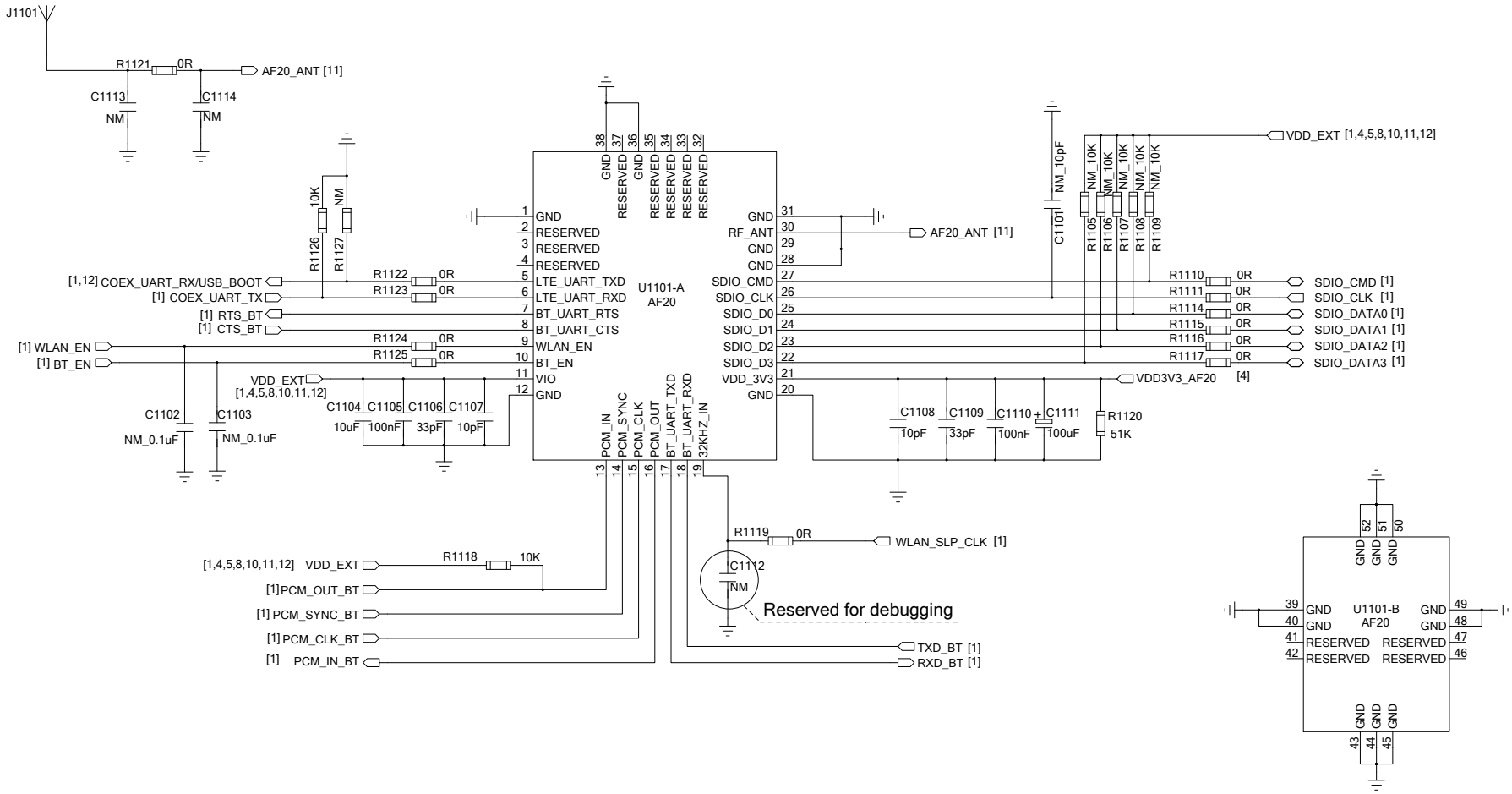
AF20 Design

AF20 Antenna Circuit



Notes:

1. Keep all RESERVED and unused pins unconnected.
2. The impedance of the SDIO data signal traces must be controlled as 50Ω when routing.
3. SDIO data lines should be shielded by ground; SDIO_CMD and SDIO_CLK signal lines should be shielded by ground seperately.
4. It is recommended to use PI type AF20 antenna circuit, thus ensuring covenicent subsequent debugging.
5. The impedance of RF signal trace must be controlled as 50Ω when routing.

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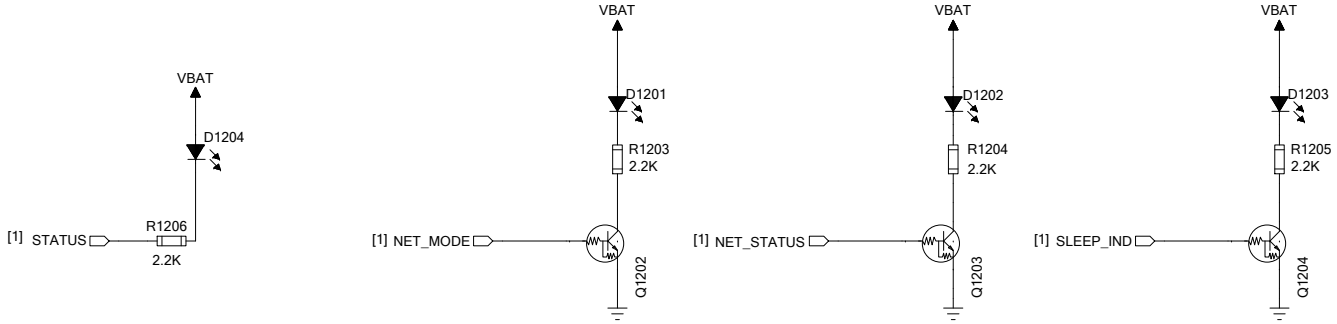
Indicators and Test Points

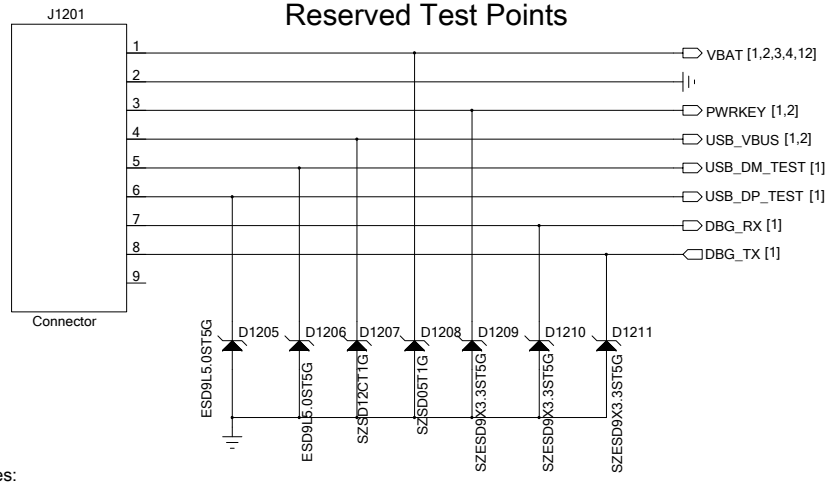
Indicators



Notes:

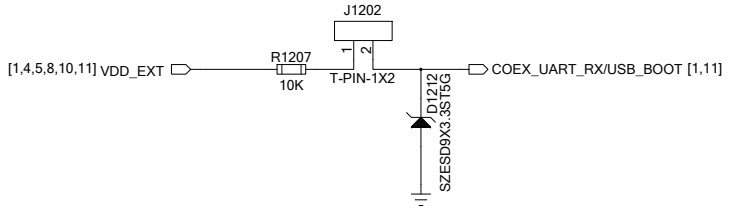
1. The STATUS is an open drain output pin, and its drive current is less than 0.9mA.
2. For more details about NET_MODE and NET_STATUS, please refer to *Quectel_AG35_Hardware_Design*.
3. If the current consumption is required as low as possible when the device is in sleep, replace the power supply of indicators with a controllable one.
   Turn off the power when the module enters into sleep mode.

Reserved Test Points



Notes:

1. Both USB and debug UART interfaces are reserved for software debugging.
2. USB interface also can be used to upgrade firmware.
3. Keep USB test points as close as possible to USB pins.
   Junction capacitance of ESD protection devices on USB data lines might influence the signal, please pay attention to it. Typically, the capacitance should be less than 1pF.
4. DBG interfaces support 1.8V power domain.
   A level translator should be used if the power domain of customers' application is 3.3V.



Note:

COEX_UART_RX/USB_BOOT is kept open by default and the module will be forced into download mode when COEX_UART_RX/USB_BOOT is at high level.

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