OAK RIDGE National Laboratory

IRIS: A Portable Runtime System Exploiting Multiple Heterogeneous Programming Systems

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U.S. DEPARTMENT OF ENERGY

No De Facto Standard for Heterogeneous Programming

- ORNL Experimental Computing Laboratory (ExCL) systems*

Systems	Snapdragon	Jetson	Zynq	DGX	Oswald	Summit	Frontier
CPU	ARM	ARM	ARM	I I I	I I I	IBM	AMD
GPU	Qualcomm	NVIDIA		NVIDIA	NV NV	NVIDIA	AMD AMD
FPGA			Xilinx		Intel Intel		
DSP	Qualcomm						

CUDA Host

CUDA Kernel

HIP Host

HIP Kernel

oneAPI Host

oneAPI Kernel

Hexagon Host

Hexagon Kernel

OpenCL Host

OpenCL Kernel

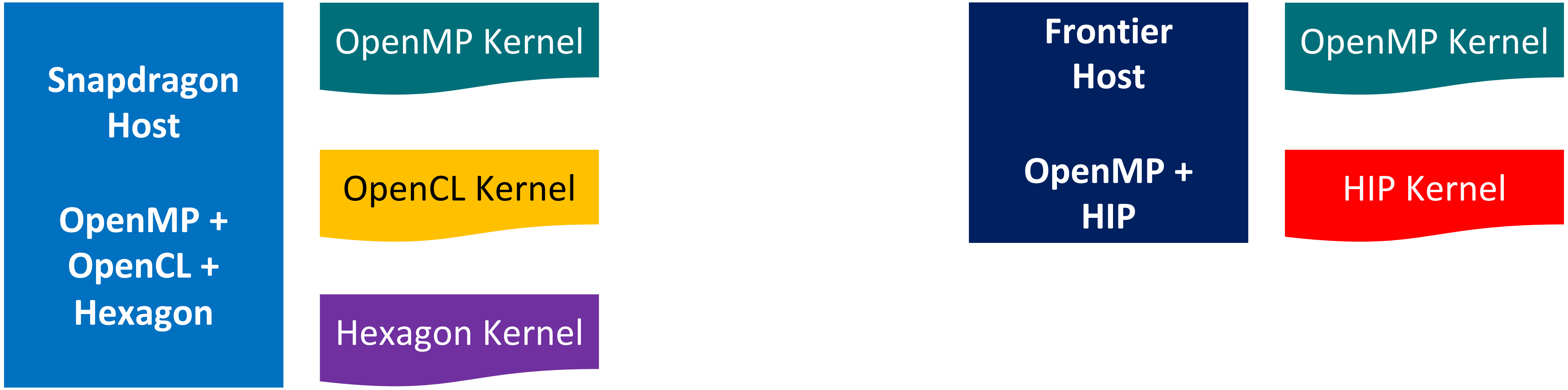
OpenMP

* ORNL ExCL: https://excl.ornl.gov/

We Need Portability in Heterogeneous Programming

- Not portable program across different HW configurations

Systems	Snapdragon	Jetson	Zynq	DGX	Oswald	Summit	Frontier
CPU	ARM	ARM	ARM	I I I	I I I	IBM	AMD
GPU	Qualcomm	NVIDIA		NVIDIA	NV NV	NVIDIA	AMD AMD
FPGA			Xilinx		Intel Intel		
DSP	Qualcomm						



Snapdragon Host

OpenMP + OpenCL + Hexagon

OpenMP Kernel

OpenCL Kernel

Hexagon Kernel

Frontier Host

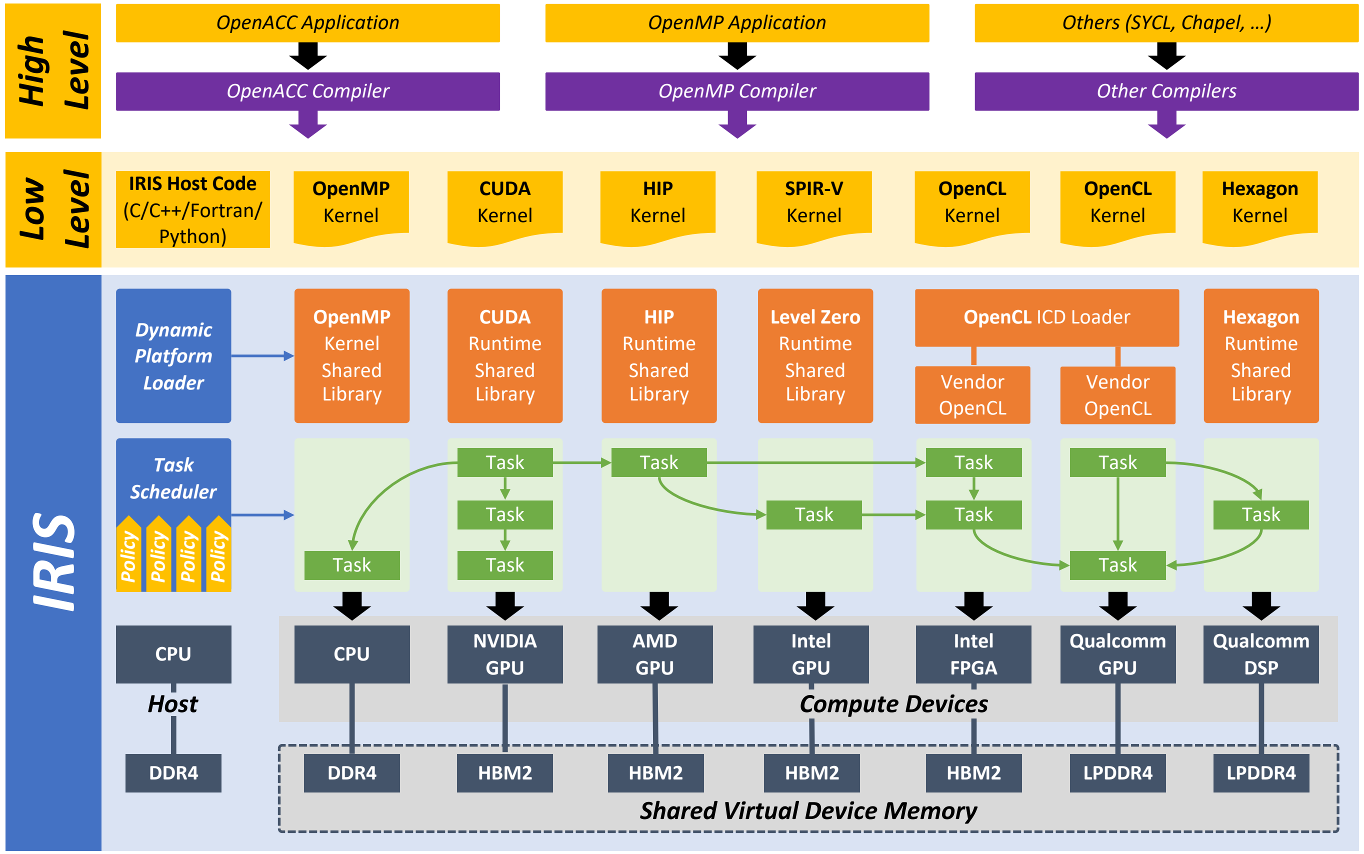
OpenMP + HIP

OpenMP Kernel

HIP Kernel

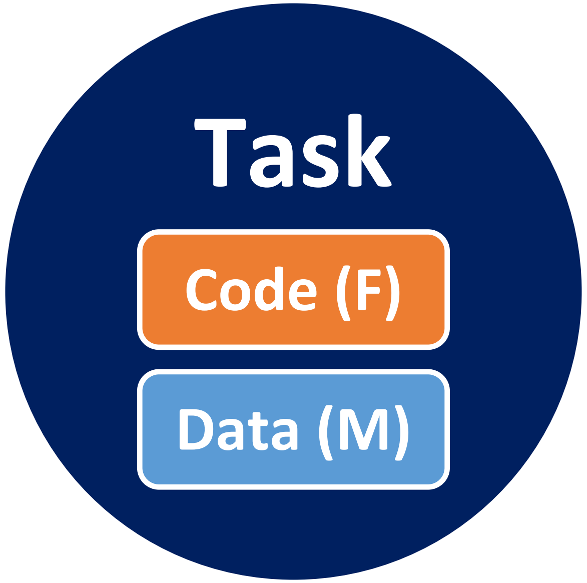
Orchestrating Multiple Programming Systems

- The IRIS Architecture



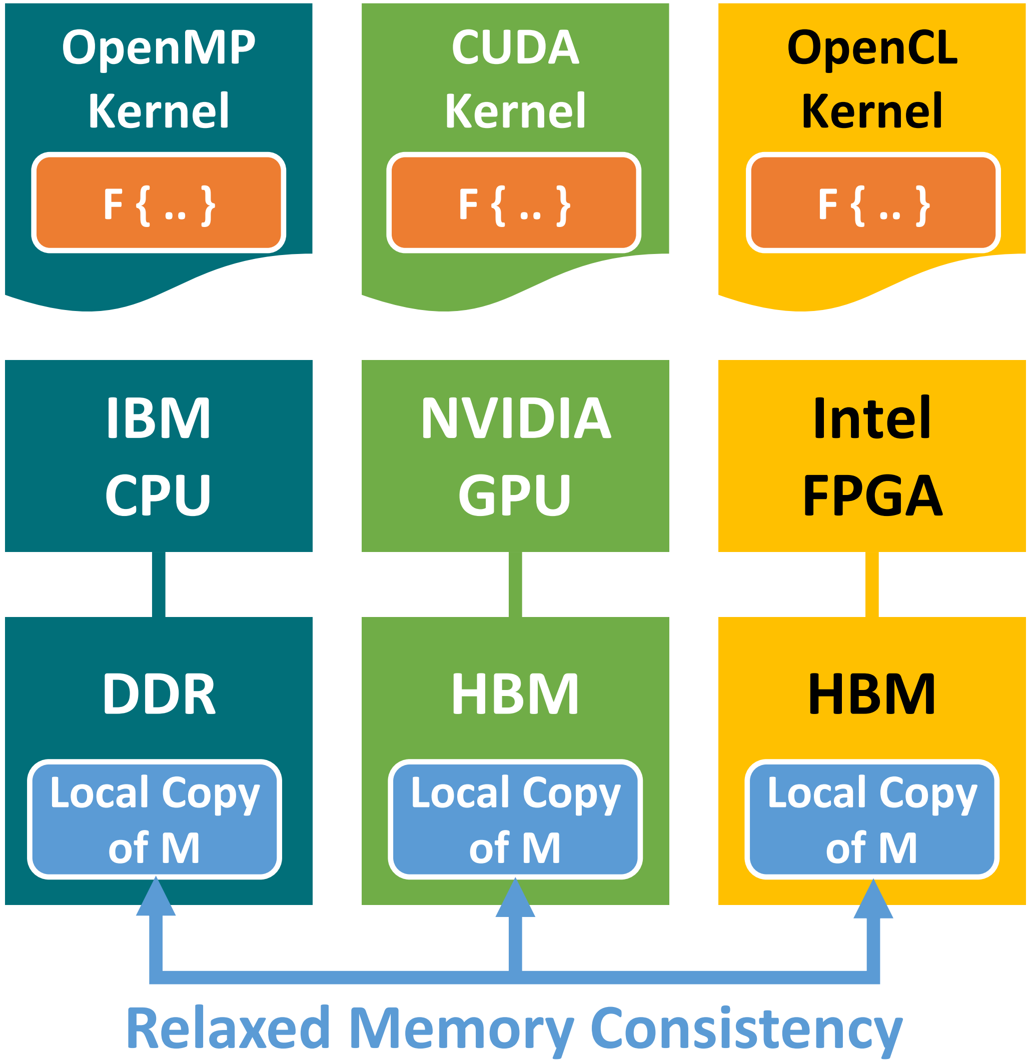
- Compiler
  - High level application → IRIS unified host code + native kernels
- Dynamic Platform Loader
  - Automatically discover all available accelerators and their programming systems
- Task Scheduler
  - Task: memory copy + kernel launch
  - DAG-style tasks graph across multiple devices
  - Device Selection Policies
- Shared Virtual Device Memory
  - An Illusion of single logical device memory across all physical device memories
  - Multiple local copies on multiple device memories (relaxed consistency model)

Multiple Native Kernels + SVDM = ***Portable Tasks & Flexible Scheduling***

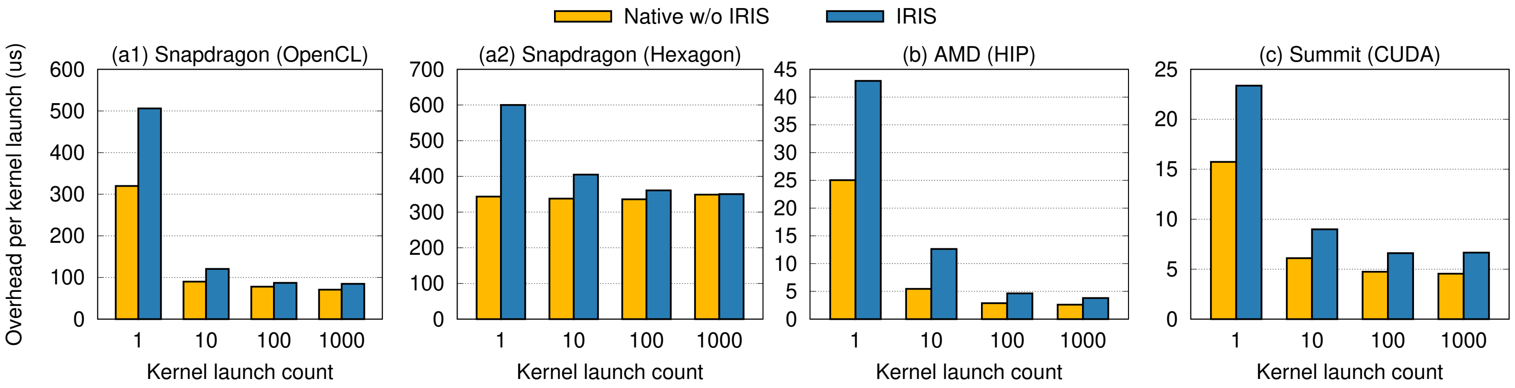


A task can be scheduled and run on any device.

An IRIS application is portable across all heterogeneous systems.

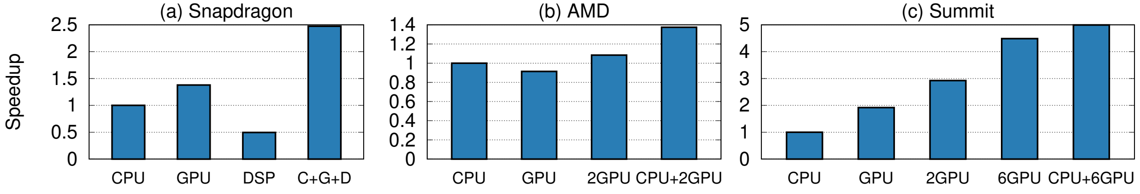


Evaluation: Negligible Runtime Overhead

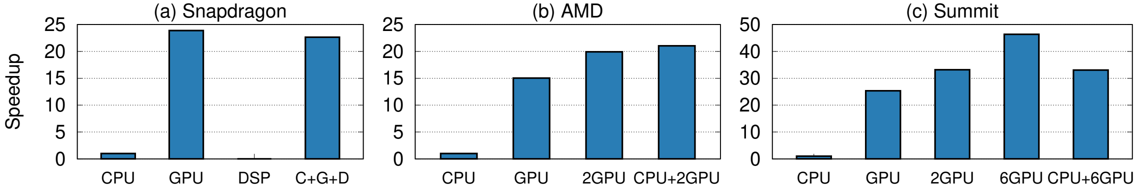


Kernel Launch Overhead

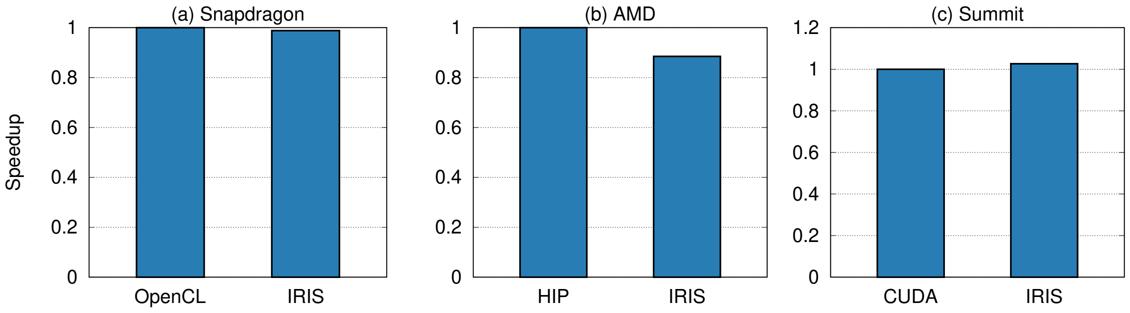
SAXPY



DGEMM



LULESH



Systems	Snapdragon	AMD	Summit
CPU	Qualcomm OpenMP	AMD OpenMP	IBM OpenMP
GPU	Qualcomm OpenCL	AMD HIP	NVIDIA CUDA
DSP	Qualcomm Hexagon		

Recap

Situation No de facto standard for heterogeneous programming

Task Achieving portability in heterogeneous programming

Activity We designed and implemented a new portable runtime system, ***IRIS***

- Orchestrating multiple programming systems (CUDA, Hexagon, HIP, Level Zero, OpenCL, OpenMP)
- Portable Tasks & Flexible Scheduling from Multiple Native Kernels + Shared Virtual Device Memory

Result IRIS achieves portability, programmability, and performance

IRIS is freely available at

https://iris-programming.com

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