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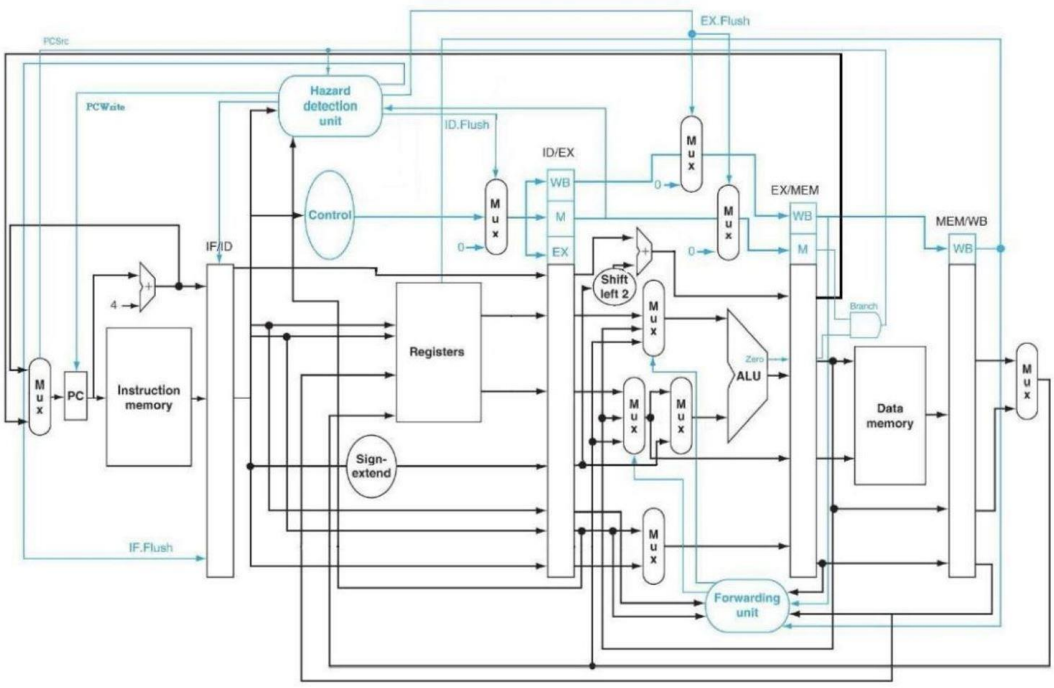
Computer Organization

Architecture



Hardware module analysis

Pipe_Reg 增加了 2 port : flush,write，來 flush 或保留狀態

Mux_ALUsrc 從 2to1 改成 3to1: 00:RD1(RD2)
01:alu_result_mem
10:writeData_wb

Hazard_Detection :

Branch→flush 沒用的 Pip_Reg

Load-use hazard detection

當(ID/EX.MemRead & (IF/ID.rs(rt)==ID/EX.rt)

Prevent update of PC and IF/ID:pcwrite=0,ifid_write=0, idex_flush=1;

Forwarding :

EX_Hazard:

ReWrite_mem & ID/EX.rs(rt) == EX/MEM.rd & EX/MEM.rd !=0→01

MEM_Hazard:

RegWrite_wb && ID/EX.rs(rt)==MEM/WB.rd & MEM/WB.rd !=0 & !EX_Hazard→10

Problems you met and solutions:

去看測資才發現這次有 mult，在 ALU 和 ALU_ctrl 補上即可

另外 hazard_detection 的接線要記得給初始值:

```
pcwrite <= 1, ifid_write <= 1, flush <= 0;
```

Result:

```
Register==========================================================

r0=        0, r1=        3, r2=        4, r3=        1, r4=        6, r5=        2, r6=        7, r7=        1

r8=        1, r9=        0, r10=       3, r11=       0, r12=       0, r13=       0, r14=       0, r15=       0

r16=       0, r17=       0, r18=       0, r19=       0, r20=       0, r21=       0, r22=       0, r23=       0

r24=       0, r25=       0, r26=       0, r27=       0, r28=       0, r29=       0, r30=       0, r31=       0


Memory============================================================

m0=        0, m1=        3, m2=        0, m3=        0, m4=        0, m5=        0, m6=        0, m7=        0

m8=        0, m9=        0, m10=       0, m11=       0, m12=       0, m13=       0, m14=       0, m15=       0

r16=       0, m17=       0, m18=       0, m19=       0, m20=       0, m21=       0, m22=       0, m23=       0

m24=       0, m25=       0, m26=       0, m27=       0, m28=       0, m29=       0, m30=       0, m31=       0
```

Summary:

用 lab4 的 code 加入 hazard_detection 和 forwarding_unit 再動一些東西就好，感謝助教佛心不用分 branch_type