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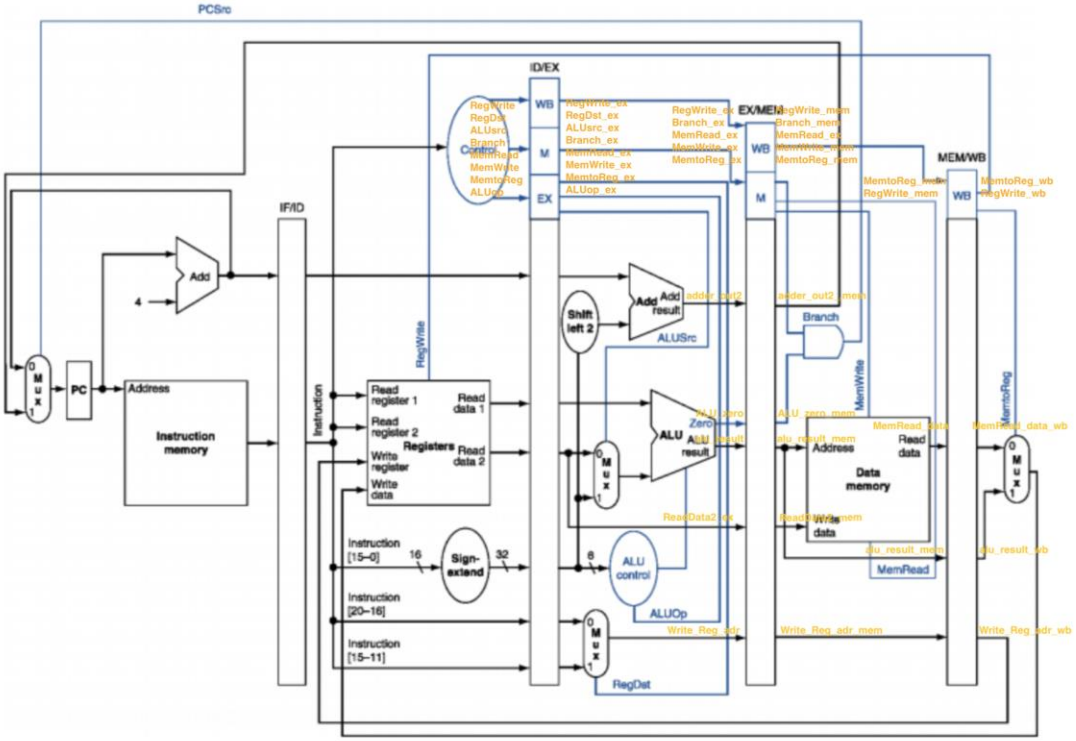
Computer Organization

Architecture



Hardware module analysis

* ALU 增加 ctrl_i=3 的情況 ：src1_i * src2_i
* WriteData 和 RegWrite_wb 都要接回 RF
* Write_Reg_address 也要沿 stages 傳，最後再接回 RF
* 新增四個 Pipe_Reg 暫存各 stage 訊號(見上圖)

(1)IF_ID
(2)ID_EX
(3)EX_MEM
(4)MEM_WB

Problems you met and solutions:

剛弄好想說為什麼輸出都是 0，以為 WB 有東西沒接回 RF，又看到人家說可能是同時 write/read from RF，把 write 改成 always。

最後發現是 testbench 的檔名”testbench/CO_test4.txt”，要把 testbech 拿掉

……:))))

Result:

```
Register=======================================================

r0=     0, r1=     3, r2=     4, r3=     1, r4=     6, r5=     2, r6=     7, r7=     1

r8=     1, r9=     0, r10=    3, r11=    0, r12=    0, r13=    0, r14=    0, r15=    0

r16=    0, r17=    0, r18=    0, r19=    0, r20=    0, r21=    0, r22=    0, r23=    0

r24=    0, r25=    0, r26=    0, r27=    0, r28=    0, r29=    0, r30=    0, r31=    0


Memory=========================================================

m0=     0, m1=     3, m2=     0, m3=     0, m4=     0, m5=     0, m6=     0, m7=     0

m8=     0, m9=     0, m10=    0, m11=    0, m12=    0, m13=    0, m14=    0, m15=    0

r16=    0, m17=    0, m18=    0, m19=    0, m20=    0, m21=    0, m22=    0, m23=    0

m24=    0, m25=    0, m26=    0, m27=    0, m28=    0, m29=    0, m30=    0, m31=    0
```

Bonus:

移動或加 NOP，讓 I1/I2, I5/I6, I8/I9 之間空至少兩行

00100000000000010000000000010000 I1: addi $1,$0,16
00000000000000000000000000000000 NOP
00100000000001100000000000001000 I3: addi $3,$0,8
00100000001000100000000000000100 I2: addi $2,$1,4
10101100000000010000000000000100 I4: sw $1,4($0)
00000000000000000000000000000000 NOP
10001100000001000000000000000100 I5: lw $4,4($0)
00000000011000010011000000100000 I7: add $6,$3,$1
00100000001001110000000000001010 I8: addi $7,$1,10
00000000100000110010100000100010 I6: sub $5,$4,$3
00100000000010010000000001100100 I10: addi $9,$0,100
00000000111000110100000000100100 I9: and $8,$7,$3

```
Register=======================================================

r0=     0, r1=     16, r2=    20, r3=    8, r4=     16, r5=    8, r6=     24, r7=    26

r8=     8, r9=     100, r10=  0, r11=    0, r12=    0, r13=    0, r14=    0, r15=    0

r16=    0, r17=    0, r18=    0, r19=    0, r20=    0, r21=    0, r22=    0, r23=    0

r24=    0, r25=    0, r26=    0, r27=    0, r28=    0, r29=    0, r30=    0, r31=    0


Memory=========================================================

m0=     0, m1=     16, m2=    0, m3=     0, m4=     0, m5=     0, m6=     0, m7=     0

m8=     0, m9=     0, m10=    0, m11=    0, m12=    0, m13=    0, m14=    0, m15=    0

r16=    0, m17=    0, m18=    0, m19=    0, m20=    0, m21=    0, m22=    0, m23=    0

m24=    0, m25=    0, m26=    0, m27=    0, m28=    0, m29=    0, m30=    0, m31=    0
```

Summary:

這次只要把 wb 的東西接回 RF，和把各 stage 的訊號釐清一次就好，還沒有做 forwarding 跟 hazard detection，要是再加上去我看我就不用讀期末考啦
因為 testbench 檔名寫錯 de 了一天真的是哈哈哈，下次記得除了 error 還要回去滑 tcl 看哪裡有問題，痛哭流涕，終於寫完 lab4 可以看下禮拜的期末考了