PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

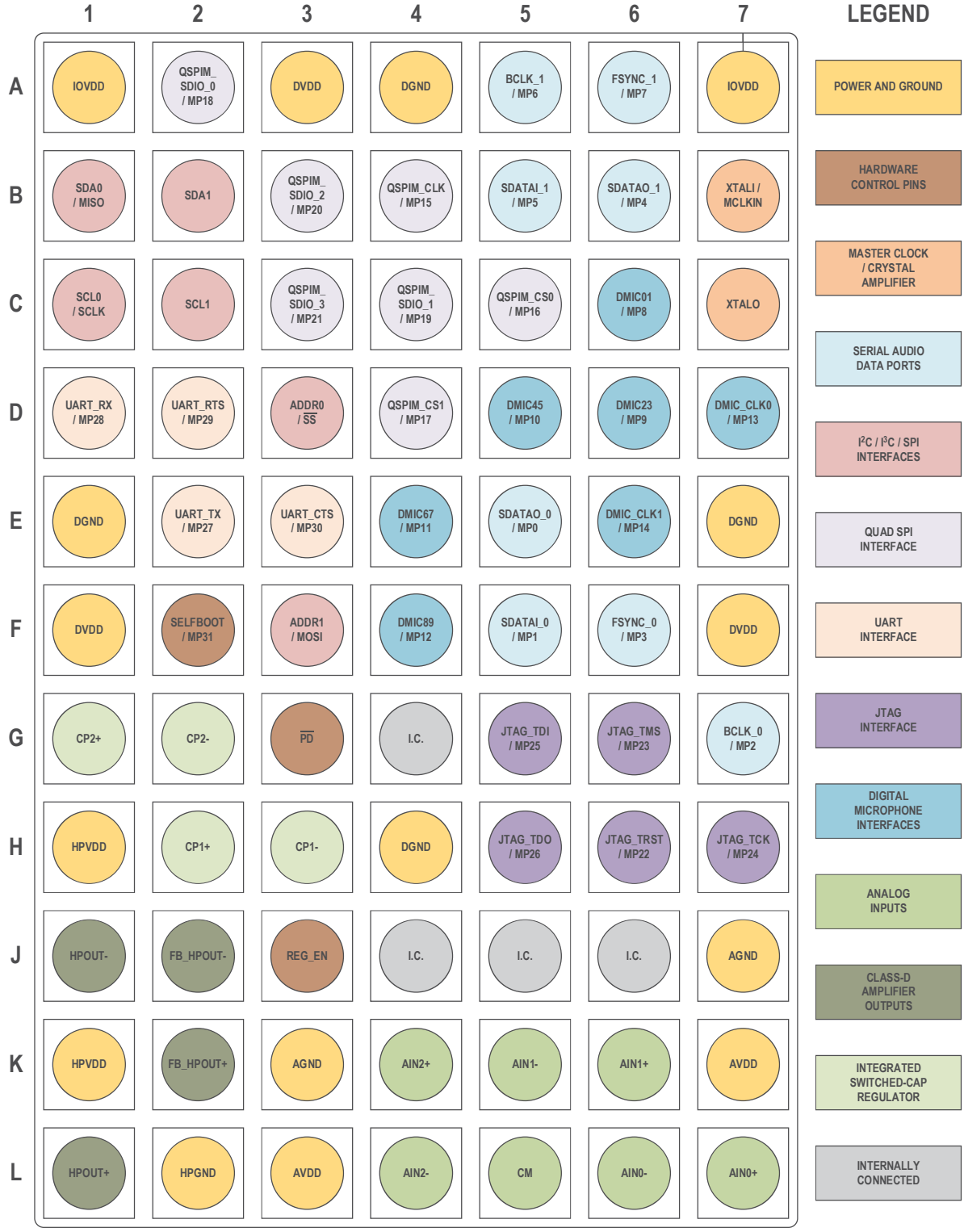

Figure 9. Top View Ball Configuration (View from Top-Side)

Table 8. Pin Function Descriptions

PIN	NAME	DESCRIPTION	Type
A1	IOVDD	Digital Input and Output Pin Supply. The digital output pins are supplied from IOVDD, and this pin sets the highest input voltage seen on the digital input pins. The current draw of this pin is variable because the current is dependent on the loads of the digital outputs. Decouple each IOVDD input to DGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor.	PWR
A2	QSPIM_ SDIO_0 / MP18	Quad Master SPI Data I/O (QSPIM_SDIO_0) or Multipurpose I/O 18	D_IO
A3	DVDD	Digital Core Supply. The digital supply can be generated from an on-chip regulator or supplied directly from an external supply. Decouple each DVDD input to DGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor.	PWR
A4	DGND	Digital Ground. The AGND and DGND pins can be tied directly together in a common ground plane.	PWR
A5	BCLK_1 / MP6	Serial Audio Data Port 1 Bit Clock or Multipurpose I/O 6	D_IO
A6	FSYNC_1 / MP7	Serial Audio Port 1 Frame Sync/Left Right Clock (FSYNC_1) or Multipurpose I/O 7	D_IO
A7	IOVDD	Digital Input and Output Pin Supply. The digital output pins are supplied from IOVDD, and this pin sets the highest input voltage seen on the digital input pins. The current draw of this pin is variable because the current is dependent on the loads of the digital outputs. Decouple each IOVDD input to DGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor.	PWR
B1	SDA0/MISO	I^2C Data 0 I/O (SDA0) or SPI Data Output (MISO). In I^2C mode, this pin is a bidirectional open-drain input. The line connected to this pin must have a 2.0kΩ pullup resistor. In SPI mode, the SPI data output is used for reading back registers and memory locations. This pin is tri-stated when an SPI read is not active.	D_IO
B2	SDA1	I^2C/I^3C Master Data 1 I/O	D_IO
B3	QSPIM_ SDIO_2 / MP20	Quad Master SPI Data I/O 2 (QSPIM_SDIO2) or Multipurpose I/O 20	D_IO
B4	QSPIM_ CLK / MP15	Quad Master SPI Clock (QSPIM_CLK) or Multipurpose I/O 15	D_IO
B5	SDATAI_1 / MP5	Serial Audio Port 1 Input Data (SDATAI_1) or Multipurpose I/O 5	D_IO
B6	SDATAO_1 / MP4	Serial Audio Port 1 Output Data (SDATAO_1) or Multipurpose I/O 4	D_IO
B7	XTALI / MCLKIN	Crystal Clock Input (XTALI)/Master Clock Input (MCLKIN)	D_IN

C1	SCL0 / SCLK	I²C Clock 0 (SCL0) or SPI Clock (SCLK). In I²C mode, this pin is an open-collector input. When the device is in self-boot mode, this pin is an open-collector output (I²C master). In I²C mode, the line connected to this pin must have a 2.0kΩ pullup resistor. In SPI mode, this pin is the SPI Clock. This pin can either run continuously or be gated off between SPI transactions.	D_IN
C2	SCL1	I²C/I³C Master Clock Output	D_O
C3	QSPIM_ SDI0_3 / MP21	Quad Master SPI Data I/O 3 (QSPIM_SDIO3) or Multipurpose I/O 21	D_IO
C4	QSPIM_ SDIO_1 / MP19	Quad Master SPI Data I/O 1 (QSPIM_SDIO1) or Multipurpose I/O 19	D_IO
C5	QSPIM_CS0 / MP16	Quad Master SPI Chip Select 0 (QSPIM_CS0) or Multipurpose I/O 16	D_IO
C6	DMIC01 / MP8	Digital Microphone Stereo Input 0 and 1 (DMIC01) or Multipurpose I/O 8	D_IO
C7	XTALO	Crystal Clock Amp Output. This pin is the output of the crystal amplifier. Do not use this pin to provide a clock to other ICs in the system.	A_OUT
D1	UART_RX / MP28	UART Port Data Receiver Input (UART_RX) or Multipurpose I/O 28	D_IO
D2	UART_RTS / MP29	UART Port Flow Control Ready to Send Output (UART_RTS) or Multipurpose I/O 29	D_IO
D3	ADDR0 / $\overline{SS}$	I²C Address 0 (ADDR0) or SPI Latch Signal ($\overline{SS}$). In I²C mode, ADDR0 and ADDR1 are used to select one of four I²C address options. In SPI mode, this pin must go low at the beginning of a transaction and high at the end of a transaction. Each SPI transaction may take a different number of SCLK cycles to complete, depending on the address and read/write bit that is sent at the beginning of the SPI transaction.	D_IN
D4	QSPIM_CS1 / MP17	Quad Master SPI Chip Select 1 (QSPIM_CS1) or Multipurpose I/O 17	D_IO
D5	DMIC45 / MP10	Digital Microphone Stereo Input 4 and 5 (DMIC45) or Multipurpose I/O 10	D_IO
D6	DMIC23 / MP9	Digital Microphone Stereo Input 2 and 3 (DMIC23) or Multipurpose I/O 9	D_IO
D7	DMIC_CLK0 / MP13	Digital Microphone Clock Output 0 (DMIC_CLK0) or Multipurpose I/O 13	D_IO
E1	DGND	Digital Ground. The AGND and DGND pins can be tied directly together in a common ground plane.	PWR
E2	UART_TX / MP27	UART Port Data Transmit Output (UART_TX) or Multipurpose I/O 27	D_IO

E3	UART_CTS / MP30	UART Port Flow Control Clear to Send Input (UART_CTS) or Multipurpose I/O 30	D_IO
E4	DMIC67 / MP11	Digital Microphone Stereo Input 6 and 7 (DMIC67) or Multipurpose I/O 11	D_IO
E5	SDATAO_0 / MP0	Serial Audio Port 0 Output Data (SDATAO_0) or Multipurpose I/O 0	D_IO
E6	DMIC_CLK1 / MP14	Digital Microphone Clock Output 1 (DMIC_CLK1) or Multipurpose I/O 14	D_IO
E7	DGND	Digital Ground. The AGND and DGND pins can be tied directly together in a common ground plane.	PWR
F1	DVDD	Digital Core Supply. The digital supply can be generated from an on-chip regulator or supplied directly from an external supply. Decouple each DVDD input to DGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor.	PWR
F2	SELFBOOT / MP31	Self-Boot Select or Multipurpose I/O 31. Connect this pin to IOVDD through a 100kΩ resistor at power-up to enable the self-boot mode. This pin also outputs the buffered Crystal Oscillator clock by default at the start-up. Otherwise, set this pin to DGND through a 100kΩ resistor. Once the power-up is completed, this pin can be re-configured as Multipurpose I/O 31.	D_IN
F3	ADDR1 / MOSI	I^2C Address 1 (ADDR1) or SPI Data Input (MOSI). In I^2C mode, ADDR0 and ADDR1 are used to select one of four I^2C address options. In SPI mode, the SPI data input is used for writing registers and memory locations.	D_IN
F4	DMIC89 / MP12	Digital Microphone Stereo Input 8 and 9 (DMIC89) or Multipurpose I/O 12	D_IO
F5	SDATAI_0 / MP1	Serial Audio Port 0 Input Data (SDATAI_0)/Multipurpose I/O 1	D_IO
F6	FSYNC_0 / MP3	Serial Audio Port 0 Frame Sync/Left Right Clock (FSYNC_0) or Multipurpose I/O 3	D_IO
F7	DVDD	Digital Core Supply. The digital supply can be generated from an on-chip regulator or supplied directly from an external supply. Decouple each DVDD input to DGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor.	PWR
G1	CP2+	Switched-Cap Regulator Capacitor 2 Positive Connection. Connect a 1µF capacitor between CP2+ and CP2-.	PWR
G2	CP2-	Switched-Cap Regulator Capacitor 2 Negative Connection. Connect a 1µF capacitor between CP2+ and CP2-.	PWR
G3	$\overline{PD}$	Active Low Power-Down Input. All digital and analog circuits are powered down. The external pulldown resistor to DGND is recommended on this pin to hold the device in power-down mode if the input signal from the system micro-controller is floating while power is applied to the supply pins.	D_IN
G4	I.C.	Internally Connected. Connect to DGND.	DGND

G5	JTAG_TDI / MP25	JTAG Debug Port Data Input (JTAG_TDI) or Multipurpose I/O 25	D_IO
G6	JTAG_TMS / MP23	JTAG Debug Port Master Select (JTAG_TMS) or Multipurpose I/O 23	D_IO
G7	BCLK_0 / MP2	Serial Audio Port 0 Bit Clock (BCLK_0) or Multipurpose I/O 2	D_IO
H1	HPVDD	Headphone Amplifier 1.8V Analog Power Supply. The PCB trace to this pin must be wider to supply the higher current necessary for driving the headphone outputs. Decouple each HPVDD input to HPGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor to provide the peak current necessary for low frequency signals.	PWR
H2	CP1+	Switched-Cap Regulator Capacitor 1 Positive Connection. Connect a 1µF capacitor between CP1+ and CP1-.	PWR
H3	CP1-	Switched-Cap Regulator Capacitor 1 Negative Connection. Connect a 1µF capacitor between CP1+ and CP1-.	PWR
H4	DGND	Digital Ground. The AGND and DGND pins can be tied directly together in a common ground plane.	PWR
H5	JTAG_TDO / MP26	JTAG Debug Port Data Output (JTAG_TDO) or Multipurpose I/O 26	D_IO
H6	JTAG_TRST / MP22	JTAG Debug Port Reset (JTAG_TRST) or Multipurpose I/O 22	D_IO
H7	JTAG_TCK / MP24	JTAG Debug Port Clock (JTAG_TCK) or Multipurpose I/O 24	D_IO
J1	HPOUT-	Headphone Output Inverted	A_OUT
J2	FB_HPOUT-	Headphone Output Inverted Feedback Signal. Connect close to the inverted side of the headphone load after any filtering components.	A_IN
J3	REG_EN	Regulator Enable. Tie this pin to HPVDD to enable the internal DVDD regulator and tie this pin to ground to disable the regulator.	A_IN
J4	I.C.	Internally Connected. Leave this pin unconnected.	DNC
J5		Internally Connected. Connect to DGND.	DGND
J6		Internally Connected. Leave this pin unconnected.	DNC
J7	AGND	Analog Ground. The AGND and DGND pins can be tied directly together in a common ground plane.	PWR
K1	HPVDD	Headphone Amplifier 1.8V Analog Power Supply. The PCB trace to this pin must be wider to supply the higher current necessary for driving the headphone outputs. Decouple each HPVDD input to HPGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor to provide the peak current necessary for low frequency signals.	PWR
K2	FB_HPOUT+	Headphone Output Noninverted Feedback Signal. Connect close to the noninverted side of the headphone load after any filtering components.	A_IN

K3	AGND	Analog Ground. The AGND and DGND pins can be tied directly together in a common ground plane.	PWR
K4	AIN2+	Analog Input ADC2 Non-Inverting Input	A_IN
K5	AIN1-	Analog Input ADC1 Inverting Input	A_IN
K6	AIN1+	Analog Input ADC1 Non-Inverting Input	A_IN
K7	AVDD	1.8V Analog Supply. Decouple each AVDD input to AGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor.	PWR
L1	HPOUT+	Headphone Output Noninverted	A_OUT
L2	HPGND	Headphone Amplifier and Regulator Ground	PWR
L3	AVDD	1.8V Analog Supply. Decouple each AVDD input to AGND with a 0.1µF capacitor, and a single shared 2.2µF bulk capacitor.	PWR
L4	AIN2-	Analog Input ADC2 Inverting Input	A_IN
L5	CM	Common-Mode Reference Output. The CM output is fixed at 0.85V nominal. Connect a 10µF and 0.1µF decoupling capacitor between this pin and AGND to reduce crosstalk between the ADC channels. The material of the capacitors is not critical. This pin can supply a reference bias to external analog circuits as long as they are not drawing current from the CM output (Example: high impedance input of an external amplifier).	A_OUT
L6	AIN0-	Analog Input ADC0 Inverting Input	A_IN
L7	AIN0+	Analog Input ADC0 Non-Inverting Input	A_IN