KADI SARVA VISHWAVIDHYALAYA

BE Semester III

Examination November /December – 2023

Sub Name: Digital Electronics
Sub code: CT 304 N
Date: 18/12/2023

Time: 12:00 pm to 03:00 pm
Total Marks: 70

Instructions:

1. Answer Each Section in a Separate Answer sheet.
2. Use of Scientific Calculator is permitted. .
3. All questions are separate
4. Indicate clearly, the options you attempted along with its respective question number.
5. Use the last page of supplementary for rough work.

SECTION I

Q.1 (a)	Convert $(4F7.A8)_{16}$ to octal,binary & decimal.	**[05]**
(b)	Perform the subtraction with the following decimal numbers using 10's and 9's complement : 5250-321	**[05]**
(c)	Represent the decimal number 8620 in BCD,Excess-3 code,2,-4-2-1 code,Binary number & Gray Code	**[05]**
	OR	
(c)	Simplify the following Boolean functions to a maximum number of literals a) XY+XY' b) (X+Y) (X+Y')	**[05]**
Q.2 (a)	Implement Boolean function with only OR and NOT Gates. F = xy + x'y' + y'z	**[05]**
(b)	Simplify the following Boolean function by using K-MAP method. F = ∑ (0,1,2,8,10,11,14,15)	**[05]**
	OR	
Q.2 (a)	State and explain DeMorgan's law.	**[05]**
(b)	Obtain the simplified expressions in the product of sums. F (A,B,C,D) = ∏ (0, 1, 2, 3, 4, 10, 11)	**[05]**
Q-3 (a)	Explain In Detail with necessary diagram:Implementation of NAND as an universal gate.	**[05]**
(b)	Define & explain Multiplexer in detail.	**[05]**
	OR	
Q-3 (a)	Write a short note on BCD adder with necessary diagram.	**[05]**
(b)	Differentiate between encoder and decoder.	**[05]**

SECTION II

Q.4 (a)	Draw and explain Binary parallel adder with necessary logic diagram.	[05]
(b)	Explain J-K Flip Flop in with truth table & logic diagram.	[05]
(c)	Explain the Excitation table of S-R flip-flop in detail.	[05]
	OR	
(c)	Draw & explain 4- bit shift register.	[05]
Q.5 (a)	Define a synchronous counter and explain the 4-bit synchronous counter in detail.	[05]
(b)	Draw & explain 4-bit BCD counter.	[05]
	OR	
Q.5 (a)	Draw Mealy model for D flip flop.	[05]
(b)	Write a short note on Read only memory (ROM).	[05]
Q-6 (a)	Explain the Programmable Array Logic (PAL).	[05]
(b)	Explain D/A converter R-2R Ladder circuits.	[05]
	OR	
Q-6(a)	Explain Counter type A/D Converter.	[05]
(b)	Explain Flash Type A/D converter.	[05]

Enrollment No. | | | | | | | | | | | |

KADI SARVA VISHWAVIDYALAYA
LDRP INSTITUTE OF TECHNOLOGY & RESEARCH, GANDHINAGAR

B.E. MID-SEMESTER EXAMINATION NOVEMBER 2023

Date : 03/11/2023	Branch : CE/IT
Subject Name & Code: Digital Electronics CT-304 N	Semester : 3
Time : 09.15 AM to 10.45 AM	Max. Marks : 30

Instructions:
1) All questions are **compulsory**.
2) Figures to the **right** indicate **full** marks.
3) Indicate **clearly**, the options you attempt along with its respective question number.
4) Use of scientific Calculator is permitted.
5) Use the last page of main supplementary for **rough work**.

			Marks
Q.1	(A)	Convert the decimal number **250.5** to following number systems: (1) base 2 (2) base 3 (3) base 4 (4) base 8 (5) base 16.	[5]
	(B)	Perform the subtraction of the binary number **11010-1101** using 2's complement.	[5]
Q.2	(A)	Explain basic digital logic gates with their symbol and truth table.	[5]
	(B)	Express the following function in a sum of minterms and a product of maxterms: **F (A, B, C, D) = D(A'+B) + B'D**	[5]
		OR	
Q.2	(A)	Write a short note on half adder.	[5]
	(B)	Explain 4-to-1 line multiplexer with logic diagram.	[5]
Q.3	(A)	Explain Clocked RS flip flop with logic diagram.	[5]
	(B)	Explain 4- bit register in detail.	[5]
		OR	
Q.3	(A)	Explain 4-bit binary ripple counter in detail.	[5]
	(B)	Draw and explain Mealy model for D flip flop.	[5]

~~All the Best~~

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KADI SARVA VISHWAVIDYALAYA

B.E. Semester III EXAMINATION (Nov/Dec-2022)

Subject Code: CT304-N **Subject Name: Digital Electronics**
Date: 16/12/2022 **Time:10:00am to 1:00pm** **Total Marks: 70 Marks**

Instructions:
1. **All questions are compulsory.**
2. **Figures to the right indicate full marks.**
3. **Use of scientific calculator is permitted.**
4. **Indicate clearly, the options you attempt along with its respective question number.**
5. **Use the last page of main supplementary for rough work.**

Section-I

Q:1 Attempt Following.

(A) Explain excess-3 code in detail. [5]
(B) Explain D'Morgan's theorems in detail. [5]
(C) Convert the binary 1001 to gray code. [5]

OR

Q:1 (C) Convert hexadecimal 2AC5.D to decimal and octal. [5]

Q:2 Answer the following question.

(A) Implement following Boolean function using only AND and NOT gates. [5]
$F=x'z'+y'z'+yz'+xyz$
(B) Simplify following Boolean function using tabulation method. [5]
$F=\sum(0,1,2,8,10,11,14,15)$

OR

Q:2 (A) Obtain the simplified expressions in product of sums. [5]
$F(A,B,C,D)=\pi(0,1,2,3,4,10,11)$
(B) Prove that complement of EX-OR gate is result in EX-NOR gate. [5]

Q:3 Answer the following question.

(A) Write a short note about full subtractor with neat diagram. [5]
(B) Write a short note about decoder. [5]

OR

Q:3 (A) Design a combinational circuit to convert BCD code to excess-3 code converter. [5]
(B) Write a short note about multiplexer. [5]

Section II

Q:4 Attempt following.

(A) Write a short note about D flip flop with neat diagram. [5]

(B) Write down comparison between combinational circuits and sequential circuits. [5]

(C) Explain logic diagram of master-slave flipflop. [5]

OR

Q:4 (C) Write a short note about bidirectional shift register with parallel load with neat diagram. [5]

Q:5 Answer the following question.

(A) Write a short note about 4 bit binary ripple counter. [5]

(B) Explain state diagram of JK flipflop. [5]

OR

Q:5 (A) Write definitions about state table and state diagram. [5]

(B) What is ROM? Explain types of ROM memory. [5]

Q:6 Answer the following question.

(A) Explain difference between PLA and PAL. [5]

(B) Explain a short note about R-2R ladder type DAC. [5]

OR

Q:6 (A) Write down a short note about flash type ADC. [5]

(B) Write down a short note about successive approximation type ADC. [5]

21BECE30302

L.D.R.P Institute of Technology and Research, Gandhinagar
CE/IT Engineering Department
Mid Semester Examination -2022

Subject Name: Digital Electronics
Subject Code: CT304-N
Semester: 3rd

Date: 05/11/2022
Time: 1:30 to 3:00 pm
Total Marks: 30

Instructions: 1. Attempt all questions.
2. Make suitable assumptions wherever necessary.
3. Figures to the right indicate full marks.

Q:1 **(A)** Explain logic gates with its truth tables and symbol. [5]

Q:1 **(B)** Explain full adder circuit with neat diagram. [5]

Q:2 **(A)** Convert this. [5]

1. $(5217)_8=(\quad)_{10}$ 2703
2. $(250)_{10}=(\quad)_2$ 11111010
3. $(0.4375)_{10}=(\quad)_{16}$ 0.8F7D
4. $(0.25)_8=(\quad)_{10}$ 0.328125
5. $(250)_{10}=(\quad)_{16}$ 2A

(B) Simplify following Boolean expression using k-map. [5]
w'z+xz+x'y+wx'z

OR

Q:2 **(A)** Find 1's and 2's complement of $(10000000)_2$ [5]

(B) Implement function $F(A,B,C)=\sum(1,3,5,6)$ using 4*1 Multiplexer. [5]

Q:3 **(A)** Explain clocked SR flipflop in detail with neat diagram. [5]

(B) Implement function F=xy+x'y'+y'z using only OR and NOT gates. [5]

OR

Q13 **(A)** Explain JK flipflop in detail with neat diagram. [5]

(B) Design 4 bit synchronous binary counter using JK flipflop. [5]