

NORTH SOUTH UNIVERSITY



Department of Electrical and Computer Engineering Spring 2016 Report

BCD to 7-segment display

Course code: EEE 211

Course name: Digital Logic Design

Sec: 1

Group: ECE 234

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To all friends and others who shared the support financially or physically, thank you.

Above all, to the Great Almighty, the author of knowledge and wisdom.

We thank you.

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1. Introduction

1.1 Project description

This is a BCD to seven segment display project. This project consists of two phases. Sequential logic circuit and combinational logic circuit.

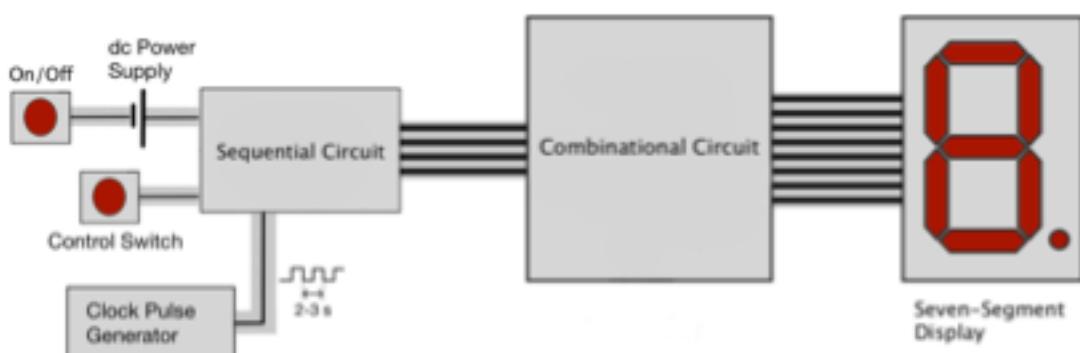


Figure 1: Circuit block diagram. Sequential circuit produces a sequence of codes. Code from sequential circuit is decoded by combinational circuit to light up corresponding segments of a seven-segment display.

Consider the digital system shown in Fig. 1. Switching on the circuit results in a string of characters “ECE234” being scrolled between 6 seven-segment display at a set time interval of 2-3 seconds, with the sequence (forward and backward) being controlled by the control switch.

The sequential logic circuit produces a sequence of codes that are required to

represent the string of characters for the seven-segment display. A control switch is present to change the direction of the sequence moving forward or backward. The sequential logic circuit is connected to a seven-segment display via a combinational logic circuit. The latter decodes the input codes from the sequential logic circuit in order to drive the individual segments of the seven-segment display to show each character as dictated by the sequence and the shift registers scroll the characters between the displays.

1.2 Project Gantt chart

	Start date	End date	Duration
Combinational Circuit Design	February 14	February 16	3 days
Combinational Circuit Implementation	5 march	7 march	3 days
Sequential Circuit Design	10 march	21 march	12 days
Final project setup	25 march	28 march	4 days



Figure: Gantt chart

2. Design

2.1 Design of Combinational Logic circuit

Reference	Character	A B C	a b c d e f g
0	E	0 0 0	1 0 0 1 1 1 1
1	C	0 0 1	1 0 0 1 1 1 0
2	2	0 1 0	1 1 0 1 1 0 1
3	3	0 1 1	1 1 1 1 0 0 1
4	4	1 0 0	0 1 1 0 0 1 1
5		1 0 1	d d d d d d d d
6		1 1 0	d d d d d d d d
7		1 1 1	d d d d d d d d

Truth Table

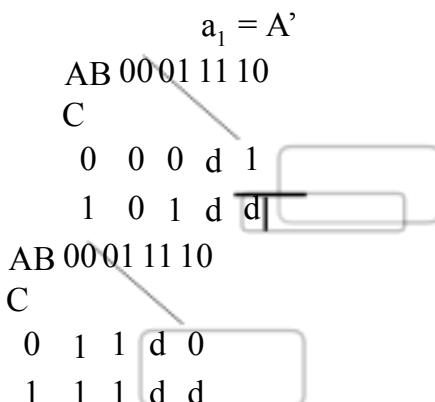
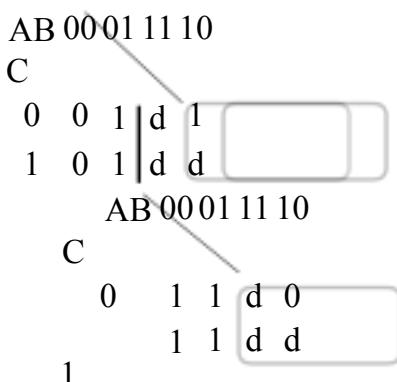
1st canonical form:

$$\begin{aligned}
 a_1 &= A'B'C' + A'B'C + A'BC' + A'BC \\
 b_1 &= A'BC' + A'BC + AB'C' \\
 c_1 &= A'BC + AB'C \\
 d_1 &= A'B'C' + A'B'C + A'BC' + A'BC \\
 e_1 &= A'B'C' + A'B'C + A'BC' \\
 f_1 &= A'B'C' + A'B'C + AB'C' \\
 g_1 &= A'B'C' + A'BC' + A'BC + AB'C
 \end{aligned}$$

2nd canonical form:

$$\begin{aligned}
 a_2 &= A' + B + C \\
 b_2 &= (A + B + C)(A + B + C') \\
 c_2 &= (A + B + C)(A + B + C')(A + B' + C) \\
 d_2 &= A' + B + C \\
 e_2 &= (A + B' + C')(A' + B + C) \\
 f_2 &= (A + B' + C)(A + B' + C') \\
 g_2 &= A + B + C'
 \end{aligned}$$

1st canonical minimal:



$$b_1 = A + B$$

$$c_1 = A + BC$$

$$\begin{array}{l} AB\ 0001\ 1110 \\ C \\ \begin{array}{cccccc} 0 & |1|1 & d & 0 \\ 1 & 1 & 0 & d & d \end{array} \end{array}$$
$$\begin{array}{l} AB\ 0001\ 1110 \\ C \\ \begin{array}{cccccc} 0 & 1 & 0 & d & 1 \\ 1 & 1 & 0 & d & d \end{array} \end{array}$$

$$d_1 = A'$$

$$e_1 = A'B' + A'C'$$

$$\begin{array}{l} AB\ 0001\ 1110 \\ C \\ \begin{array}{cccccc} 0 & 1 & 1 & d & 1 \\ 1 & 0 & 1 & d & d \end{array} \end{array}$$

$$f_1 = B'$$

$$g_1 = B + C'$$

2nd canonical minimal:

$$\begin{array}{l} AB\ 0001\ 1110 \\ C \\ \begin{array}{cccccc} 0 & 0 & 1 & d & 1 \\ 1 & 0 & 1 & d & d \end{array} \end{array}$$
$$\begin{array}{l} AB\ 0001\ 1110 \\ C \\ \begin{array}{cccccc} 0 & 1 & 1 & d & 0 \\ 1 & 1 & 1 & d & d \end{array} \end{array}$$

$$a_2 = A'$$

$$AB\ 0001\ 1110$$

$$b_2 = A + B$$

C	0	0	0	d	1
	1	0	1	d	d

AB 00011110

C	0	1	1	d	0	
	1	1	1	d	d	

$$c_2 = (A + C)(A + B)$$

$$d_2 = A'$$

AB 00011110

C	0	1	1	d	0	
	1	1	0	d	d	

AB 00011110

C	0	1	0	d	1	
	1	1	0	d	d	

$$e_2 = A'(B' + C')$$

$$f_2 = B'$$

AB 00011110

C	0	1	1	d	1
	1	0	1	d	d

$$g_2 = B + C'$$

Input for MUX

Reference	Character	A	B	C	a	b	c	d	e	f	g
0	E	0	0	0	1	0	0	1	1	1	C'
1	C	0	0	1							
2	2	0	1	0	1	1	C	1	0	0	1
3	3	0	1	1							
4	4	1	0	0	0	1	1	0	0	1	1
5		1	0	1							
6		1	1	0	d	d	d	d	d	d	d
7		1	1	1							

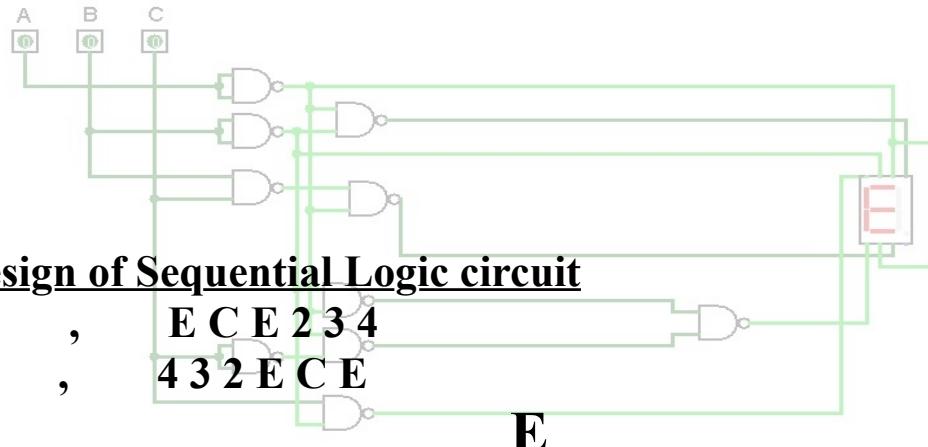
2.2 Justification of choice of design

We have used the minimal of 2nd canonical form of NAND gates for combinational logic. Since this circuit has the minimum number of logic gates, it will be cost efficient. No other gates are needed rather than only NAND gates and because of the use of only NAND gates, it is possible to integrated the gates in a single IC.

Literal cost Gate cost Cost with not gate

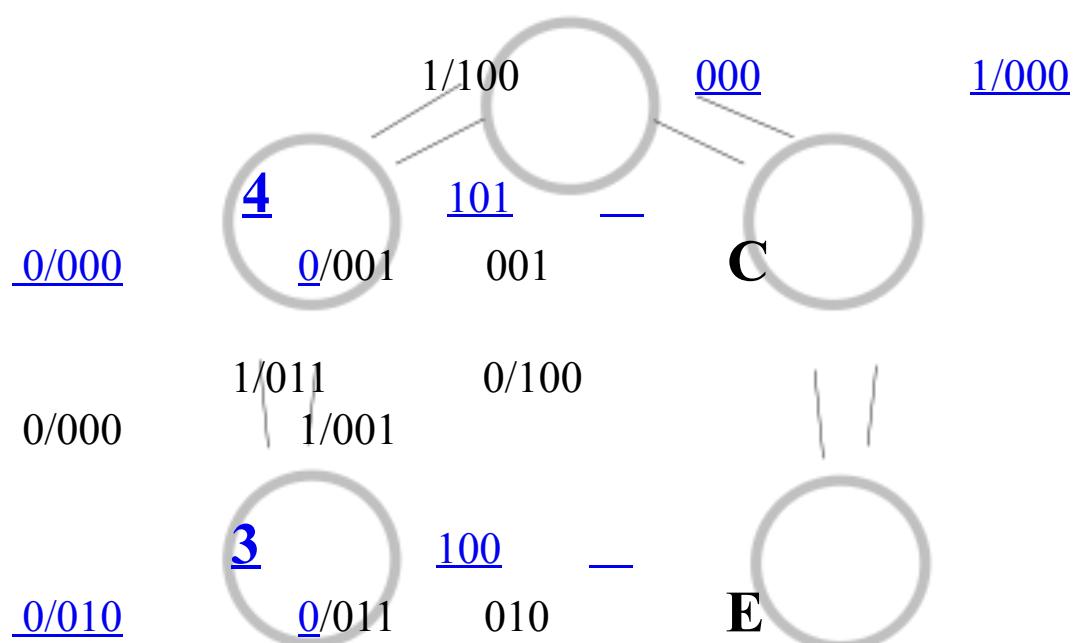
$$7 \quad 10 + 7 = 17 \quad 17$$

2.3 Simulation of Combinational circuit



2.4 Design of Sequential Logic circuit

$$\begin{array}{ll} I = 0 & , \\ I = 1 & , \end{array} \quad \begin{array}{l} E \ C \ E \ 2 \ 3 \ 4 \\ 4 \ 3 \ 2 \ E \ C \ E \end{array}$$



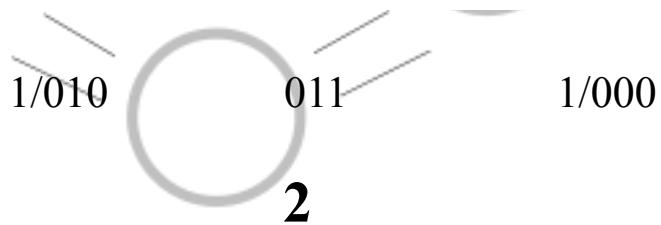


Figure: Mealy Model

Present state Next state Flip flop inputs

State Characteristics table

I	ABC	ABC	T _A	T _B	T _C	D _A	D _B	D _C	J _A	K _A	J _B	K _B	J _C	K _C
0	0 0 0	0 0 1	0	0	1	0	0	1	0	d	0	d	1	d
0	0 0 1	0 1 0	0	1	1	0	1	0	0	d	1	d	d	1
0	0 1 0	0 1 1	0	0	1	0	1	1	0	d	d	0	1	d
0	0 1 1	1 0 0	1	1	1	1	0	0	1	d	d	1	d	1
0	1 0 0	1 0 1	0	0	1	1	0	1	d	0	0	d	1	d
0	1 0 1	0 0 0	1	0	1	0	0	0	d	1	0	d	d	1
0	1 1 0	d d d	d	d	d	d	d	d	d	d	d	d	d	d
0	1 1 1	d d d	d	d	d	d	d	d	d	d	d	d	d	d
1	0 0 0	1 0 1	1	0	1	1	0	1	1	d	0	d	1	d
1	0 0 1	0 0 0	0	0	1	0	0	0	0	d	0	d	d	1
1	0 1 0	0 0 1	0	1	1	0	0	1	0	d	d	1	1	d
1	0 1 1	0 1 0	0	0	1	0	1	0	0	d	d	0	d	1
1	1 0 0	0 1 1	1	1	1	0	1	1	d	1	1	d	1	d
1	1 0 1	1 0 0	0	0	1	1	0	0	d	0	0	d	d	1
1	1 1 0	d d d	d	d	d	d	d	d	d	d	d	d	d	d
1	1 1 1	d d d	d	d	d	d	d	d	d	d	d	d	d	d

IA 00011110

BC

00 0 0 1 0

01 1 0 0 0

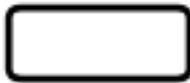
11 1 d d 0

10 0 d d 1 

1st canonical minimal:

IA 00011110

BC

00 0 0 1 1 

01 0 1 0 0 

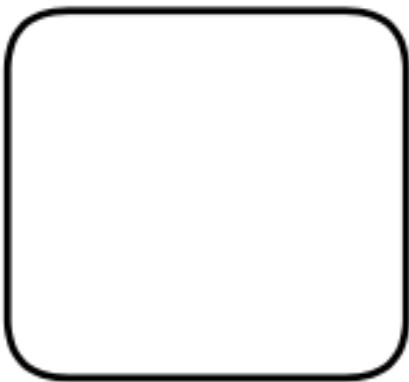
11 1 d d 0 

10 0 d d 0

$$T_{A1} = IB'C' + I'AC + I'BC \quad T_{B1} = I'A'C + IAC' + IBC'$$

IA 00011110

BC

00 1 1 1 1 

01 1 1 1 1

11 1 d d 1

10 1 d d 1

IA 00011110

BC

00 0 1 0 1 

01 0 0 1 0 

11 1 d d 0 

10 0 d d 0

$$T_{C1} = 1 \quad D_{A1} = IA'B'C' + IAC + I'AC' + I'BC$$

IA 0001 11 10
 BC
 00 0 0 1 0
 01 1 0 0 0
 11 0 d d 1
 10 1 d d 0

IA 0001 11 10
 BC
 00 1 1 1 1
 01 0 0 0 0
 11 0 d d 0
 10 1 d d 1

$$D_{B1} = I'A'B'C + IAC' + IBC + I'BC' \quad D_{C1} = C'$$

IA 0001 11 10
 BC
 00 0 d d 1
 01 0 d d 0
 11 1 d d 0
 10 0 d d 0

IA 0001 11 10
 BC
 00 d 0 1 d
 01 d 1 0 d

11 d d d d

10 d d d d

$$J_{A1} = I'BC + IB'C'$$

$$K_{A1} = I'C + IC'$$

IA 00011110

BC

00 0 0 1 0

01 1 0 0 0

11 d d d d

10 d d d d

IA 00011110

BC

00 d d d d

01 d d d d

11 1 d d 0

10 0 d d 1

$$J_{B1} = I'A'C + IA'C'$$

$$K_{B1} = I'C + IC'$$

IA 00011110

BC

00 1 1 1 1
01 d d d d
11 d d d d
10 1 d d 1



IA 00 01 11 10

BC

00 d d d d
01 1 1 1 1
11 1 d d 1
10 d d d d



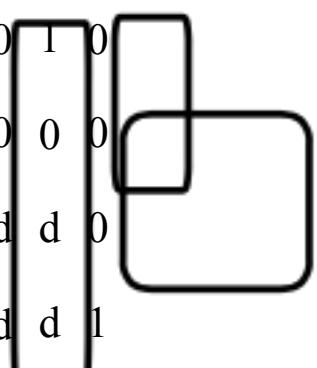
$J_{C1} = 1$

$K_{C1} = 1$

IA 00 01 11 10

BC

00 0 0 1 0
01 1 0 0 0 0
11 1 d d 0
10 0 d d 1



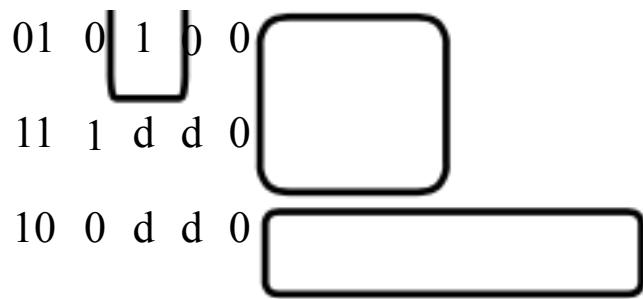
2nd canonical minimal:

IA 00 01 11 10

BC

00 0 0 1 1



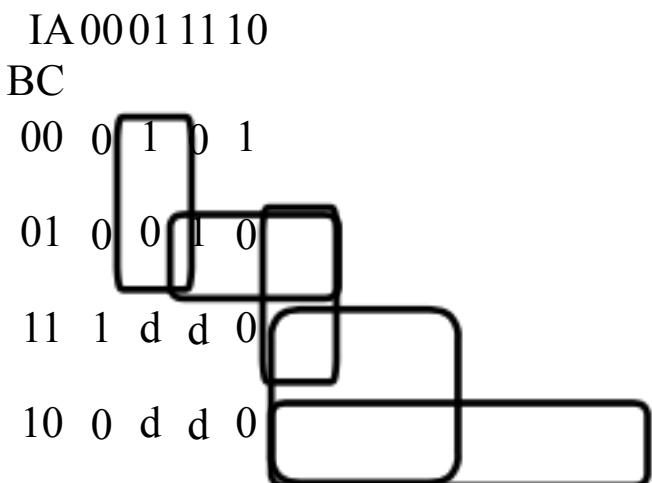


$$T_{A2} = (I+A+B)(I+C)(I'+C')(B'+C) \\ (I'+C')(I'+A+B)$$

$$T_{B2} = (I+C)(I+A')$$

IA 00011110
BC
00 1 1 1 1

01 1 1 1 1
11 1 d d 1
10 1 d d 1



$$T_{C2} = 0 \quad D_{A2} = (I+A+B)(I+B+C')(B'+C) (I'+A'+C)(I'+B') \\ (I'+A+C')$$

IA 00011110

BC

00	0	0	1	0	
01	1	0	0	0	
11	0	d	d	1	
10	1	d	d	0	

IA 00011110

BC

00 1 1 1 1

01 0 0 0 0

11 0 d d 0

10 1 d d 1

$$D_{C2} = C'$$

$$(I' + A + C)(I' + B + C')$$

IA 00011110

BC

00	0	d	d	1	
01	0	d	d	0	
11	1	d	d	0	
10	0	d	d	0	

IA 00011110

BC

00 d 0 1 d

01 d 1 0 d

11 d d d d

10 d d d d

$$J_{A2} = (I+B)(I'+C')(B'+C)$$

$$K_{A2} = (I+C)(I'+C')$$

IA 00011110

BC

00	0	0	1	0	
01	1	0	0	0	
11	d	d	d	d	
10	d	d	d	d	

IA 00011110

BC

00	d	d	d	d	
01	d	d	d	d	
11	1	d	d	0	
10	0	d	d	1	

$$J_{B2} = (I+C)(A'+C')(I'+A)$$

$$K_{B2} = (I+C)(I'+C')$$

IA 00011110

BC

00 1 1 1 1

01 d d d d

11 d d d d

10 1 d d 1

IA 00011110

BC

00 d d d d

01 1 1 1 1

11 1 d d 1

10 d d d d

$J_{C2} = 0$

ABC	A _O	B _O	C _O
0 0 0	0	0	0
0 0 1	0	0	1
0 1 0	0	0	0
0 1 1	0	1	0
1 0 0	0	1	1
1 0 1	1	0	0
1 1 0	d	d	d
1 1 1	d	d	d

$K_{C2} = 0$

Present state

Output

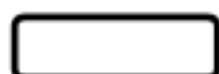
1st canonical minimal:

AB 00011110

C

0 0 0 D 0

1 0 0 d 1



$$A_{01} = AC$$

$$\begin{array}{c} AB00011110 \\ C \\ \begin{array}{ccccc} 0 & 0 & 0 & d & 1 \end{array} \boxed{} \\ \begin{array}{ccccc} 1 & 0 & 1 & D & 0 \end{array} \boxed{} \end{array}$$

$$B_{01} = AC' + BC$$

$$\begin{array}{c} AB00011110 \\ C \\ \begin{array}{ccccc} 0 & 0 & 0 & d & 1 \end{array} \boxed{} \\ \begin{array}{ccccc} 1 & 1 & 0 & d & 0 \end{array} \boxed{} \end{array}$$

$$C_{01} = AC' + A'B'C$$

2nd canonical minimal:

$$\begin{array}{c} AB00011110 \\ C \\ \begin{array}{ccccc} 0 & 0 & 0 & D & 0 \end{array} \boxed{} \quad \boxed{} \\ \begin{array}{ccccc} 1 & 0 & 0 & D & 1 \end{array} \boxed{} \end{array}$$

$$\begin{array}{c} A_{02} = AC \\ AB00011110 \end{array}$$

C	0	0	0	d	1	
	1	0	1	d	0	

$$B_{O2} = (A+C)(B+C')$$

AB	0	0	0	1	1	1	0
C	0	0	0	d	1		
	1	1	0	d	0		

$$C_{O2} = B'(A+C)(A'+C')$$

Sequential input for MUX

I	A	B	C	A	B	C	T _A	T _B	T _C	T _A	T _B	T _c	
0	0	0	0	0	0	1	0	C	1				
0	0	0	1	0	1	0							
0	0	1	0	0	1	1							
0	0	1	0	1	1	0							
0	0	1	1	1	0	0	1	C	C	1			
0	0	1	1	1	1	1							
0	1	0	0	1	0	1	0	0	1	C	0	1	
0	1	0	1	1	1	1							
0	1	0	1	0	0	1	1	0	1				
0	1	1	0	d	d	d	d	d	d	1	1	1	
0	1	1	1	d	d	d	d	d	d				
1	0	0	0	1	0	1	1	0	1	C'	0	1	
1	0	0	1	0	0	0							
1	0	1	0	0	1	0	0	1	1	0	C'	1	
1	0	1	1	0	1	0	0	1	1				
1	1	0	0	0	1	1	1	1	1	C'	C'	1	

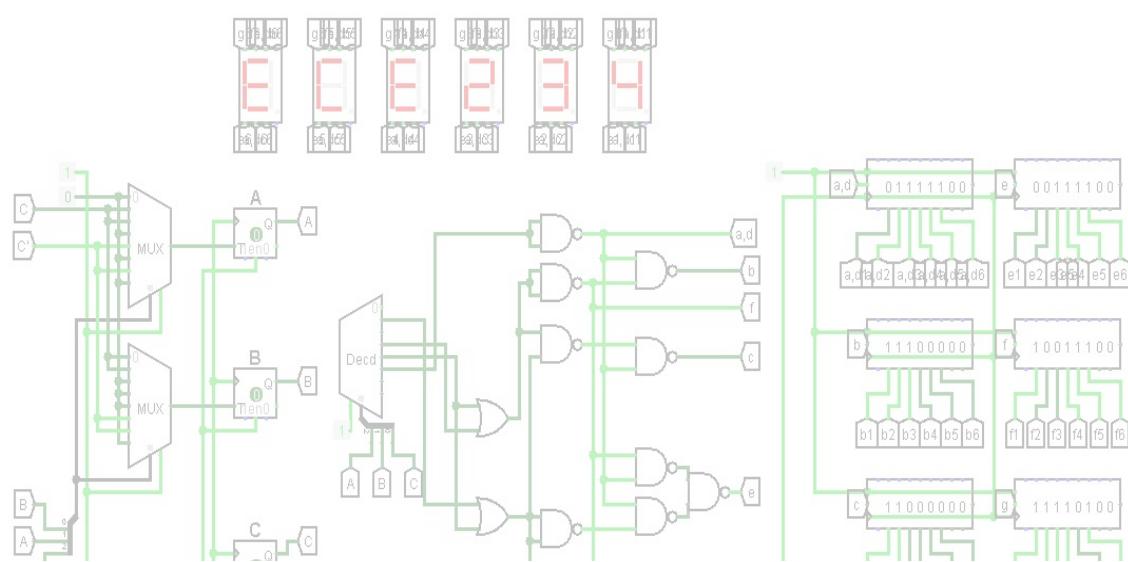
1	1	0	1	1	0	0	0	1				
1	1	1	0	d	d	d	d	d	1	1	1	
1	1	1	1	d	d	d	d	d				

2.5 Justification of choice of design

The sequential logic circuit we had choose to build is using two 8:1 MUX and three T flip flops. If we use T flip flop then T_C becomes 1 so we need 1 MUX less in our circuit.

But the alternate circuits need more ICs in place of MUX. The output logic circuit is simply a decoder and OR gates where only 2 ICs are need. So these choice made our circuit cost efficient.

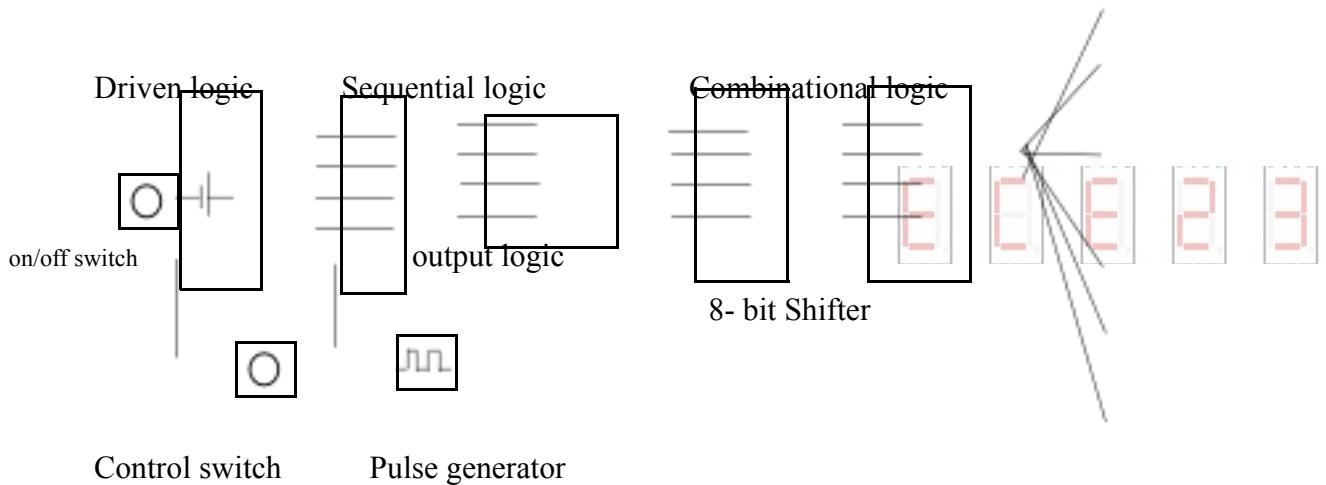
2.6 Simulation of Digital Logic circuit





3. Implementation

The circuit we have built is divided into 4 groups. Driven sequential logic, output logic, combination logic and shifter logic. In the sequential logic we have used two 8:1 MUX which is connected to the three T flip-flops. These flip flop will change the state with every clock pulse. The output from the flip flops are then connected to the output logic where a decoder and OR gates are connected. Then the output from the output logic circuit is connected to the combinational circuit of the sequence. The output from the combinational circuit is then connected to the 8-bit SIPO register which then connected to the six 7-segment display. The registers will help to scroll (forward and backward) the string of characters through the display with the help of a switch.



Equipment

Components	Specification	Quantity
8:1 MUX	IC 74151	2 pieces
J-K flip flop	IC 74107	2 pieces
3 to 8 line Decoder	IC 74238	1 piece
OR gates	IC 7432	1 piece
NAND gates	IC 7400	3 pieces

8-bit shift register	IC 74164	6 pieces
Timer	NE555N	1 piece
7 segment display		6 pieces
Capacitor	100 uF, 1 nF	1 piece each
Resistor	27 kΩ, 1 kΩ, 100 Ω	1 piece, 1 piece, 6 pieces
Battery		4 x 1.5 AA
Switch		2 pieces
Breadboard		4 unit
Jumper wire		

Hardware used

[7432](#)



[74151](#)

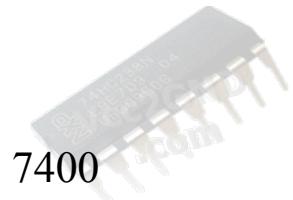


[74107](#)

[74164](#)



[74238](#)



[7400](#)



7-segment display



NE555N

4. Conclusion

We have successfully completed our project though we faced many problems while building circuits. We have made the connections as we have chosen in our schematic diagram. The circuit is working well and the characters are also scrolling through the six 7-segment displays.

4.1 Budget

Product	Quantity	Units price	Price
ICs	15	25	375
Timer	1	8	8
7 segment display	6	10	60
Breadboard	4	140	560
Jumper wire	4 set	90	360
			Total 1363

4.2 Difficulties faced

We have faced many difficulties through our project. Sometimes neither ICs were working properly nor breadboard, or 7-segment displays got damaged due to high input voltage. So we have to check every ICs, breadboard or displays before making connections. It is very difficult to identify a problem after the setup of whole circuit. If we do not check every components before implementation then we have to start again from the beginning.

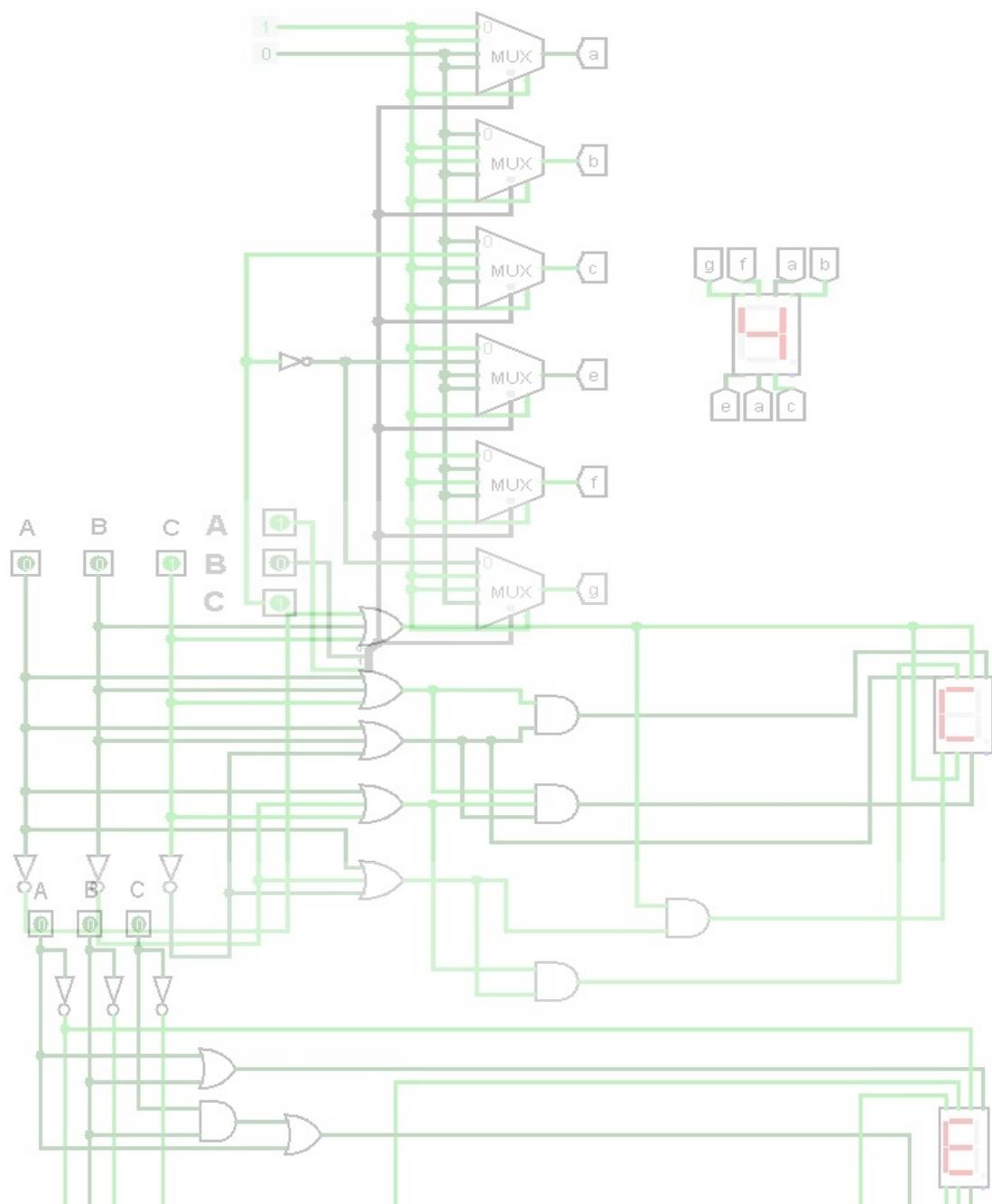
4.3 Future Recommendation

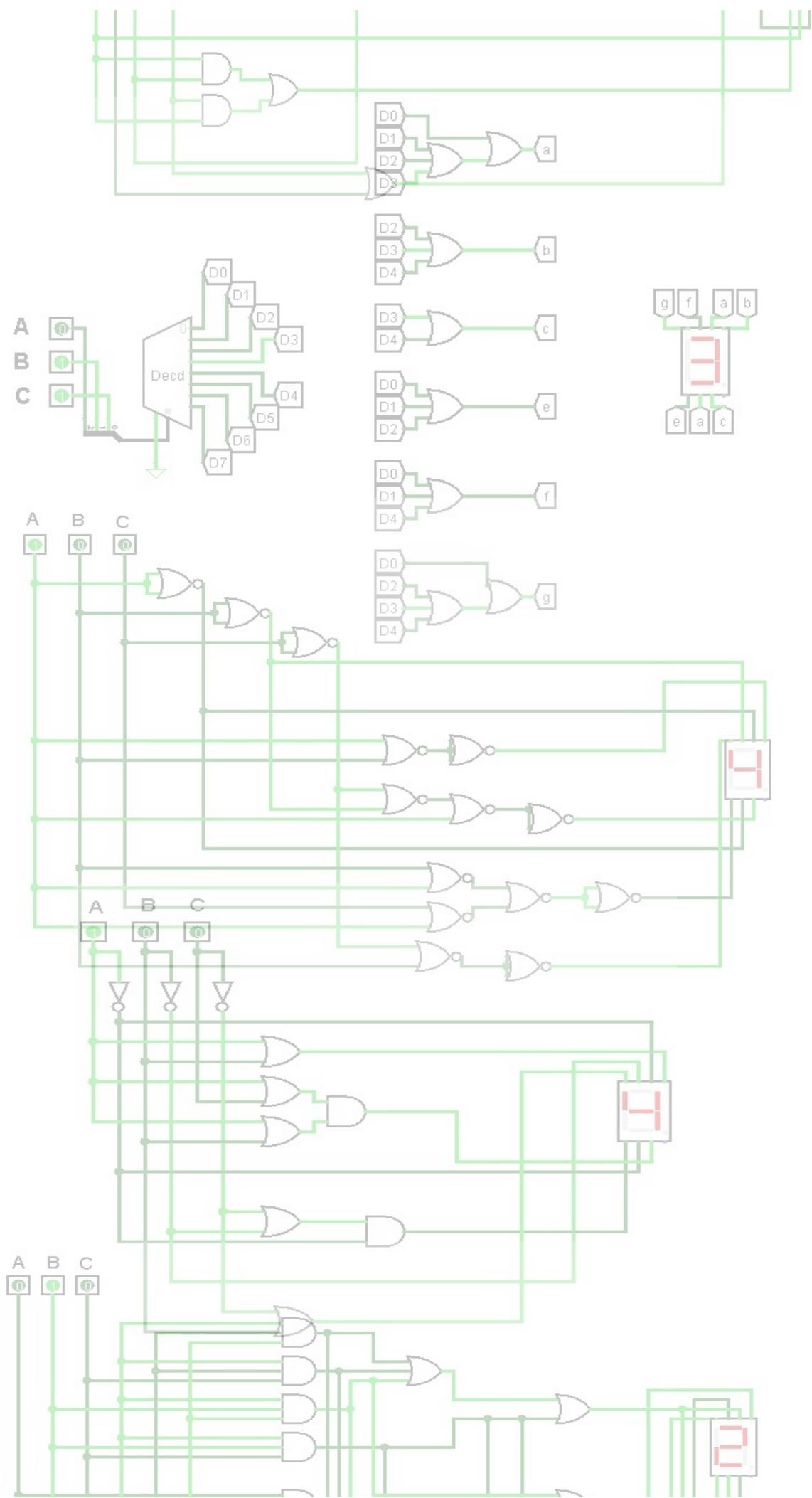
We can integrated the whole circuit in a single IC. So it will become more compact and will be user friendly. An user can just buy an IC and convert BCD to seven-segment display without making complicated connections using

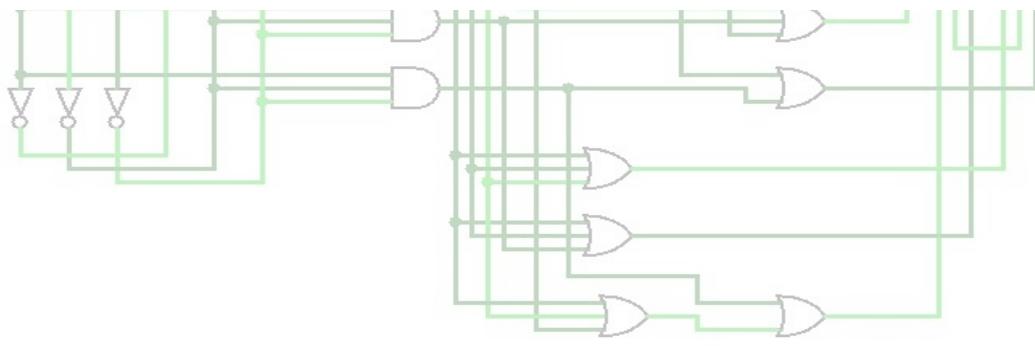
multiple ICs. We can even use more multiple displays to scroll a string of characters and hang in a public place to print different messages to people.

5. Appendix A

Logisim schematics of alternate combinational logic circuits

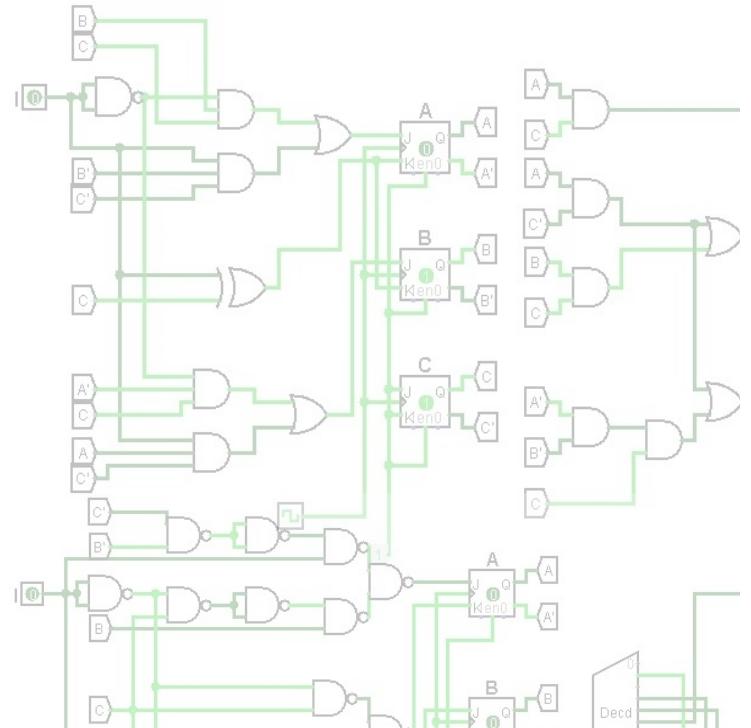


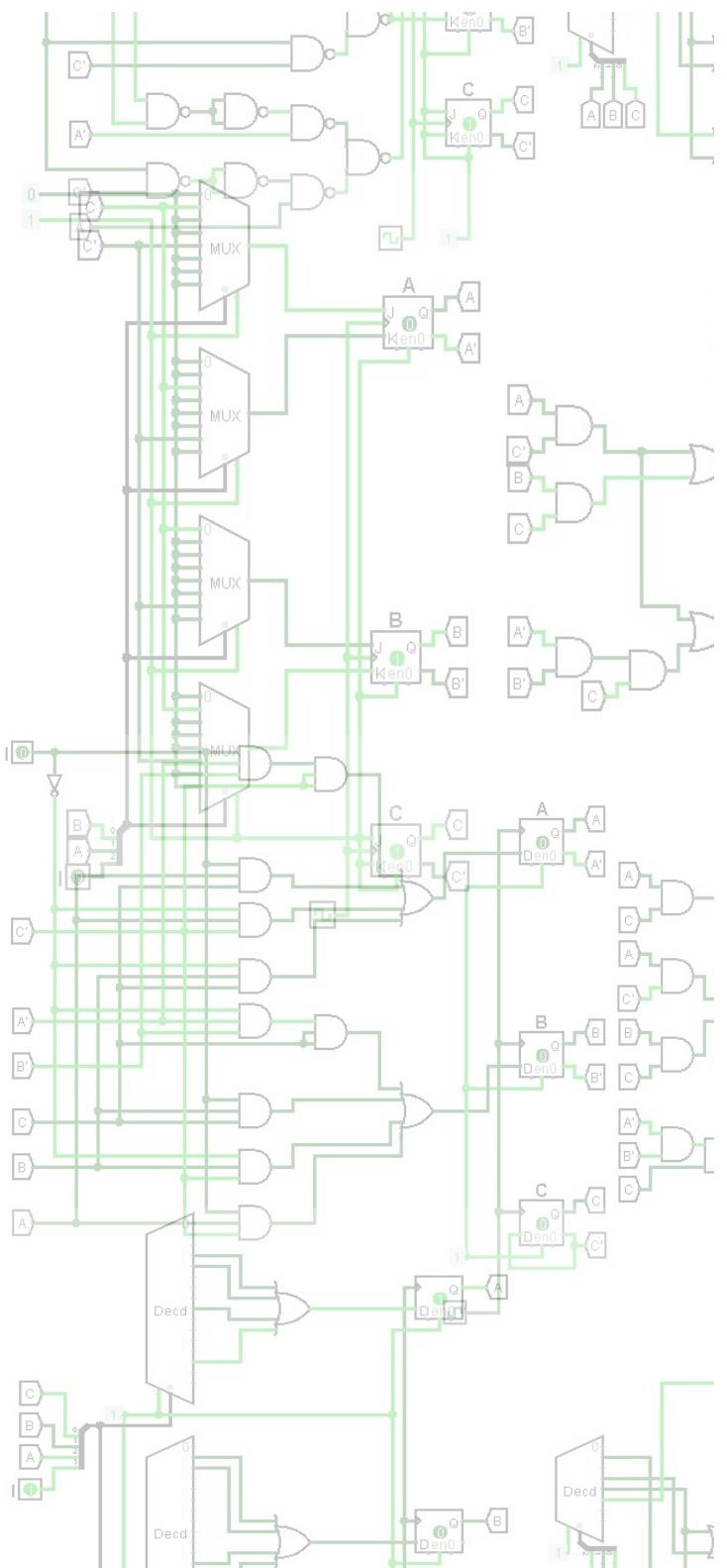


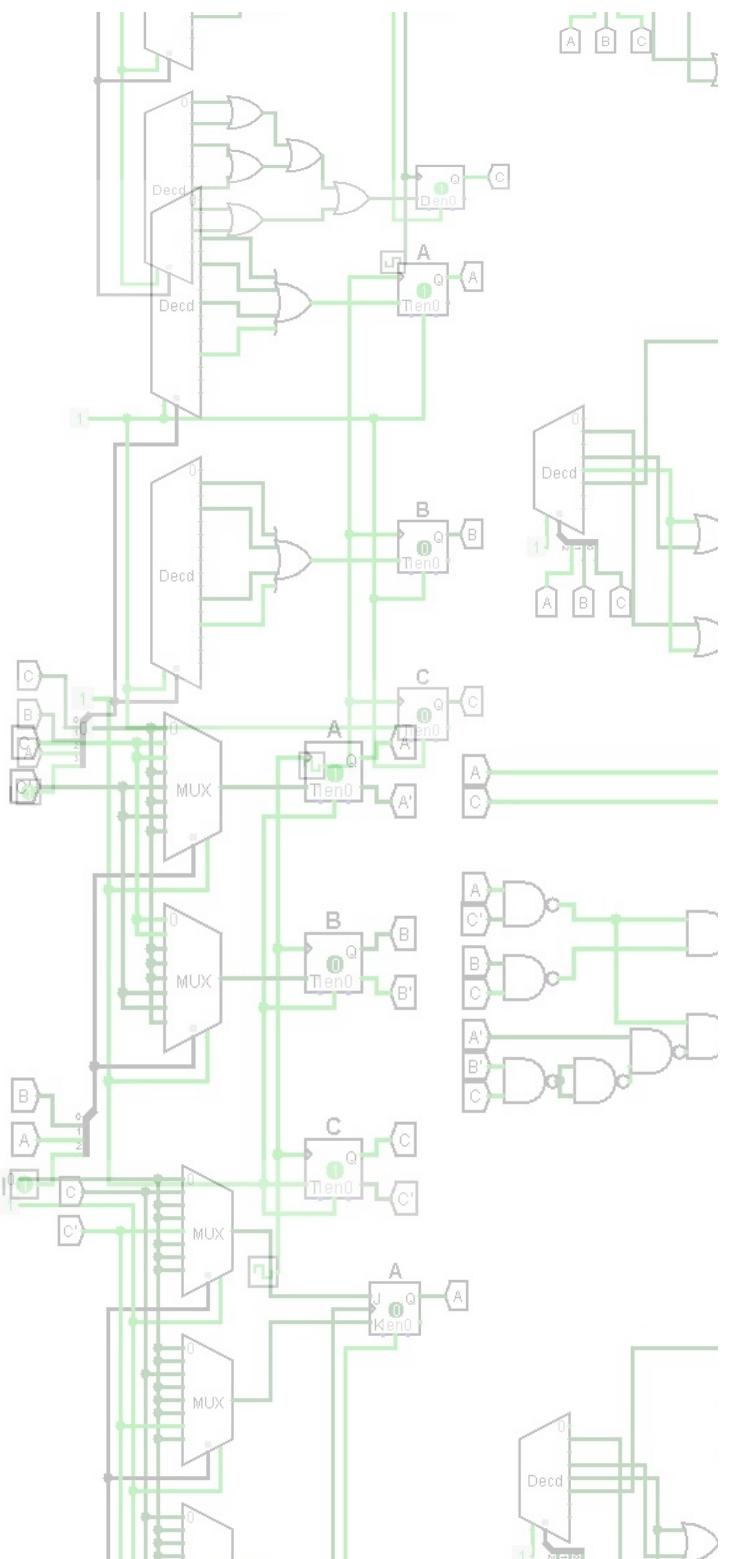


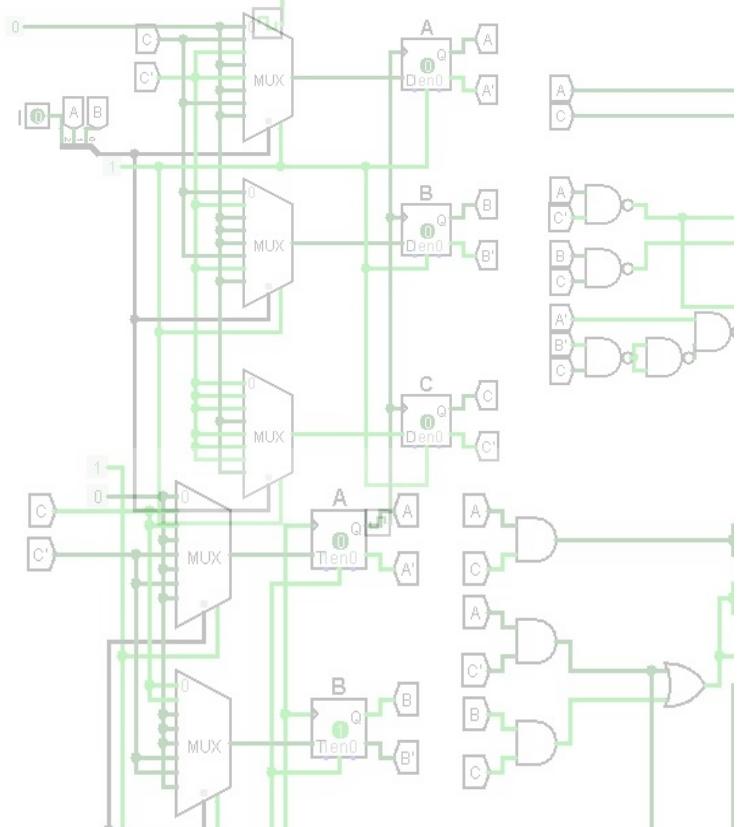
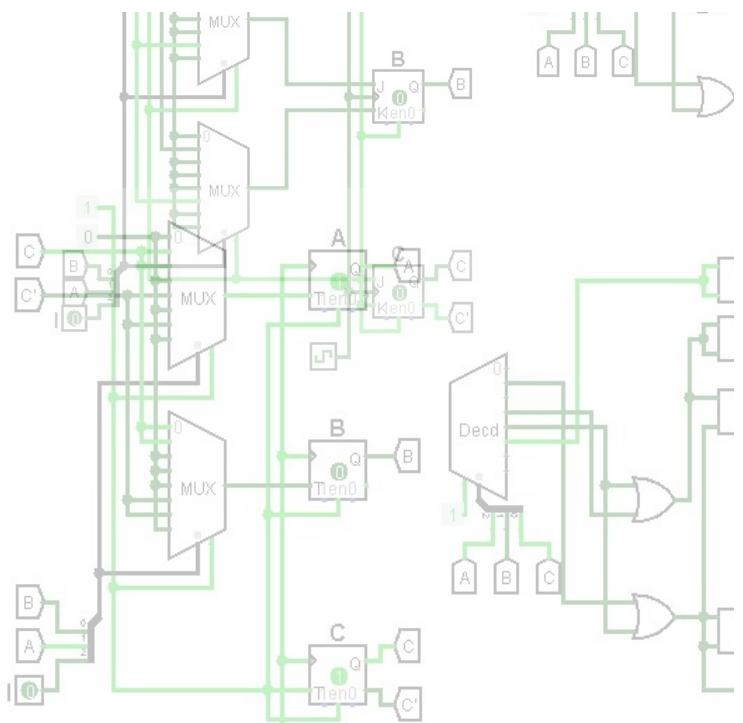
6. Appendix B

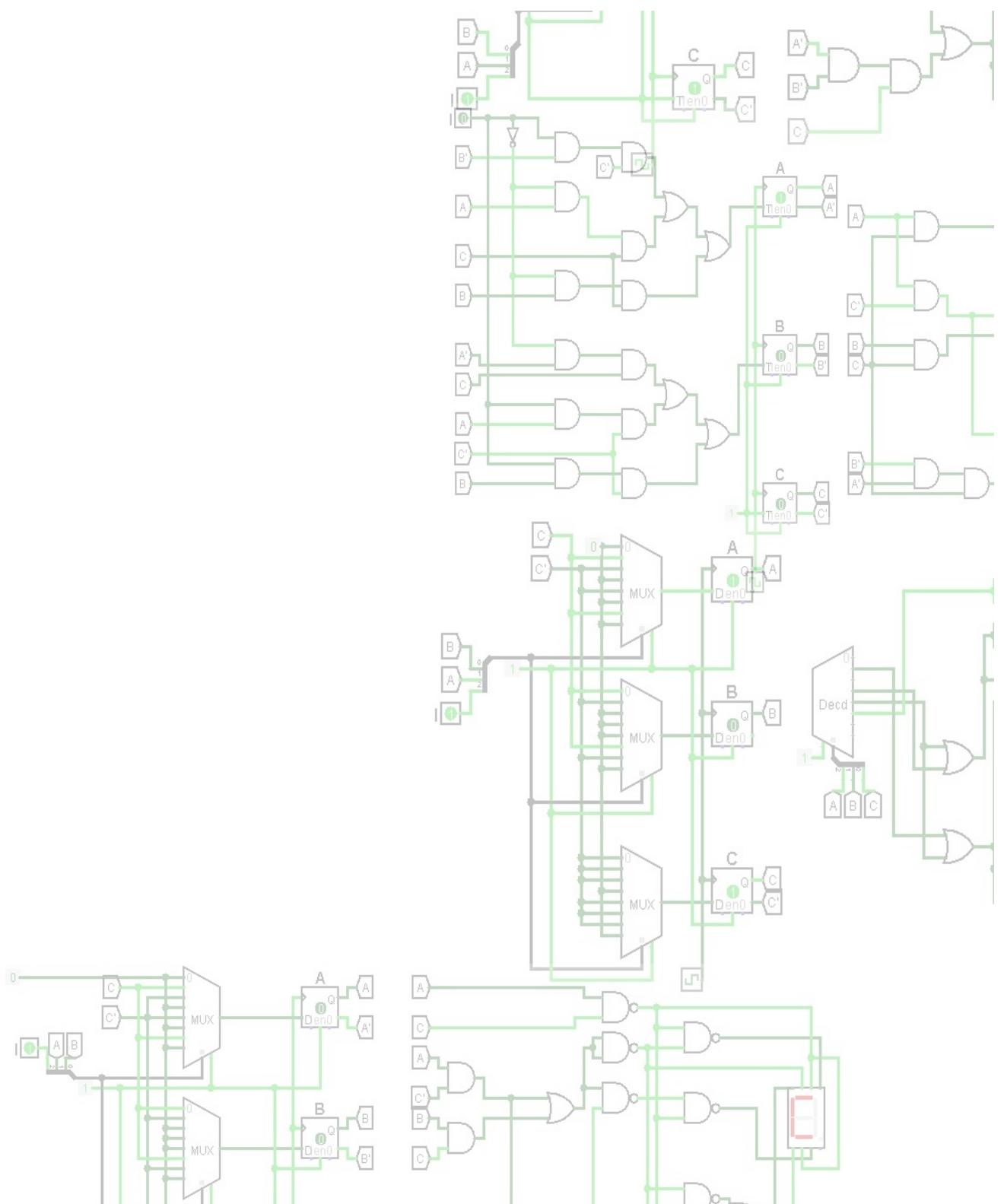
Logisim schematics of alternate sequential logic circuits











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