NORTH SOUTH UNIVERSITY

Department of Electrical and Computer Engineering
Summer 2019
Report
BCD to 7-segment display

Course code: CSE231
Course name: Digital Logic Design
Sec: 6
Group: 03
Submitted to:

Group members:

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Acknowledgement

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To all friends and others who shared the support financially or physically, thank you.

Above all, to the Great Almighty, the author of knowledge and wisdom.

We thank you.

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1. Introduction

1.1 Project description

This is a BCD to seven segment display project. This project consists of two main parts. Sequential logic circuit and combinational logic circuit.

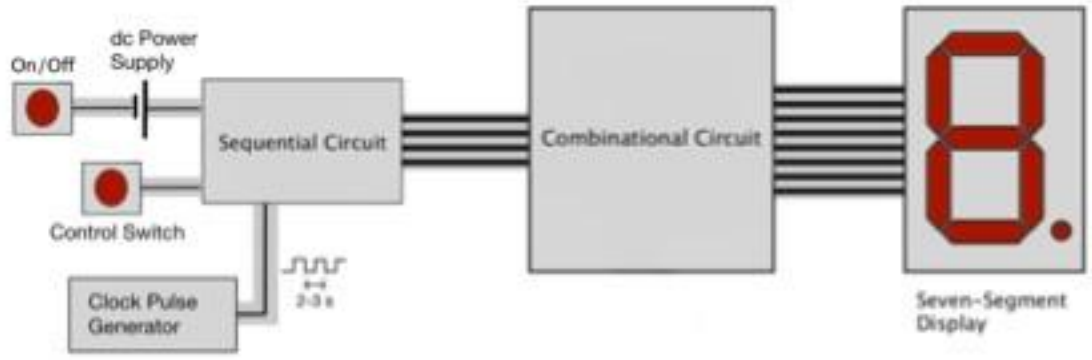


Figure 1: Circuit block diagram. Sequential circuit produces a sequence of codes. Code from sequential circuit is decoded by combinational circuit to light up corresponding segments of a seven-segment display.

Consider the digital system shown in Fig. 1. Switching on the circuit results in a string of characters “CSE231-6-3” being scrolled between 10 seven-segment display at a set time interval of 1-2 seconds.

The sequential logic circuit produces a sequence of codes that are required to represent the string of characters for the seven-segment display. A control switch is present to change the direction of the sequence moving forward or backward. The sequential logic circuit is connected to a seven-segment display via a combinational logic circuit. The latter decodes the input codes from the sequential logic circuit in order to drive the individual segments of the seven-segment display to show each character as dictated.

1.2 Project Gantt chart

	Start date	End date	Duration
Combinational Circuit Design	Aug’22	Feb’22	1-day
Combinational Circuit Implementation	Aug’ 28	Aug’ 30	3 days
Sequential Circuit Design	Aug’23	Aug’ 24	2 days
Final project setup	Aug 30	Aug 31	2 days

2. Design

2.1 Design of Combinational Logic circuit

Reference	Character	WXYZ	abcdefg
0	C	0000	1001110
1	S	0001	1011011
2	E	0010	1001111
3	2	0011	1101101
4	3	0100	1111001
5	1	0101	0110000
6	-	0110	0000001
7	6	0111	1011111
8	-	1000	0000001
9	3	1001	1111001
10	*	1010	*******
11	*	1011	*******
12	*	1100	*******
13	*	1101	*******
14	*	1111	*******
15	*		

Figure: Truth Table

K-Maps

Output: a

Format: Sum of products

W, X \ Y, Z	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	0	0	1	0
10	0	1	1	0

$\overline{W}\,\overline{X} + \overline{W}\,\overline{Y}\,\overline{Z} + \overline{X}\,Z + Y\,Z$

Set As Expression

Output: b

Format: Sum of products

W, X \ Y, Z	00	01	11	10
00	0	0	1	0
01	1	1	0	0
11	1	1	1	0
10	0	1	1	0

$\overline{X}\,Y\,Z + X\,\overline{Y} + W\,Z$

Set As Expression

Output: c

Format: Sum of products

W, X \ Y, Z	00	01	11	10
00	0	1	0	0
01	1	1	1	0
11	1	1	1	0
10	0	1	0	0

$\overline{Y}\,Z + X\,\overline{Y} + X\,Z$

Set As Expression

Output: d

Format: Sum of products

W, X \ Y, Z	00	01	11	10
00	1	1	1	1
01	1	0	1	0
11	0	0	1	0
10	0	1	1	0

$\overline{W}\,\overline{X} + \overline{W}\,\overline{Y}\,\overline{Z} + \overline{X}\,Z + Y\,Z$

Set As Expression

Output: e

Format: Sum of products

W, X \ Y, Z	00	01	11	10
00	1	0	1	1
01	0	0	1	0
11	0	0	1	0
10	0	0	1	0

$\overline{W}\,\overline{X}\,\overline{Z} + Y\,Z$

Set As Expression

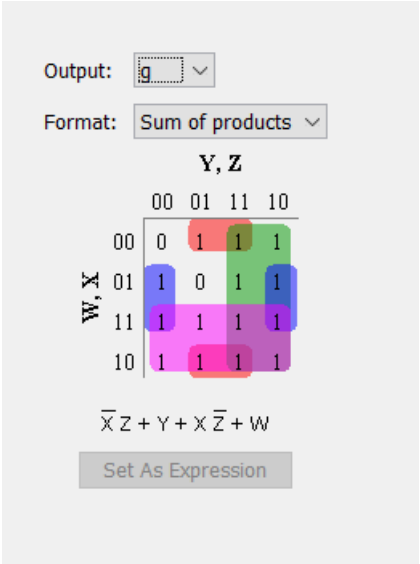
Output: f

Format: Sum of products

W, X \ Y, Z	00	01	11	10
00	1	1	0	1
01	0	0	1	0
11	0	0	1	0
10	0	0	0	0

$\overline{W}\,\overline{X}\,\overline{Y} + \overline{W}\,\overline{X}\,\overline{Z} + X\,Y\,Z$

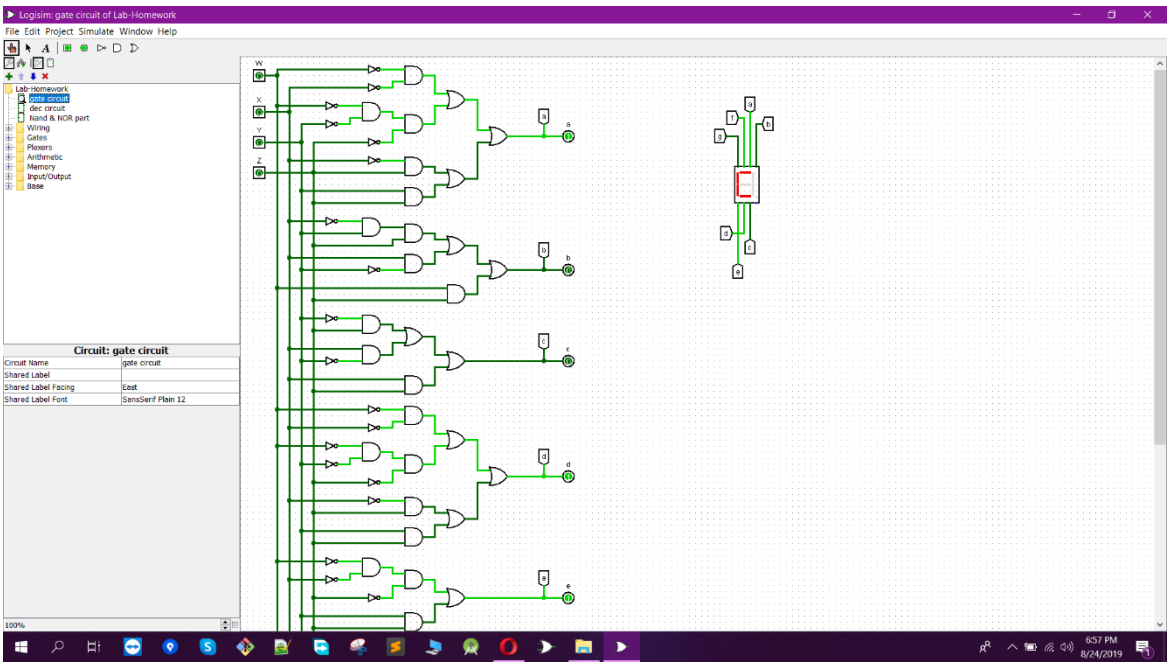
Set As Expression

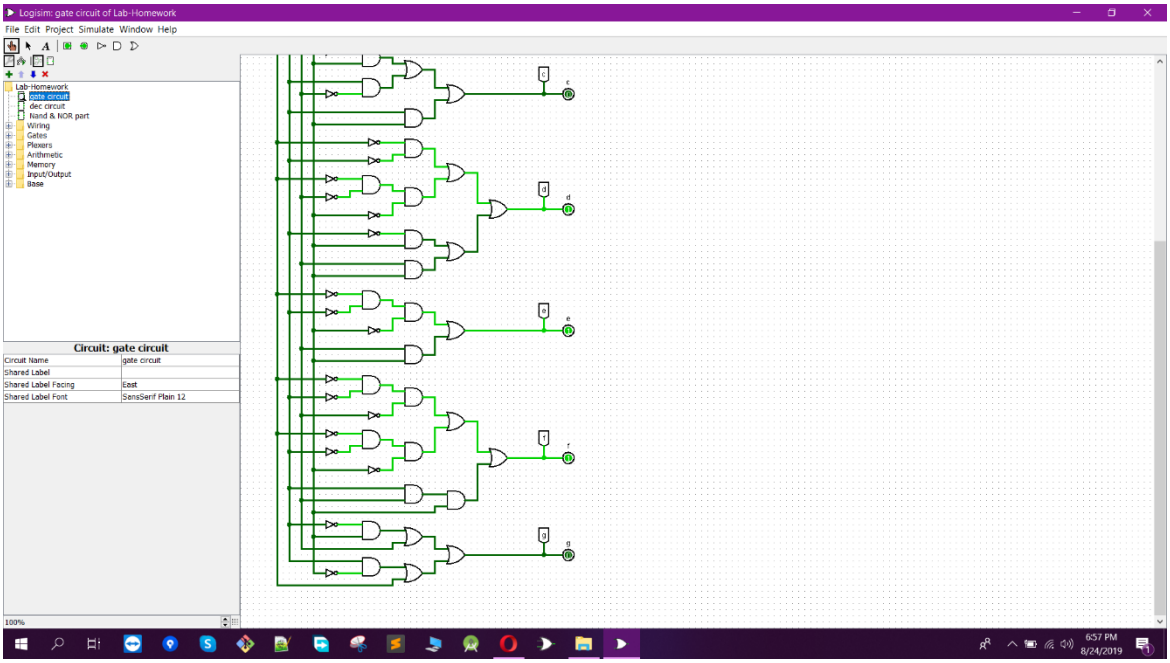


2.2 Justification of choice of design

We have used the minimal of basic gates of AND and OR gates for combinational logic circuit. Since this circuit has the minimum number of logic gates, it will be cost efficient. No other gates are needed rather than only AND, OR and NOT gates.

2.3 Simulation of Combinational circuit





2.4 Design of Sequential Logic circuit

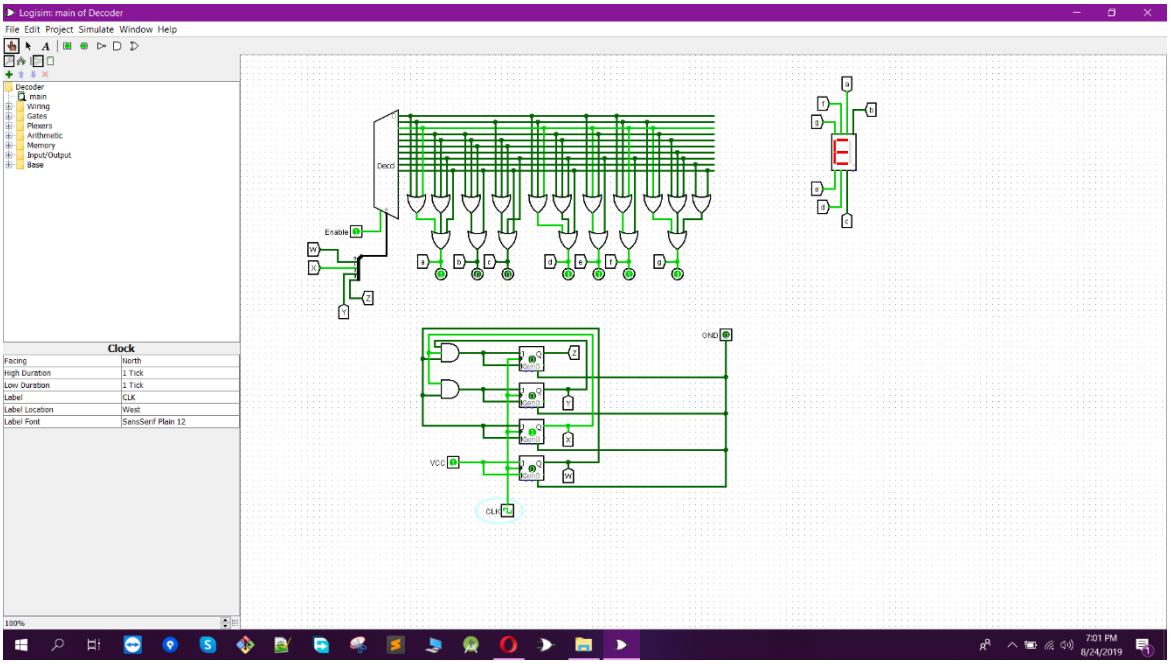


Figure: Sequential Logic Circuit

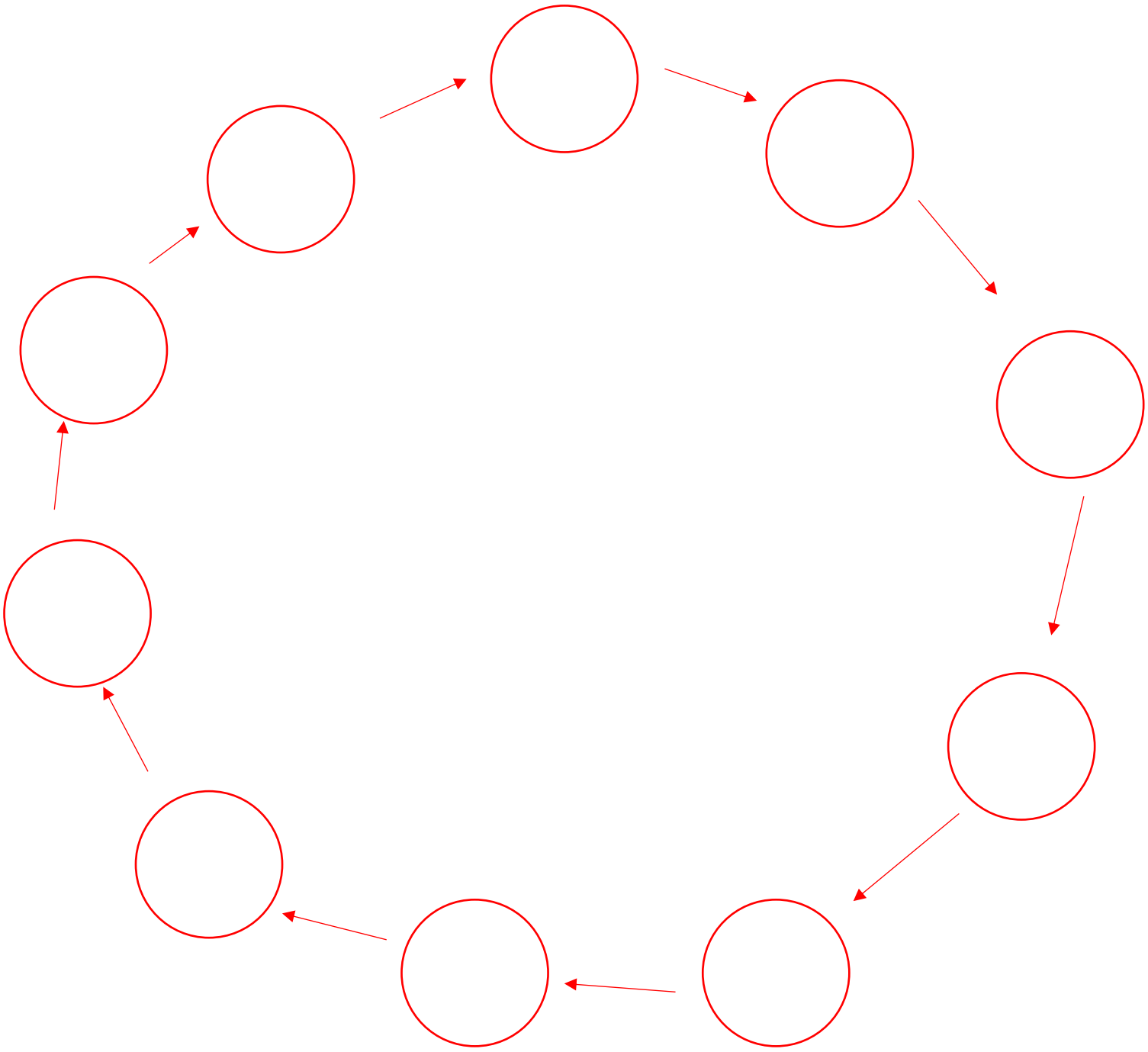
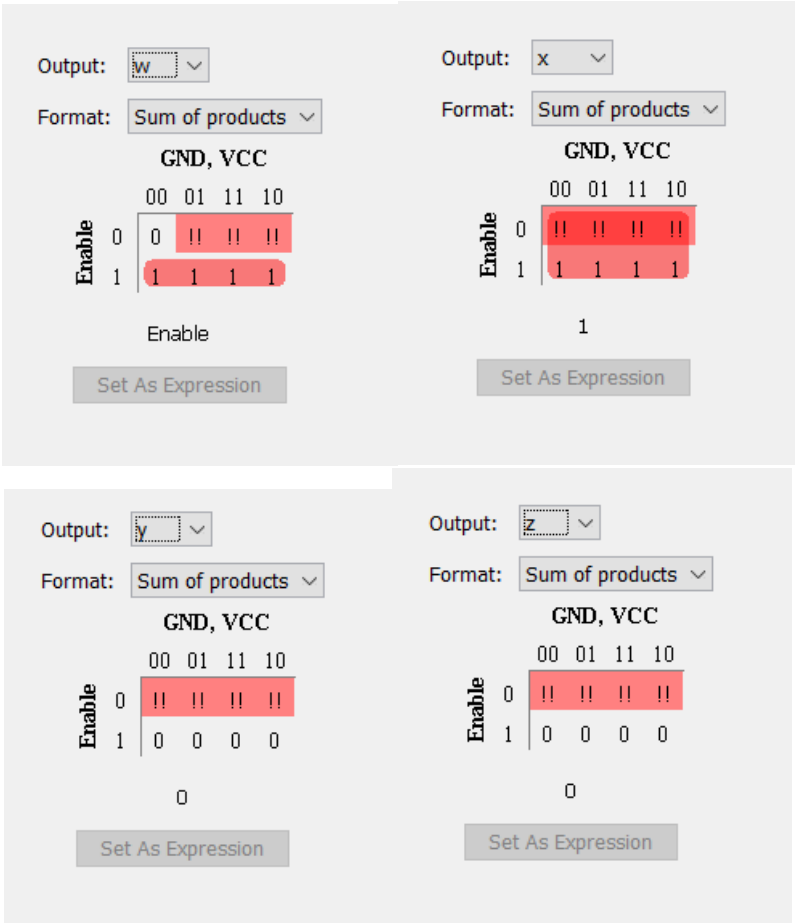


Figure: State Diagram of the Design

	Present State				Next State				Output				
	Wt	Xt	Yt	Zt	Wt+1	Xt+1	Yt+1	Zt+1	Tw	Tx	Ty	Tz	Display
0	0	0	0	0	0	0	0	1	0	0	0	1	C
1	0	0	0	1	0	0	1	0	0	0	1	1	S
2	0	0	1	0	0	0	1	1	0	0	0	1	E
3	0	0	1	1	0	1	0	0	0	1	1	1	2
4	0	1	0	0	0	1	0	1	0	0	0	1	3
5	0	1	0	1	0	1	1	0	0	0	1	1	1
6	0	1	1	0	0	1	1	1	0	0	1	1	-
7	0	1	1	1	1	0	0	0	1	1	1	1	6
8	1	0	0	0	1	0	0	1	0	0	0	1	-
9	1	0	0	1	0	0	0	0	1	0	0	1	3

Figure: Characteristic Table of the Design

K-Maps

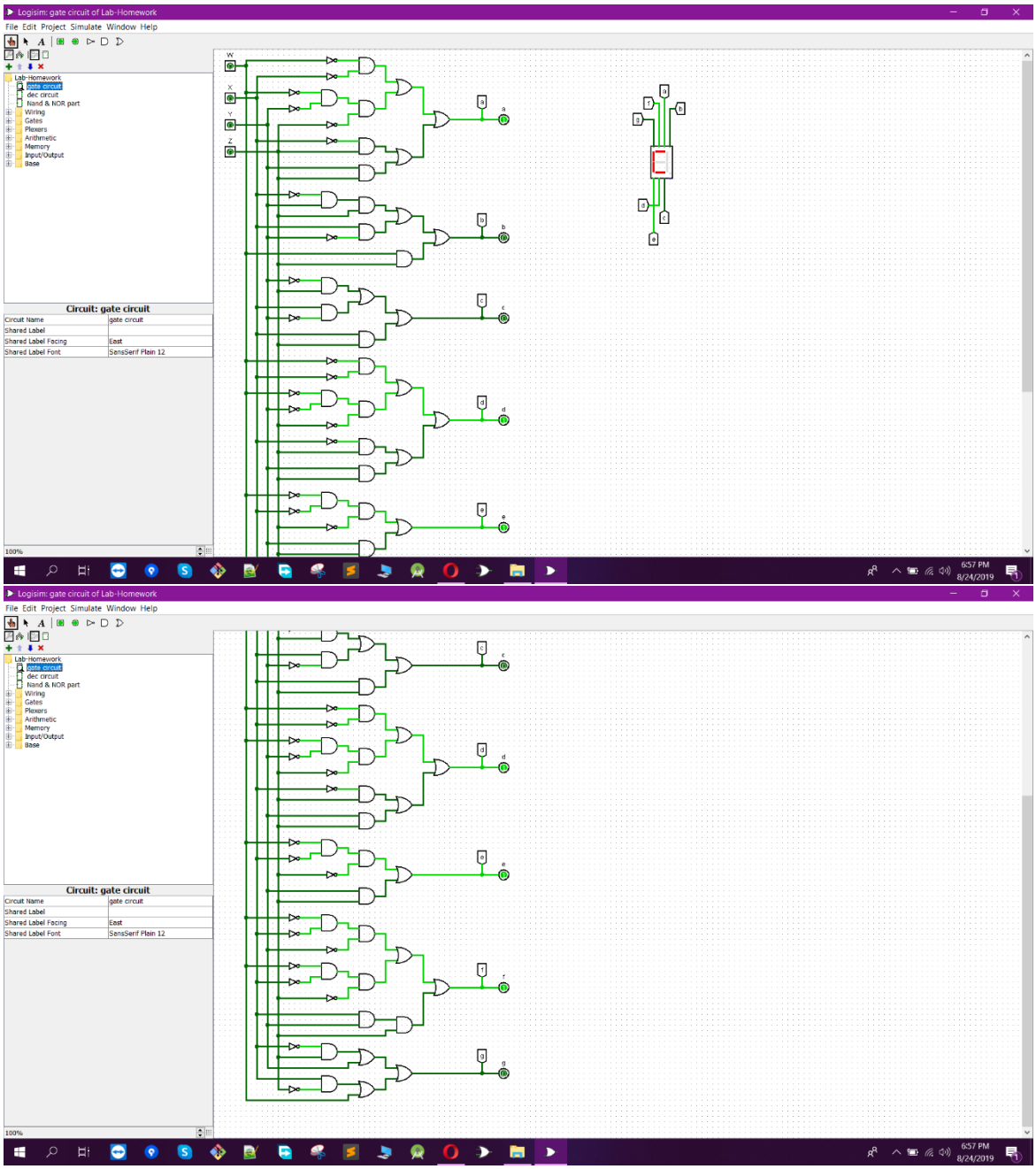


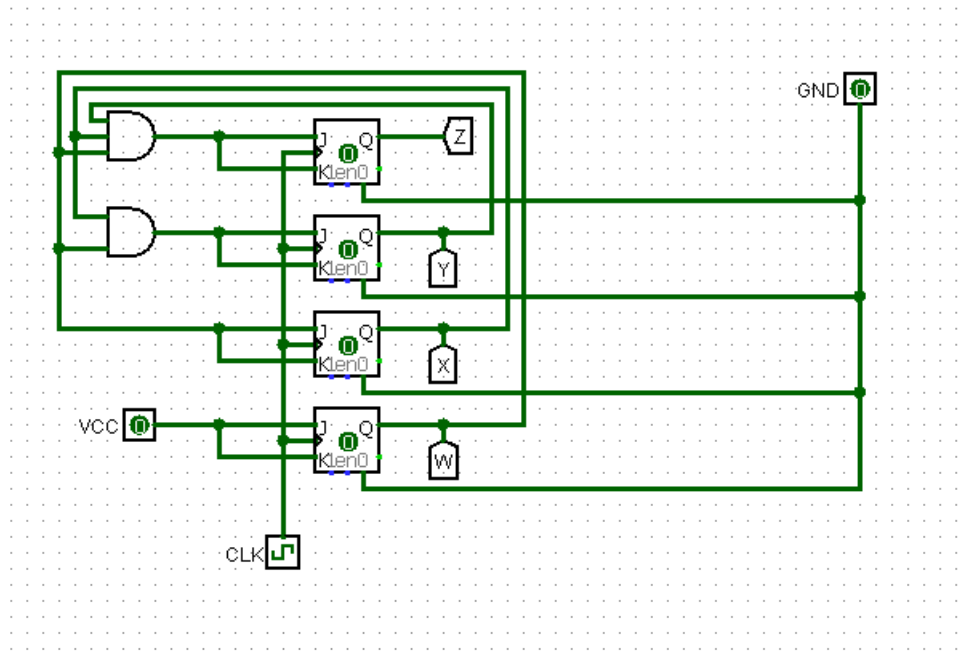
2.5 **Justification of choice of design**

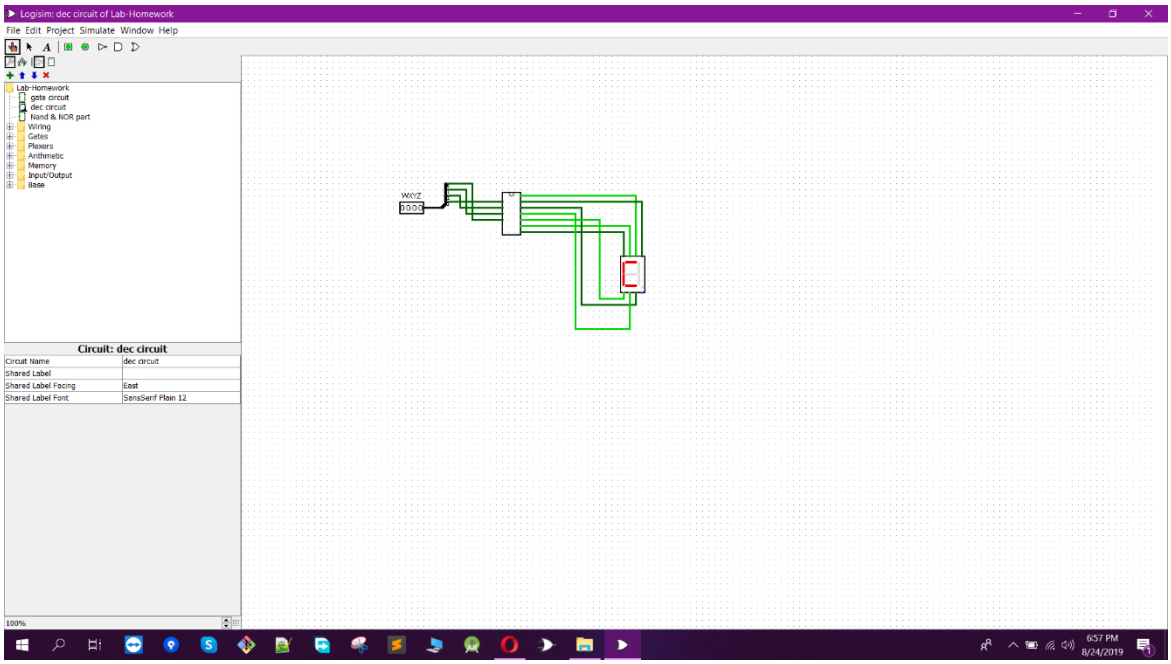
The sequential logic circuit we chose to build is using two 8:1 MUX and three T flip flops. If we use T flip flop then T_C becomes 1 so we need 1 MUX less in our circuit.

But the alternate circuits need more ICs in place of MUX. The output logic circuit is simply a decoder and OR gates where only 2 ICs are need. So, these choices made our circuit cost efficient.

2.6 **Simulation of Digital Logic circuit**




GND
VCC
CLK
J
Q
K
Z
Y
X
W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File Edit Project Simulate Window Help
Lab-Homework
gate circuit
dec circuit
Nand & NOR part
Wiring
Gates
Plexors
Arithmetic
Memory
Input/Output
Base
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Circuit Name
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Shared Label
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SansSerif Plain 12
100%
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3. Implementation

Description

The circuit we have built can be divided into 3 groups, sequential logic, combinational logic and output logic. In the sequential logic, we have used AND, OR, NOT gates, JK Flipflops, amplifier, 7-segment display, 555 timer ic, LEDs. The flipflops changes the states with every clock pulse. The connection goes to the 7-Segment Display followed by the combinational circuit of the sequence. The output is observed from the 7-segment display.

Equipment Required

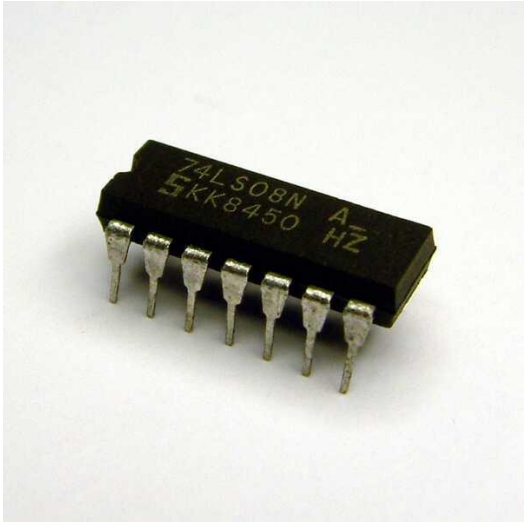
	Component	IC Number	Quantity	Price
1	3 input OR gate	IC7411	3	22*3=66
2	Display	Common Cathode 7 segment Display	1	13
3	Timer	IC555	1	8
4	J-K flip flop	IC7476	2	24
5	2 input AND gate	IC7408	4	25*4=100
6	Resistors	-	2	4
7	LED	-	1	2
8	Wires	-	As required	150
9	Bread Board	-	4	90*4=360
10	Battery	-	3 (9v)	45
Total				772

Hardware used

1. 7411 IC

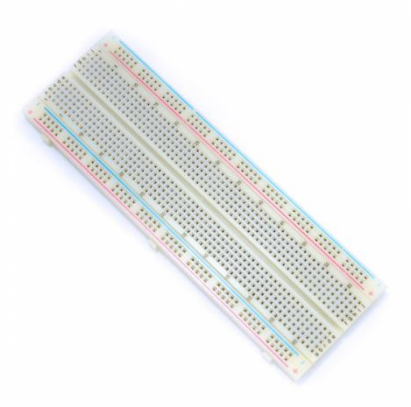
2. 7476 IC

3. 7408 IC

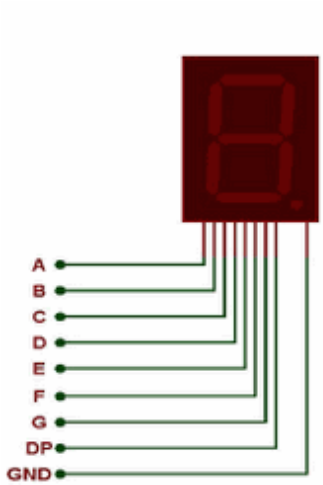


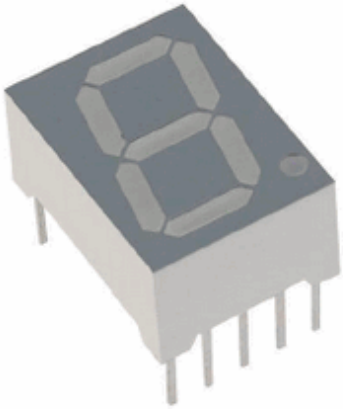
4. LED

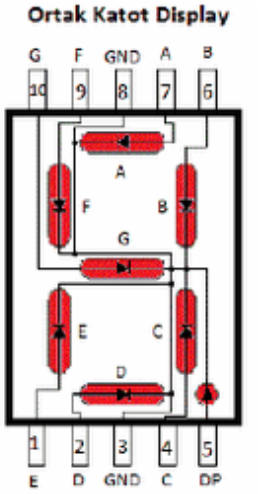
5. Breadboard



6. 7-Segment Display







7. Battery

4. Conclusion

Despite of all the hardships, we have been able to complete the project successfully. We have made the connections as shown in the schematic diagrams. We are delighted to say that the circuit is working fine and the characters are also scrolling through the 7-segment display.

4.2 **Difficulties faced**

Throughout this project we have face many difficulties. Starting from implementation, we tried implementing the circuit using decoder, but for unavailability we could not get active-high decoder and proper outputs did not show with active-low decoder. So, we had to switch to basic gates. This took our time and also couple LEDs got damaged. Also, we had to check each ICs and flipflops and 7-segment display before using them to avoid faulty equipment. We had to be very careful with all the devices because of their sensitivity. We had to learn how to build clock pulse with the help of Google, which was very confusing and also consumed a lot of time.

4.3 **Future Recommendation**

We implement this circuit for lengthier displays. We can also use multiple displays to scroll a string of characters for general purpose to print different messages in public places. This can be used for practical purpose as signboards or etc.

5. **Appendix A**

Logisim schematics of alternate combinational logic circuits