Final Homework Summer 2019 ***(CSE231.6 – Asif Ahmed Neloy)***
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Introduction

The following project covers most of the topics of CSE231. The aim of the project is to access the students' ability to tie in theoretical and experimental knowledge from CSE231 to complete a practical project on Digital Logic Design and to work in a team.

The homework consists of three phases. The project description is given in Sec. 1. Objectives and tasks for each phase of the project are described in Sec. 3. Each phase consists of an individual deadline that is summarized in Sec. 4. It is imperative that you meet all deadlines in order to complete the full project in due time. The mark distribution for the Homework is also summarized in Sec. 4.

This homework idea is derived from project outline provided by Dr. Arshad Chowdhury (AMC) Sir back in Summer 2016.

Project Description

Consider the digital system shown in Fig. 1. Switching on the circuit results in the string of characters "**CSE231-section no.-Group no.**" being displayed on the seven-segment display one character at a time at a set time interval of 2-3 seconds. At the end of the sequence, the string is repeated. Example: A Team No. 5 of section-1 will display "**CSE231-6-5**".

The sequential logic circuit produces a sequence of codes that are required to represent the string of characters "**CSE231-section no.-Group no"**. The sequential logic circuit is connected to an active high seven-segment display via a combinational logic circuit. The combinational logic circuit decodes the input codes from the sequential logic circuit in order to drive the individual segments of the seven-segment display to show each character `C', `S', 'E' `2','3' and `1' , `-' etc. as dictated by the sequence.

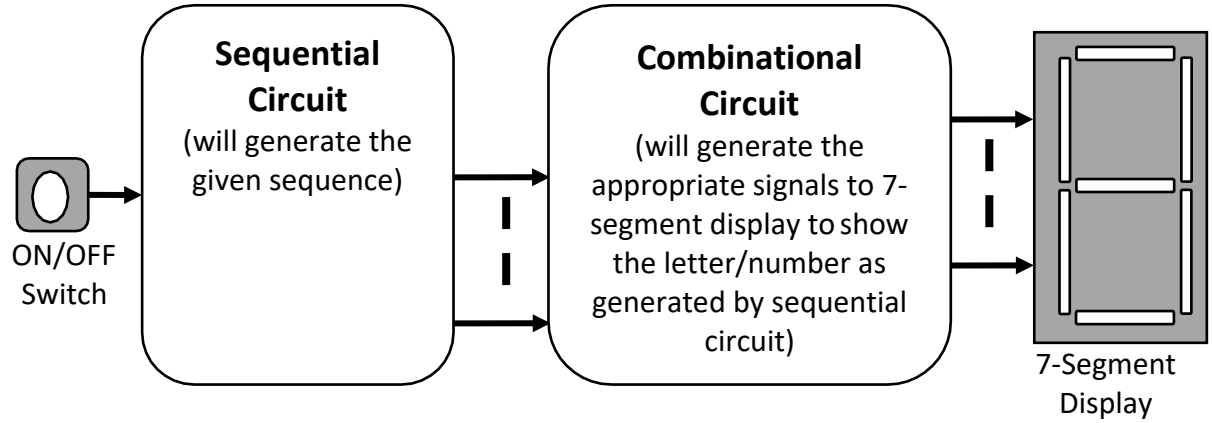

Fig. 1: Circuit block diagram. Sequential circuit produces a sequence of codes. Code from sequential circuit is decoded by combinational circuit to light up corresponding segments of a seven-segment display.

NOTE: Only ONE seven-segment display is to be used and the display will show one character at a time based on the sequence

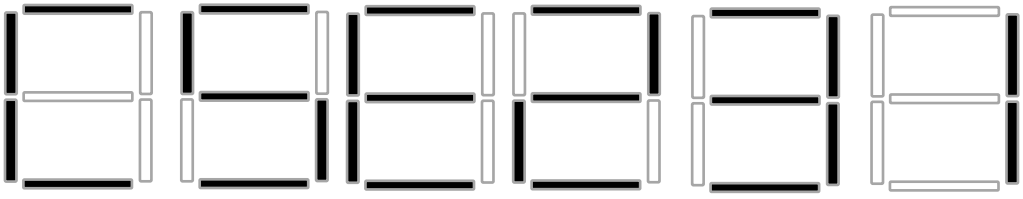

Fig.2: Display of "CSE231" by a seven-segment display.

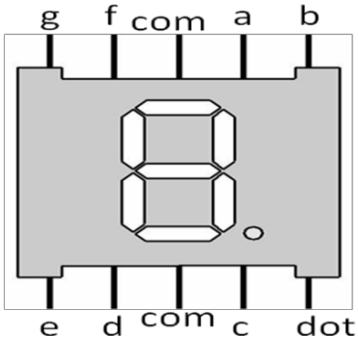

Fig. 3 shows the schematic of seven-segment display with its segments and corresponding input pins labelled (a - g). The COM ports are for V_{CC} and Gnd.

1. Objectives and Tasks

Phase 1: Combinational Circuit

Phase 1A: Combination circuit Design

Design the combinational logic part of the system described in Sec. 2, that is, the decoder to display the characters of the string "**CSE231-section no.-Group no"** on a seven-segment display. Groups can choose to do any one of the given sequences.

The team must complete design and working schematics of the combinational circuit only using **Logisim** and **submit a hard-copy and a soft-copy of it**, on or before the deadline, and during

the assigned office hours. The group must show the theoretical design steps of the circuits. The combinational circuit must be designed and implemented in the following forms:

a. 1st Canonical Form
b. Minimal logic implemented using universal gates (NAND, NOR)
c. Decoder
d. Multiplexer

It is at the discretion of the team to opt for their choice of design. However, the group must be able to provide rationale for their design choice and it must be using relevant material covered in the course. Think about number of bits, efficiency, complexity, etc.

Phase 1B: Combinational Circuit Implementation

The group must implement hardware and demonstrate the combinational circuit to display the required characters on a seven-segment display.

Phase 2: Sequential Circuit

Design the sequential logic part of the system described in Sec. 4, that is, the sequence generator for the string of characters "**CSE231-section no.-Group no"** in the correct order. Each character must be displayed for about 2-3 seconds. Groups can choose to do any one of the given sequences.

It is at the discretion of the team to opt for their choice of design. However, the team must be able to provide rationale for their design choice and it must be using relevant material covered in the course.

The team must complete design and working schematics of the sequential circuit only using **Logisim** and **submit a hard-copy** and a **soft-copy** of it, on or before the deadline, and during the assigned office hours. The group must show the theoretical design steps of the circuit and ensure its compatibility with the combinational circuit.

Phase 3: Final Submission

Students are required to implement their digital electronics circuit (combinational and sequential) and demonstrate its working before or on the Final deadline. The circuit should loop through the chosen sequence ("**CSE231-section no.-Group no"**) at the set interval automatically once the circuit is switched on.

Point Distribution

Task	Points
Phase 1A: Combination Design	25
Phase 1B: Combinational Implementation	25
Phase 2: Sequential Part Design	25
Phase 3: Final Implementation	25

Final marks will only be confirmed upon satisfactory completion of the project. Marks will be given at the discretion of the faculty member considering the group is capable of the work submitted based on their overall performance.

Final marks of the project will be distributed among group members based on the appraisal submitted by the Team Leader. Each member of a group will be assessed individually and his/her mark may vary from other group members based on assessment during the presentation and the appraisal.