LAB 5 REPORT

Name – Chirath A.A.I.

Index – 210086E

Lab Task – The objective of this lab to design a 3-bit counter, program it to count both clockwise and counterclockwise dependent on an external input and test its operation in simulation and on the development board.

Q_t			Button	Q_{t+1}			D_2	D_1	D_0
Q_2	Q_1	Q_0		Q_2	Q_1	Q_0			
0	0	0	0	0	0	1	0	0	1
0	0	0	1	1	0	0	1	0	0
0	0	1	0	0	1	1	0	1	1
0	0	1	1	0	0	0	0	0	0
0	1	0	0	x	x	x	x	x	x
0	1	0	1	x	x	x	x	x	x
0	1	1	0	1	1	1	1	1	1
0	1	1	1	0	0	1	0	0	1
1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1	1	0
1	0	1	0	x	x	x	x	x	x
1	0	1	1	x	x	x	x	x	x
1	1	0	0	1	0	0	1	0	0
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	0	1	1	0
1	1	1	1	0	1	1	0	1	1

- D_0

$Q_0.B$ / $Q_2.Q_1$	00	01	11	10
00	1			1
01	X	X	1	1
11		1	1	
10			X	X

$D_0 = Q_1.B + Q_2'.B'$

- D_1

$Q_0.B$ / $Q_2.Q_1$	00	01	11	10
00				1
01	X	X		1
11		1	1	1
10		1	X	X

$D_1 = Q_2.B + Q_0.B'$

- D_2

$Q_2.Q_1$ \ $Q_0.B$	00	01	11	10
00		1		
01	X	X		1
11	1	1		1
10		1	X	X

$D_2 = Q_1.B' + Q_0'.B$

- VHDL codes

D - Flip Flop

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity D_FF is
    Port ( D : in STD_LOGIC;
           Res : in STD_LOGIC;
           Clk : in STD_LOGIC;
           Q : out STD_LOGIC;
           Qbar : out STD_LOGIC);
end D_FF;

architecture Behavioral of D_FF is

begin

    process (Clk) begin
        if (rising_edge(Clk)) then
            if Res = '1' then
                Q <= '0';
                Qbar <= '1';
            else
                Q <= D;
                Qbar <= not D;
            end if;
        end if;
    end process;

end Behavioral;
```

Slow Clock

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx leaf cells in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity Slow_Clk is
    Port ( Clk_in : in STD_LOGIC;
           Clk_out : out STD_LOGIC);
end Slow_Clk;

architecture Behavioral of Slow_Clk is

signal count : integer := 1;
signal clk_status : std_logic :='0';

begin
    -- For 100 MHz input clock this genarates 1 Hz clock
    process (Clk_in) begin
        if (rising_edge(Clk_in)) then
            count <= count + 1;
            if (count = 5) then
                clk_status <= NOT clk_status;
                Clk_out <= clk_status;
                count <= 1;
            end if;
        end if;
    end process;

end Behavioral;
```

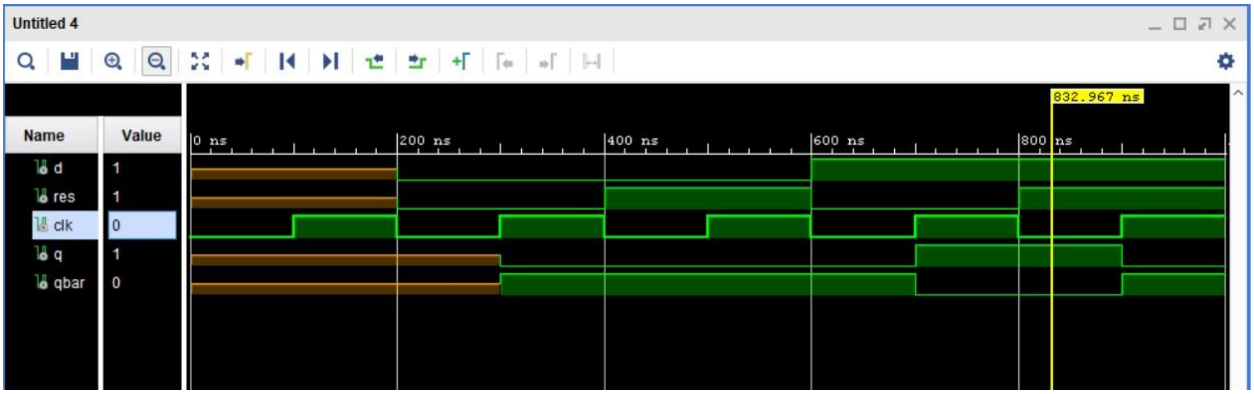
Counter

```
22  library IEEE;
23  use IEEE.STD_LOGIC_1164.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx leaf cells in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity Counter is
35      Port ( Dir : in STD_LOGIC;
36             Res : in STD_LOGIC;
37             Clk : in STD_LOGIC;
38             Q : out STD_LOGIC_VECTOR (2 downto 0));
39  end Counter;
40
41  architecture Behavioral of Counter is
42
43      component D_FF port(
44          D : in STD_LOGIC;
45          Res : in STD_LOGIC;
46          Clk : in STD_LOGIC;
47          Q : out STD_LOGIC;
48          Qbar : out STD_LOGIC);
49      end component;
50
51      component Slow_Clk port(
52              Clk_in : in STD_LOGIC;
53              Clk_out : out STD_LOGIC);
54          end component;
55
56  signal D0, D1, D2 : STD_LOGIC; -- Internal signals
57  signal Q0, Q1, Q2 : STD_LOGIC; -- Internal signals
58  signal Clk_slow : STD_LOGIC; -- Internal clock
59
```

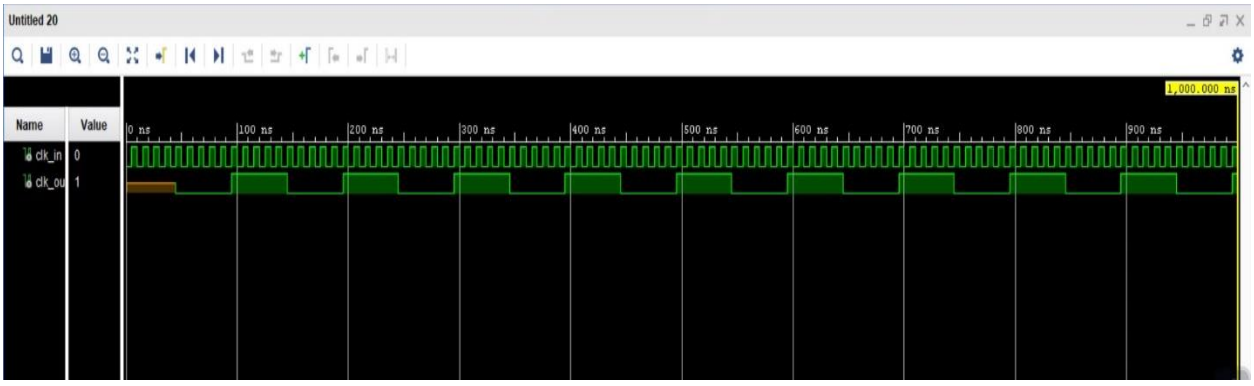
```
60  begin
61
62  Slow_Clk0 : Slow_Clk port map(
63      Clk_in => Clk,
64      Clk_out => Clk_slow);
65
66  D_FF0 : D_FF port map (
67      D => D0,
68      Res => Res,
69      Clk => Clk_slow,
70      Q => Q0);
71  D_FF1 : D_FF port map (
72      D => D1,
73      Res => Res,
74      Clk => Clk_slow,
75      Q => Q1);
76  D_FF2 : D_FF port map (
77      D => D2,
78      Res => Res,
79      Clk => Clk_slow,
80      Q => Q2);
81
82  D0 <= ((not Q2) and (not Dir)) or (Q1 and Dir);
83  D1 <= (Q0 and (not Dir)) or (Q2 and Dir);
84  D2 <= (Q1 and (not Dir)) or ((not Q0) and Dir);
85
86  Q(0) <= Q0;
87  Q(1) <= Q1;
88  Q(2) <= Q2;
89
90
91  end Behavioral;
```

- Timing Diagrams

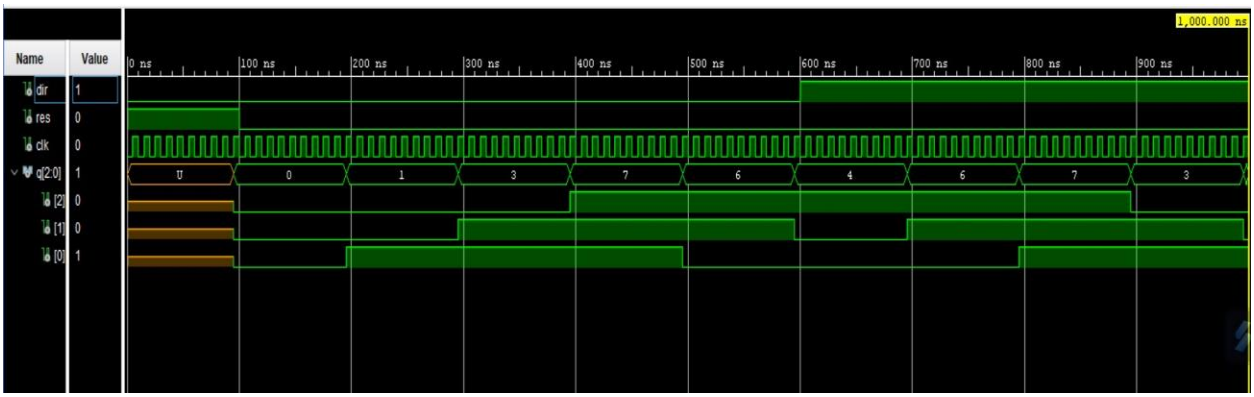
D - Flip Flop



Slow Clock



Counter



- Conclusion

  In conclusion D – Flip flop is a essential component of digital circuits that can store one bit of information and it's commonly use in counters. D – flip flop is an improved version of S-R Flip flop.
  On the other hand, counter is a digital circuit that sequentially count series of events and its made by series of D – Flip flops. In this lab we created a counter we can change the direction in this one using a switch. There are other type of counters and the all a used in many different scenarios.