

IBRAHIM RUPAWALA

3571 Lisbon Dr, San Jose, CA

Mobile: 480-284-9270 **Email:** ibrahimrupawala@gmail.com

Linkedin: <https://www.linkedin.com/in/irupawala/> **Github:** <https://github.com/irupawala>

EDUCATION

Master of Science, Electrical and Computer Engineering

Dec 2017

Arizona State University, Tempe, USA

Bachelor of Engineering, Electronics Engineering

May 2013

Gujarat Technological University, Gujarat, India

TECHNICAL SKILLS

Programming Languages: Python, C++

Database Technologies: Postgre SQL, MongoDB

Frameworks & Packages: Pandas, Numpy, Matplotlib, Scikit

Tools & Technologies: Visual Studio Code, Express, React, JIRA, Git, Jupyter Notebook, Matlab

Related Coursework: Data Structures and Algorithms, System Design, Computer Architecture, OOP Design, Operating Systems

WORK EXPERIENCE

Staff Engineer, Western Digital Technologies, Milpitas, CA

Jan 2018 – Present

- SSD System Features Development to optimize NAND Flash modes and perform memory management as per the customer specific requirements to improve system level performance and reliability.
- Responsible for developing device trims which involves device parameter adjustments to optimize the NAND flash device specifications (endurance, performance, power) as per the requirement of different internal and external business units.
- Performance and reliability test development to ensure the device specifications are met.
- Developed and automated test data collection, parsing, cleaning and visualization with Python.

Engineering Intern, Micron Technologies, Milpitas, CA

May 2017 - Dec 2017

- Developed memory diagnostic software tools. Design and implement automation for system level testing.
- Internal tools software development to verify and reproduce system software failure modes.
- Proactively create experiments and tooling to detect and diagnose hardware/software issues.

Graduate Teaching Assistant, Arizona State University, Tempe, AZ

Oct 2016 - May 2017

- Helped students in performing lab assignments using cadence environment for the course Analog & Digital Circuits.

IC Design Intern, Analog Rails, Tempe, AZ

May 2016 - Jul 2017

- Designed standard cell library and performed characterization of the cells. Performed RTL verification of the cells.
- Characterized standard cell library creating models for delay, constraints, and power that efficiently model cell behavior.

PROJECTS

- **MIPS R300 Microprocessor Design:** Designed and verified MIPS 5 stage pipelined microprocessor with Data Hazard Detection, Data Forwarding, Control Hazard Detection & Branch Delay Slot in System Verilog with an IPC of 0.90.
- **Advanced Shortest Paths Algorithms:** Implemented Contraction Hierarchies Algo that results in 1000 times faster query performance compared to Dijkstra's algo on graphs for road networks. Also Implemented Bidirectional Dijkstra, A-Star Algo's.
- **Phi X174 Genome Sequence Assembler:** Developed an assembler to recreate Genome Sequence from 100 nucleotides long 5386 error prone reads using Hamiltonian and Eulerian Path in Overlap Graph and DeBruijn Graph respectively.
- **Twitter Sentiments Analysis:** Trained Naive Bayes classifier Model to predict sentiment from thousands of Twitter tweets. Performed tokenization to tweet text using Scikit Learn. Performed data cleaning and removed punctuation and stop words.
- **Facial Expression Recognition using Keras:** Build and trained CNN in Keras from scratch to recognize facial expressions. The objective is to classify each face into one of seven categories (Angry, Disgust, Fear, Happy, Sad, Surprise, Neutral).

ACHIEVEMENTS

- Gold Medal for Consistent Academic Performance by Gujarat Technological University, India
- Merit based award for Outstanding Academic Performance by Ministry of HR Development, India
- Outstanding Teaching Assistant Award and Tuition fees waiver by Arizona State University, USA