Karthik Shivaram (He/Him) · 1st

Storage Engineer, SSD at Meta Platforms (Facebook)

- Meta
- New York University

San Jose, California, United States · Contact info

500+ connections

70 mutual connections: Ken Smith, Rimmi Amjad, and 68 others

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Highlights

You both worked at Micron Technology

Karthik worked at Micron Technology before you started

Say hello

About

Hardware and Product Development Engineer with extensive experience in Developing Solid-State Storage Solutions, SSD's in specific! Love solving problems!

Karthik Shivaram (He/Him)
Storage Engineer, SSD at Meta Platforms (Facebook)

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Specialties:
• Solid State Storage Design (SSDs)
• Firmware Validation
• Storage Protocols (SATA, SAS, SCSI, PCIe, NVMe...)
• x86 System Architecture
• Hardware Development
• Test Plan & Test Case Development
• Unit & Integration Testing
• Troubleshooting & Analytical Skills
• SSD/ Storage Component Qualification
• Linux/Unix programming
• Datacenter Hardware

Featured

Our team is hiring, we are looking for Interns for next summer (2022) in the areas of...

Platform Security Engineer Intern
facebook.com • 1 min read

29

Will be speaking at SNIA Storage D
Conference this year! Join me to lea

212 • 9 comments

Activity

2,263 followers

Awesome!
Karthik commented

Karthik Shivaram (He/Him)
Storage Engineer, SSD at Meta Platforms (Facebook)

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Sharing for more visibility, great opportunity to work and solve problems at-scale!

Karthik shared this
14 Reactions

Will be speaking at SNIA Storage Developers Conference this year! Join me to learn more about Boot Drives in Hyper-Scale!...

Karthik shared this
212 Reactions • 9 Comments

See all activity

Experience

Storage Engineer, SSD

Meta · Full-time
Feb 2018 – Present · 3 yrs 10 mos
Menlo Park, California

• Build SSD (Flash Solid State Drive) I/O infrastructure in many aspects, including, but not limited to, performance, cost, capacity, endurance, power efficiency, durability and data integrity.
• Collaborate with various cross-functional teams to develop specifications for SSDs to be incorporated in storage and compute servers. Understand requirements from different storage and compute application teams.
• Work closely with SSD and storage controller vendors to propose, develop, test and deploy technology optimized for Facebook server designs. Understand the underlying technologies of Solid State Disks (SSD).
• Evaluate various storage technology solutions, from hardware components and architecture to data transport protocols and topologies.
• Design and assist development of automatic infrastructure to allow all diagnosis of hardware faults and tools for inducing faults.
• Drive and lead the team to build up various suites and tools for productizing new hardware in Facebook Data Centers.
• Driving and standardizing SSD requirements in OCP.

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Karthik Shivaram (He/Him)
Storage Engineer, SSD at Meta Platforms (Facebook)

• Part of a team that developed the World's Fastest Enterprise SSDs based on Samsung V-NAND (3D-NAND)
• Managed a Test Development Team of 4 Engineers that worked on creating tests to verify some cool new features present in the latest Enterprise Class NVMe Drives made by Samsung
• Developed a good understanding of the NVMe specifications and lead validation of new features such as SR-IOV, Dual Port and Multiple Namespaces to name a few...
• Developed a sound understanding of the AGILE development flow and used Atlassian tools for multi-site (cross- functional) collaboration
• Used CTD (Combinatorial Testing) techniques in most validation projects
• Worked with test tool vendors and internal customers to improve and implement the support for new NVMe features and in-turn contribute to the development of the overall NVMe eco-system
• Evaluated new test tool vendors and qualified several new testing tools and improved Samsung's SSD validation strategies
• Helped in growing the team by participating in hiring for critical leadership roles
• Utilized the available budget and made judicious purchases to expand the test capacity and improve overall test infrastructure within Samsung's San Jose SSD test lab
• Partnered with cross functional teams across the globe within Samsung and helped in validation of next-gen SSD controller resulting in a successful tape out

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[Brochure] Samsung PM1725a NVMe SSD |...

Enterprise SSD - Flash Storage | Samsung...

Staff System Design Engineer

SanDisk
Jan 2013 – Sep 2015 · 2 yrs 9 mos
Milpitas, CA

System Design (System Design Engineer)

testing methods
• Improvised Architecture of FVT (Firmware Verification Test) - An Innovative Test Architecture Tool (Implemented in Python)
• Led the Firmware Validation and Created a Comprehensive Test-Plan to Verify Complex System Features
• Trained and Developed a team of 7 Engineers overseas and drove implementation of various requirements from Product Architecture to Validation Tools
• Employed CTD (Combinatorial Test Design) techniques to optimize Test Plans
• Performed Firmware Integration and Debugging of Regression Failures

Product Development (Sr. Product Design Engineer)
• Manufacturing Product & Process Development of SanDisk's first OEM Grade PCIe Client SSD
• PCIe Protocol Verification during the Hardware Bring-up of PCIe Test Platform
• Debugged & Verified Firmware Fixes by suitable Test Suites in a Manufacturing Environment
• Improved Manufacturing Yield & Reduced Test-Time on several occasions and successfully resolved product & tester related issues (in Asia) during all phases of SSD Manufacturing
• Successfully deployed several test-platforms into manufacturing facilities in SanDisk APAC
• Designer & Implementer of a "Secure Manufacturing Line" used in High-Volume Manufacturing of all SanDisk's Self-Encryption Drives
• Developed test-strategies and designed experiments to validate and replicate firmware related issues seen during Mass Production
• Mentored and built a support team in Asia by Conducting several "Tech-Talks" to explain Firmware Features and SSD Architecture of SanDisk Client SSDs
• Performed Failure Analysis of Line Rejects and root-caused NAND, Controller, Firmware, Data-Path related problems in the product and achieved resolution in a timely fashion

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SSD Systems Engineer (R&D)
Micron Technology
Dec 2010 – Dec 2012 · 2 yrs 1 mo
Boise, Idaho Area

• Firmware and Hardware Debugging with an overall understanding of System Architecture
• Root-Caused NAND Failures using Logic Analyzers and other Debug Tools
• Programmed and Built Test Firmware for System Performance & Quality Improvement Analysis
• Analyzed Hardware & Firmware Bugs and proposed changes to the Current System Architecture
• Developed a solid understanding of the FTL, Page Table Design, SSD Data-Path, Wear Leveling, Garbage Collection, Task Prioritization in an RTOS, NAND Interfacing, SSD Performance Optimization and Surprise Power Loss Protection Techniques
• Helped in developing products from Concept to High-Volume Manufacturing
• Worked closely with Customers & Application Engineers to understand their requirements and Design Experiments to Validate special requests
• Troubleshot & Resolved OEM Qualification Issues on Customer Site multiple times
• Understood Customer Requirements & translated them to realizable Technical Specifications and created Test Plans for these features
• Enhanced Debug Features of Future Generation Products
• Authored several White-Papers delivered to Tier-1 Enterprise OEM's
• Characterized Power and Performance for all types of SSDs (Client & Data-Center)
• Automated several tests using Perl, Python & DriveMaster
• Performed Firmware Validation of SATA products (White-Box & Black-Box) using DriveMaster
• Products Developed: Micron P410, P400e, P300 (SLC) and Micron "C" Series SSD's

(http://micron.com/products/solid-state-storage/enterprise-sata-ssd/p400e-enterprise-sata-ssd)

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Technical Associate (Part-Time)

Engineering Conferences International
Feb 2009 – Jun 2011 · 2 yrs 5 mos
New York, NY

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Hardware Design Engineer
Radiant Communications Corp.
Nov 2009 – Dec 2010 · 1 yr 2 mos
Massapequa, NY

• Designed & Implemented Agilent HDMP 1032/1034 functionality on Xilinx SPARTAN-6. Developed the RTL code in VHDL & simulated it on ModelSim. Finally, verified encoder & decoder functionality using VHDL Test Benches.
• Hardware & Firmware Debugging of DV-100 (A/V+Data Multiplexer over Fiber)

(http://www.rccfiber.com/products/product_gallery.htm)

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900 Series - Multiplex Solutions Over 1 or 2...

RF Test Engineer
Mini-Circuits Laboratory
Jun 2008 – Nov 2009 · 1 yr 6 mos
Brooklyn, NY

• Part of the Engineering Test Team as an Intern & Full-Time Team Member. Responsible for testing & analyzing the behavior of current generation & future RF/ Microwave Products Designed by MCL
• Involved in the characterization of RF-IC's, MMIC's and other Microwave components such as Power Splitters, Attenuators, Couplers etc.
• Also, involved in product validation by testing and analyzing microwave properties such as Loss, Coupling, Attenuation, Gain, Noise Figure, IP3, S-Parameters using ENA/PNA-X Network Analyzers, Signal Analyzers, Power Meters, High-Resolution Microscopes and other lab instruments.
• Underwent training in performing Failure Analysis of RF Components.

(http://www.minicircuits.com/pages/new_products.html)

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Electrical Engineer (Contract)

Board Schematics & preparing Bill-of-Materials (BOM) of Ultra-Sonic Sensors.
• Identified and resolved a critical timing issue in a FPGA based sensor.
• Redeveloped the micro-controller (C8051F120/17) firmware for LL-101 (Liquid Level Ultrasonic Sensor)

(http://cosense.com/products/point-level-liquid-level-sensors)

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Graduate Assistant
Polytechnic Institute of New York University
Jan 2008 – Jun 2008 · 6 mos
Brooklyn, NY

• Assisted the Engineering Conferences International (ECI) staff in the planning and execution of ECI conferences by performing administrative duties such as proofreading, data entry and documentation.

Intern
UTL Technologies
Dec 2006 – May 2007 · 6 mos
Bengaluru Area, India

• Interned at UTL Technologies and completed a Project in the area of Embedded System Design. As part of the internship, we built a prototype of an Infra-Red (IR) remote controller consisting of ATMEL & NXP 8051 controllers.
• Develop & Debug Firmware using MCS-51 Assembly (Intel x86)
• Schematic Entry & Documentation

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Show fewer experiences

Education

New York University
Master of Science, Electrical Engineering
2007 – 2008

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Research:

• "Design of Low-Power and Robust SRAM Memory Cell (65nm) (Reliability Aware Design)" - Low Power VLSI Custom Circuit Design using Cadence Design Tools

Design Projects:

• Implementation of BLAKE (SHA-3 Candidate for Next Generation Hash Function/ Submitted to NIST) - FPGA Design
• Remote Keyless Entry System - FPGA Design with Power Analysis (XPower) & On-Chip Debugging using ChipScope
• Design of Hardware Trojans (NYU-Poly "Cyber Security Awareness Week – 2008", Embedded System Challenge) - Advanced FPGA Design (VHDL & Verilog)/ Timing & Placement Constraints
• Hardware Design of Block Cipher (RC-5, 64-Bit) - Spartan3 FPGA Design
• 16-bit RISC Processor Design w/ Domino Logic (ASIC Design Flow) - VLSI CAD
• Implementation of TRIVIUM Stream Cipher - FPGA Design
• Design of Viterbi Decoder - VLSI Custom Circuit Design
• Performance Evaluation of Computer Systems - Capacity Planning
• Internet Architecture & Protocols Lab

Polytechnic University

Graduate Certificate, Computer Engineering
2007 – 2008
Activities and Societies: IEEE-Poly

FPGA & VLSI Design

Visvesvaraya Technological University

Bachelor of Engineering, Electronics & Communication, 73
2003 – 2007
Activities and Societies: • Member of the College Cricket Team • Student Member : Department of Electronics & Telecommunications • V.T.U - EduSAT • Event Cordinator: Annual College Cultural Fest (2006-07)

Senior Project Title "Design of Embedded System :