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IBRAHIM RUPAWALA

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SUMMARY

- Experienced professional with demonstrated history of working in semiconductor industry and masters in electronics and mixed signal circuit design seeking opportunity to contribute towards development of cutting-edge products.

EDUCATION

MS [Electrical & Electronics Eng]	Arizona State University, USA	GPA: 3.74/4	*Jan'16-Dec'17*
BE [Electronics Eng]	Gujarat Tech University, India	CGPA: 8.27/10	*Jul'09-May'13*

TECHNICAL SKILLS

- **Programming Languages:** C++ for test development, TCL for scripting, Python for Data Parsing and Visualization.
- **Hardware Description Languages:** Verilog, System Verilog
- **Tools:** Synopsys Design Compiler, VCS, PrimeTime, Hspice, Hercules, StarRC, Modelsim, WaveViewer, CosmoScope, Cadence HSPICE, ModelSim, Virtuoso, Spectre, Encounter, RTL Complier, Xilinx ISE, Vivado Design Suite, NCSim, System Generator, Matlab Simulink, Mentor Graphics Calibre, JMP, Spotfire
- **Tech Skills:** ASIC Design, Semiconductor Physics, Product Development, Statistical Analysis, Computer Architecture
- **Lab Tools:** Oscilloscope, Logic Analyzer, Multi-meter, Probe Station, ATE and SLT proprietary lab equipment's.

WORK EXPERIENCE

Staff Electronics Engineer, Western Digital, Milpitas, CA   *Jan' 2018 – Present*

- Responsible for all aspects of product bring-up, including early technology study, specifications negotiations, validation of new product features, test conditions and flow development. Characterization and debug of new silicon designs and process technologies. Optimization of test flows/methodologies for improved quality, test time reduction and cost.
- Performed post-silicon electrical and physical failure analyses to debug the device and identify the root cause for functional and parametric yield losses. Implemented changes as part of ECO (Engr Change Order) for bugs and improvement items.
- Involved in various aspects of memory chip design, focusing on Micro Architecture to deliver target power, area and performance goals. Performed feasibility studies at beginning of design phase for new architecture & features.
- Validated and optimized multiple design and device modes using lab tools to ensure the functionality and product specifications like power consumption, performance, energy per bit, bit error rate, etc are met.
- Designed multiple trims to optimize device specifications (endurance, performance, power) as per the requirement of business units. Developed tests, patterns/vectors, timing, and diagnostics on company's proprietary ATE's.
- Developed multiple screens and monitors to ensure the health of the dies and meet the yield criteria (DPPM).
- Debugging issues, weak points, or potential improvement areas related to any portion of the System Level Tests (SLT's) to help facilitate system features and to improve system level performance and reliability to meet customer specifications.

Product Engineering Intern, Micron Technology, Milpitas, CA   *May' 2017 – Dec' 2017*

- Optimized the erase/program/read timings and voltages parameters to configure the power and performance of the chip.
- Designed silicon test plan and correlated silicon to simulation data. Performed post-silicon validation to validate design.
- Design of Experiments (DOE) to collect data using company's proprietary ATE's to provide estimation for product life, performance, reliability and to predict failure modes. Documented results and communicated to respective stake holders.
- Developed scripts to automate characterization, verification and simulation flows and reduce the test time.
- Documented the design specifications, behavioral description, and timing diagrams.

Graduate Teaching Assistant, Arizona State University, Tempe, AZ   *Oct' 2016 – May' 2017*

- Helped students in performing lab assignments using cadence environment for the course Analog & Digital Circuits.

IC Design Intern, Analog Rails, Tempe, AZ   *May' 2016 – Jul' 2016*

- Designed standard cell library and performed characterization of the cells. Performed RTL verification of the cells.
- Characterized standard cell library creating models for delay, function, constraints and power that efficiently model cell behavior. Developed the Layout of standard cells in 45 nm PDK and performed DRC and LVS checks.

ACADEMIC PROJECTS

MIPS R3000 5 Stage pipelined microprocessor with Data Forwarding & Branch Delay Slot

- Designed and verified MIPS R3000 core with Data Hazard Detection, Data Forwarding, Control Hazard Detection & Branch Delay Slot in System Verilog with an IPC of 0.90. Implemented Parameterized Sequential Multiplier & Divider

RTL to GDS II Design of Lightweight Encryption ("Simon") Engine using 7nm (FINFET) PDK

- Designed a Verilog RTL behavioral netlist for the generation of 32 bit cipher text using 32 bit plain text and 64 bit key.
- Created Layout of the entire cipher using Cadence Encounter. Verified the geometry and connectivity ensuring no setup and hold violations are obtained. Extracted power of entire circuit using Synopsys Primetime Static Timing Analysis.

AWARDS & RECOGNITION

- Promotions, SanDisk High5 Awards, MVP Award and Exceptional Impact Award for various projects at Western Digital.
- Certificate of Recognition for excellent contributions and achieving remarkable milestone at Micron Inc.
- Outstanding Teaching Assistant Award & Tuition Fees Waiver at Arizona State University.
- Gold Medal & Merit based Scholarship for Consistent Academic Performance by Gujarat Technological University.