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Sr. Silicon Design Engineer

Locations: San Jose, California

Categories: Engineering

Req ID: 27995

Hiring Target Min: USD \$120,160.00/Yr.

Hiring Target Max: USD \$180,240.00/Yr.



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Job Description

WHAT YOU DO AT AMD CHANGES EVERYTHING

We care deeply about transforming lives with AMD technology to enrich our industry, our communities, and the world. Our mission is to build great products that accelerate next-generation computing experiences – the building blocks for the data center, artificial intelligence, PCs, gaming and embedded. Underpinning our mission is the AMD culture. We push the limits of innovation to

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solve the world's most important challenges. We strive for execution excellence while being direct, humble, collaborative, and inclusive of diverse perspectives. This is who we are at our best. One Company. One Team.

AMD together we advance_

SENIOR SILICON DESIGN ENGINEER

THE ROLE:

We are looking for an adaptive, self-motivated design verification engineer to join our growing team. As a key contributor, you will be part of a leading team to drive and improve AMD's abilities to deliver the highest quality, industry-leading technologies to market. The Verification Engineering team furthers and encourages continuous technical innovation to showcase successes as well as facilitate continuous career development.

THE PERSON:

You have a passion for modern, complex processor architecture, digital design, and verification in general. You are a team player who has excellent communication skills and experience collaborating with other engineers located in different sites/timezones. You have strong analytical and problem-solving skills and are willing to learn and ready to take on problems.

KEY RESPONSIBILITIES:

- As a member of the PCIe and Serial Connectivity Team you will work on next generation PCIe / CXL and connectivity solutions to enable data center applications and fuel the data center transformation. Join us in creating leading edge PCIe / CXL technology to shape the future of data processing and cloud technologies. Some of the key responsibilities would be:
- Execute on RTL design and coding for various sections of the SOC.
- Collaborate with a team of hardware and software engineers to define the high-level architecture.
- Participate in the definition of microarchitecture of next-generation high-performance PCIe/CXL connectivity solutions.
- Contribute to silicon debug and product support as needed.

PREFERRED EXPERIENCE:

- Relevant and proven experience of RTL design, Verilog and SystemVerilog
- Deep knowledge of front-end tools (Verilog simulators, linters, clock-domain crossing checkers)
- Validated experience with synthesis, static timing, DFT, is a plus

- Exposure to physical design and verification methods
- Knowledge of high-speed interfaces including, PCIe, CXL, Ethernet, DDR3/4/5, LPDDR3/4, HBM
- Experience with scripting languages including Perl, Python, Unix shells and Makefiles
- Strong communication, collaboration and presentation skills

ACADEMIC CREDENTIALS:

- Bachelors or Masters degree in computer engineering/Electrical Engineering

LOCATION:

San Jose, CA, USA

COMPENSATION:

Expected to range from \$100,100 to \$185,900 commensurate with experience and specific skill sets

#LI-NM1

At AMD, your base pay is one part of your total rewards package. Your base pay will depend on where your skills, qualifications, experience, and location fit into the hiring range for the position. You may be eligible for incentives based upon your role such as either an annual bonus or sales incentive. Many AMD employees have the opportunity to own shares of AMD stock, as well as a discount when purchasing AMD stock if voluntarily participating in AMD's Employee Stock Purchase Plan. You'll also be eligible for competitive benefits described in more detail here (<https://amd.jibeapply.com/benefits>).

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