





















MTS Silicon Design Engineer

AMD Santa Clara, CA (On-site) 1 week ago 40 applicants

\$138,400/yr - \$207,600/yr · Full-time · Mid-Senior level

10,001+ employees · Semiconductor Manufacturing

31 connections · 71 company alumni · 11 school alumni

Skills: Application-Specific Integrated Circuits (ASIC), RTL Design, +8 more

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Meet the hiring team



Patrick Harrington 2nd
Talent Acquisition Partner at AMD
Job poster

31 mutual connections

Message

About the job

WHAT YOU DO AT AMD CHANGES EVERYTHING

We care deeply about transforming lives with AMD technology to enrich our industry, our communities, and the world. Our mission is to build great products that accelerate next-generation computing experiences – the building blocks for the data center, artificial intelligence, PCs, gaming and embedded. Underpinning our mission is the AMD culture. We push the limits of innovation to solve the world's most important challenges. We strive for execution excellence while being direct, humble, collaborative, and inclusive of diverse perspectives. This is who we are at our best. One Company. One Team.

AMD together we advance_

PHYSICAL DESIGN ENGINEER - 069

The Role

The focus of this role is to drive Physical design of critical Graphics blocks on latest architectures, and achieve PPA by exploring improvements to RTL and Physical design methodologies.

THE PERSON:

You have a passion for pushing PPA on latest technology nodes and for Physical Design in general. You are a team player who has excellent communication skills and experience collaborating with other engineers located in different sites/timezones. You have strong analytical and problem-solving skills and are willing to learn and ready to take on problems.

KEY RESPONSIBILITIES:

• Own Physical design and PPA attainment for critical Graphics blocks

- Tasks to include RTL Synthesis, Placement, Clock tree synthesis, Optimization, Routing, Parasitic Extraction, Static Timing Analysis, IR drop analysis, Physical Verification and Sign Off
- Work closely with RTL designers to analyze critical bottlenecks that impact PPA.
- · Identify complex technical problems, break them down, summarize multiple possible solutions, and lead the team in the right direction
- Drive and hands-on flow development and scripting
- Technical lead of three to five senior level engineers

PREFERRED EXPERIENCE:

- Over 6 years experience with MSEE or MSCE in ASIC Physical Design from RTL to GDSII
- · Excellent analytical and problem solving skills along with attention to details
- Strong background in RTL analysis, Timing and Physical Design closure.
- Hands on experience in taping out 7nm, 10nm, 16nm, 28nm, 32nm, and/or 40nm SOCs
- · Working experience on CAD tools from Synopsys, Cadence and Mentor Graphics
- Strong communication, Time Management, and Presentation Skills
- Must be a self-starter, and be able to independently and efficiently drive tasks to completion
- · Ability to provide mentorship and guidance to junior and senior engineers, and be an effective team player

ACADEMIC CREDENTIALS:

• Bachelors or Masters degree in computer engineering/Electrical Engineering

At AMD, your base pay is one part of your total rewards package. Your base pay will depend on where your skills, qualifications, experience, and location fit into the hiring range for the position. You may be eligible for incentives based upon your role such as either an annual bonus or sales incentive. Many AMD employees have the opportunity to own shares of AMD stock, as well as a discount when purchasing AMD stock if voluntarily participating in AMD's Employee Stock Purchase Plan. You'll also be eligible for competitive benefits described in more detail here.

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Pay range in Santa Clara, CA

Exact compensation may vary based on skills, experience, and location.

Base salary

\$138,400/yr - \$207,600/yr

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To maximize your chances of getting this job, be sure to update your profile with the most relevant skills Most common applicant skills You have 5 out of the 10 most common skills among all other applicants MATLAB C (Programming Language) **⊘** Very-Large-Scale Integration (VLSI) **⊘** Python (Programming Language) Verilog Cadence Virtuoso **▼** Field-Programmable Gate Arrays (FPGA) Application-Specific Integrated Circuits (ASIC) VHDL Applicant seniority level 24 Entry level applicants 9 Senior level applicants Applicant education level have a Master's Degree (Similar to you) have a Bachelor's Degree 13% have a Doctor of Philosophy have other degrees

Applicants are in these locations

10-15 applicants ✓

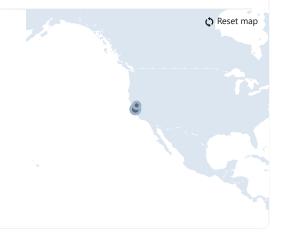
San Francisco Bay Area

1-5 applicants

Greater Sacramento

1-5 applicants

New York City Metropolitan Area



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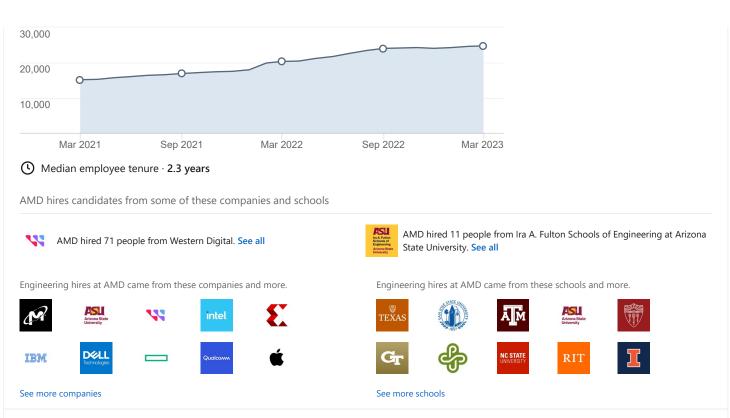
24,763

Total employees

▲ 63%

Company-wide 2 year growth ▲ 47%

Engineering 2 year growth 0



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About the company



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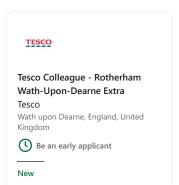
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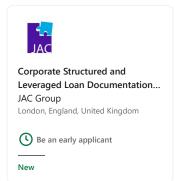
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