

SUMMARY

- Dedicated Storage Industry Professional with master's in electrical engineering seeking new and exciting opportunities

EDUCATION

- |                                     |                                |               |               |
|-------------------------------------|--------------------------------|---------------|---------------|
| • MS [Electrical & Electronics Eng] | Arizona State University, USA  | GPA: 3.74/4   | Jan'16-Dec'17 |
| • BE [Electronics Eng]              | Gujarat Tech University, India | CGPA: 8.27/10 | Jul'09-May'13 |

TOOLS AND TECHNOLOGIES

- **Programming Languages:** C++ for test development, Python for Data Analysis, Parsing & Plotting
- **Databases:** MySQL, PostgreSQL
- **EDA/Simulation Tools:** Cadence (Virtuoso, Spectre), Synopsys (Hspice, PrimeTime, WaveViewer, CosmoScope)
- **Lab Tools:** Oscilloscope, Parametric Analyzer, Memory Testers & Probe – Station, In-house Memory/SSD testers.
- **Relevant Coursework:** Semiconductor Memory Technologies & Systems, VLSI Systems & Circuits, VLSI Design, Computer Architecture, Constructionist Approach to Microprocessor design, Advanced Analog Integrated Circuits.

TECHNICAL SKILLS

- SSD System features development, SSD Qualification, PCIe, NVMe, SATA interface protocol, NAND algorithm development, Design validation & debugging, Statistical yield analysis, Failure analysis, Scripting & Data analysis

WORK EXPERIENCE

**Staff Engineer, Western Digital, Milpitas, CA** *Jan' 2018 – Present*

- System's features development for ESS (Enterprise Storage Systems) SSD to improve system level performance and reliability thus delivering the customer specific demands.
- Defining, developing, executing and automating NAND flash SSD memory reliability test, Design of experiments to qualify device as per different customer's requirements and industry standards like JEDEC.
- Interface with external vendors and internal systems, design, product, firmware engineers to understand system architecture to develop and execute the test suites for different features required by specific business units.
- Responsible for developing device trims which involves device parameter adjustments to optimize the device specifications (endurance, performance, power) as per the requirement of different internal and external business units.
- Owner of dynamic trim table, which ensures that the specifications of device is met throughout the life for the high endurance enterprise storage SSD products.
- Collaborating with Memory health and Product Engineering teams to ensure that the yield criteria of the device are met and responsible to develop screens and monitors for reducing defects (DPPM).
- NAND flash SSD memory failure analysis, root cause analysis and design debugging.
- Participation in specifications negotiations to push the power and performance envelope of the memory while ensuring the specifications and schedule requirements.
- Collaborating with Process Integration and technology development teams to address flash cell array deficiencies due to process changes during the development phase of new technology.
- Employ data analytical skills for high volume data analysis by writing scripts in python.

**Non-Volatile Engineering Product Intern, Micron Technology, Milpitas, CA** *May' 2017 – Dec'2017*

- Power and performance optimizations of program and read algorithm of Micron's 64 tier TLC NAND Flash SSD.
- Optimized the program and read algorithm by modulating the trims to find the best settings which enables to configure the device in the best performance, least power consumption and least energy per bit modes.
- Proactively create experiments and tooling to detect and diagnose hardware/firmware/software health issues.
- Performed post - silicon validation of Micron's 3D NAND flash using memory tester & probe - station.
- Analyzed test data collected to provide estimations for product life, reliability and predict failure modes

**Graduate Teaching Assistant, Arizona State University, Tempe, AZ** *Oct' 2016 – May' 2017*

- Helped students in performing lab assignments using cadence environment for the course Analog & Digital Circuits.

**IC Design Intern, Analog Rails, Tempe, AZ** *May' 2016 – Jul' 2016*

- Designed standard cell library and performed characterization of the cells. Performed RTL verification of the cells.
- Characterized standard cell library creating models for delay, function, constraints and power that efficiently model cell behavior. Developed the Layout of standard cells in 45 nm PDK and performed DRC and LVS checks.

ACADEMIC PROJECTS

- MIPS R3000 5 Stage pipelined microprocessor with Data Forwarding & Branch Delay Slot
- RTL to GDS II Design of Lightweight Encryption ("Simon") Engine