Ibrahim Rupawala

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Summary

Sr Engineer working on cutting edge 3D NAND Flash Non-Volatile Memory

Technical Skills:

--> Digital Logic Design, FPGA/ASIC Design, RTL Design, Physical Design, Verification
--> Static Timing Analysis (STA), Dynamic Timing Analysis (DTA), Setup time, Hold time.
--> VCS functional simulation, gate level simulation, RTL simulation.
--> Synthesis, Floor-planning, Place & route, Clock distribution
--> UVM verification (basics), Constrained random testing.
--> System Verilog assertion-based verification & Functional coverage.

* Programming Languages:
C++, Java for test dev,TCL, Perl for scripting, Python for Data Analysis & Visualization.

* Hardware Description Languages:
Verilog, System Verilog, UVM (basics).

* EDA/Simulation Tools:
Cadence (Virtuoso, Encounter (Floor-planning, Place & route, Clock distribution), Spectre,RC Complier), Synopsys (PrimeTime, HSPICE, Hercules, Star RC, Design Compiler, VCS), Xilinx (ISE, VivadoDesign Suite), Matlab (Simulink), Mentor Graphics (Calibre, Modelsim), Gem5 processor simulator.

* Lab Tools:
Oscilloscope, Probe-Station & Memory Testers

Related Coursework:
VLSI Design, System Verilog Verification, Hardware Acceleration & FPGA, Computer Architecture, Digital Systems & Circuits, Constructionist approach to microprocessor design, Semiconductor Memory Technology.

Experience

Staff Software Engineer
Western Digital
Feb 2018 - Present (4 years 4 months +)

Non Volatile Engineering Product Intern
Micron Technology
May 2017 - Dec 2017 (8 months)

Graduate Teaching Assistant
Arizona State University
Oct 2016 - May 2017 (8 months)

Graduate Service Assistant
Arizona State University
Aug 2016 - Dec 2016 (5 months)

Design Intern
Analog Rails
May 2016 - Oct 2016 (6 months)

Technical Engineer
Jun 2013 - May 2015 (2 years)
Technical Support for the various products manufactured and sold by company. Collaborating with the Research and Development Team and Sales & Marketing team to design electrical accessories according to the need of the clients.

Engineering Trainee
Bharat Sanchar Nigam Limited
Jun 2012 - Jul 2012 (2 months)
Underwent Industrial Training in GSM technology at BSNL (Largest Telecom Service Provider in India). Understanding the concepts of CDMA, GSM, network architecture, communication channel, cell division, call processing, PCM principles & multiplexing of telecommunication signals, fibre optic communication technologies and packet switching technologies.Practical experience on how the telephone exchange works.

Education

Ira A. Fulton Schools of Engineering at Arizona State University
Master's Degree, Electrical and Electronics Engineering
2016 - 2018
Electrical and Electronics Engineering Graduate student with focus on Electronics and Mixed Signal Circuit Design

Gujarat Technological University, Ahmedbabd
Bachelor's Degree, Electronics Engineering
2009 - 2013

Licenses & Certifications

Complete Python Bootcamp: Go from zero to hero in Python 3 - Udemy
UC-3P86STCV

Learn C++ Programming -Beginner to Advance- Deep Dive in C++ - Udemy
UC-FLMCSEOF

The Complete SQL Bootcamp - Udemy
UC-ND0DQXPE

Data Structures and Algorithms Specialization - Coursera
9FJ7UTUPLTKE

Skills

Cadence Virtuoso • Cadence Encounter • Digital Circuit Design • Analog Circuit Design • Digital Electronics • TCP/IP • CMOS • FINFET • VLSI • Electrical Engineering

Honors & Awards

Gold Medal for consistent performance in academics - Gujarat Technological University
Mar 2013

Merit Based Award - Ministry of Human Resource Development, India
Nov 2012