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IBRAHIM RUPAWALA

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SUMMARY

- Dedicated Engineering Professional with masters in Electronics and Mixed Signal Circuit Design seeking to leverage my skills at an industry-leading firm.

EDUCATION

• MS [Electrical & Electronics Eng]	Arizona State University, USA	GPA: 3.74/4	***Jan'16-Dec'17***
• BE [Electronics Eng]	Gujarat Tech University, India	CGPA: 8.27/10	***Jul'09-May'13***

TECHNICAL SKILLS

- **Programming Languages:** C++ for test development, for Data Analysis, Parsing & Plotting
- **Hardware Description Languages:** Verilog, System Verilog
- **EDA/Simulation Tools:** Cadence (Virtuoso, Spectre, Encounter, RTL Complier), Synopsys (Hspice, Hercules, StarRC, PrimeTime, Modelsim, WaveViewer, CosmoScope), Xilinx (ISE, Vivado Design Suite, System Generator)
- **Other Tools:** Matlab (Simulink), SanDisk's In-house Memory testers
- **Lab Tools:** Oscilloscope, Parametric Analyzer, Memory Testers & Probe - Station.
- **Technical Skills:** Flash Memory & CMOS, SSD Development, PCIe, NVMe, Scripting & Data Analysis
- **Related Coursework:** Semiconductor Memory Technologies & Systems, Digital Systems & Circuits, VLSI Design, Computer Architecture, Advanced Analog Integrated Circuits, Advanced Silicon Processing.

WORK EXPERIENCE

Staff Device Engineer, R & D Engineering, Western Digital, Milpitas, CA ***Jan' 2018 – Present***

- Responsible for developing trims which involves NAND parameter adjustments to optimize the NAND device specifications (endurance, performance, power) as per the requirement of different internal and external business units.
- Owner of dynamic trim table, which ensures that the specifications of NAND device is met throughout the life for the high endurance enterprise storage SSD products.
- Defining, developing, executing and automating NAND flash memory reliability test, Design of experiments to qualify NAND as per different customer's requirements and industry standards.
- Accountable for providing feedbacks to ESS (Enterprise Storage Systems) SSD team system's request to design and develop system device features to improve system level performance and reliability.
- Collaborating with Memory health and Product Engineering teams to ensure that the yield criteria of the device are met and responsible to develop screens and monitors for reducing NAND defects (DPPM).
- NAND/ SSD characterization, qualification, and failure analysis for product yield improvement.
- Drive System Countermeasures with Firmware Teams to prevent residual failure exposure for the customer.
- Participation in specifications negotiations with system teams to push the power and performance envelope of the NAND while ensuring the specifications and schedule requirements.
- Collaborating with Process Integration and technology development teams to address NAND cell array deficiencies due to process changes during the development phase of new technology.
- Employ data analytical skills for high volume data analysis. Develop new Design for Test as a solution to new challenges.

Non-Volatile Engineering Product Intern, Micron Technology, Milpitas, CA ***May' 2017 – Dec'2017***

- Power and performance optimizations of program and read algorithm of Micron's 64 tier TLC NAND Flash.
- Optimized the program and read algorithm by modulating the trims to find the best settings which enables to configure the device in the best performance, least power consumption and least energy per bit modes.
- Performed post - silicon validation of Micron's 3D NAND flash using memory tester & probe - station.
- Analyzed test data collected to provide estimations for product life, reliability and predict failure modes

Graduate Teaching Assistant, Arizona State University, Tempe, AZ ***Oct' 2016 – May' 2017***

- Helped students in performing lab assignments using cadence environment for the course Analog & Digital Circuits.

IC Design Intern, Analog Rails, Tempe, AZ ***May' 2016 – Jul' 2016***

- Designed standard cell library and performed characterization of the cells. Performed RTL verification of the cells.
- Characterized standard cell library creating models for delay, function, constraints and power that efficiently model cell behavior. Developed the Layout of standard cells in 45 nm PDK and performed DRC and LVS checks.

ACADEMIC PROJECTS

MIPS R3000 5 Stage pipelined microprocessor with Data Forwarding & Branch Delay Slot *(System Verilog, Perl)*

- Designed and verified MIPS R3000 core with Data Hazard Detection, Data Forwarding, Control Hazard Detection & Branch Delay Slot in System Verilog with an IPC of 0.90.
- Implemented Parameterized Sequential Multiplier & Sequential Divider using Genesis2

RTL to GDS II Design of Lightweight Encryption ("Simon") Engine *(Verilog, APR)*

- Designed a Verilog RTL behavioral netlist for the generation of 32 bit cipher text using 32 bit plain text and 64 bit key, also designed netlist for the generation of 64 bit key for encrypting 32 bit plaintext during each round.
- Created Layout of the entire cipher using Cadence Encounter. Verified the geometry and connectivity ensuring no setup and hold violations are obtained. Extracted power of entire circuit using Synopsys Primetime Static Timing Analysis.