

PROPOSAL

1. Project title, group number on Blackboard, names of group members
 - Project Title: Hardware Accelerator for Dijkstra Algorithm
 - Group Number on Blackboard: Project Team 3
 - Name of Group Members: 1. Saranya Govinda Raj 2. Ibrahim Rupawala 3. Vijayan Ramesh

2. Problem description and prior work (cite references)

- What is the algorithm to be implemented?
Dijkstra Algorithm
- What are the target applications?

The problem of finding the shortest spanning tree between a pair of graph nodes is often solved using Dijkstra's algorithm. The algorithm finds offline and real time applications in various areas such as path planning in mobile robots, telecom networks and segmentation in image processing.

- Why is a hardware accelerator needed for the target applications? What are the limitations of software solutions? Or existing hardware solutions if any?

Dijkstra's algorithm in software is implemented largely with the help of a priority queue, which is a sequential data structure. As the number of nodes in a network increase, the advantages of parallelizing this queue become apparent, given the quadratic growth of the algorithm. We wanted to exploit this and implement an efficient parallel version of the Algorithm on reconfigurable hardware.

3. Proposed work and expected deliverables (be realistic - you have about 7 weeks!)

- What is your implementation target? FPGA, ASIC, or both?
We are expecting to implement the design on both 28nm ASIC target (and W, Vth, VDD optimization) and Xilinx Virtex 7 FPGA target which best needs the design requirements
- What are your design specifications? e.g. target throughput, power, energy efficiency, etc.
The algorithm is designed for the applications where the time required to converge between two points is crucial. Hence the primary focus on designing the accelerator will be to improve the execution time
- If successful, what difference will your design make to the target applications?
The motivation for the project presented here originates from the routing problem in VLSI design, mobile robots, telecom networks and segmentation in image processing where the time needed to complete the full design process is one of the most crucial issues to be addressed. If implemented this design will exacerbate all these applications

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4. References

- https://en.wikipedia.org/wiki/Dijkstra's_algorithm
- <http://www.geeksforgeeks.org/greedy-algorithms-set-6-dijkstras-shortest-path-algorithm/>
- <http://www3.cs.stonybrook.edu/~skiena/combinatorica/animations/dijkstra.html>
- <https://brilliant.org/wiki/dijkstras-short-path-finder/>
- <http://ieeexplore.ieee.org/document/6269416/> -- -- Research of shortest path algorithm based on the data structure
- I. Fernandez, J. Castillo, C. Pedraza, C. Sanchez, J. Ignacio Martinez, “Parallel Implementation of The Shortest Path Algorithm on FPGA”, 2008 4th Southern Conference on Programmable Logic, pp.245-248, 26-28 March 2008.
- K. Sridharan, T. K. Priya, P. R. Kumar, “Hardware Architecture for Finding Shortest Paths”, TENCON 2009 - 2009 IEEE Region 10 Conference, pp.1-5, 23-26 Jan. 2009.
- G.R. Jagadeesh, T. Srikanthan, C.M. Lim “Field programmable gate array-based acceleration of shortest-path computation”, IET Comput. Digit. Tech., 2011, Vol. 5, Iss. 4, pp. 231–237.
- E. W. Dijkstra, “A note on two problems in connection with graphs”, Numerische Mathematik, vol.1.1, pp.269–271, 1959