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IBRAHIM RUPAWALA

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SUMMARY

- Experienced and dedicated electronics engineer with a demonstrated history of working in the semiconductor industry seeking exciting and challenging opportunity to contribute towards development of cutting-edge products.

EDUCATION

- MS [Electrical & Electronics Eng]   Arizona State University, USA   GPA: 3.74/4   *Jan'16-Dec'17*
- BE [Electronics Eng]   Gujarat Tech University, India   CGPA: 8.27/10   *Jul'09-May'13*

TECHNICAL SKILLS

- **Programming Languages:** C/C++, Python, TCL, Perl
- **Hardware Description Languages:** Verilog, System Verilog
- **Tools:** Synopsys Design Compiler, VCS, PrimeTime, Hspice, Hercules, StarRC, Modelsim, WaveViewer, CosmoScope, Cadence HSPICE, ModelSim, Virtuoso, Spectre, Encounter, RTL Complier, Xilinx ISE, Vivado Design Suite, NCSim, System Generator, Matlab Simulink, Mentor Graphics Calibre, Ascent Lint, Meridian CDC, Spyglass Lint, Spyglass CDC
- **Tech Skills:** ASIC, Computer Architecture, Static Timing Analysis, Memory Standards, Object Oriented Programming
- **Lab Tools:** Oscilloscope, Logic Analyzer, Multi-meter, Probe Station, Wafer and chip testers.

WORK EXPERIENCE

Staff Electronics Engineer, Western Digital, Milpitas, CA   *Jan' 2018 – Present*

- Responsible towards various aspects of 3D NAND flash memory chip design, focusing on Micro Architecture, RTL, Logic synthesis, gate level simulation and equivalence checking to deliver target power, performance and area goals.
- Performed feasibility studies at the beginning of design phase for new architecture and features.
- Performed post-silicon electrical and physical failure analyses to debug the design and identify the root cause for functional and parametric yield losses reported by external and internal product lines using lab tools.
- Implemented changes as part of ECO (Engr Change Order) for bugs and improvement items in synthesized modules.
- Validated and optimized multiple design and device modes using company's proprietary tools to ensure the functionality and product specifications like power consumption, performance, energy per bit, bit error rate, etc are met.
- Worked on Modelling the NAND Flash Memory Core using C++, systemC and company's proprietary tools.
- Developed and qualified multiple trims which involves die parameter tuning to optimize the NAND Flash device specifications (endurance, performance, power) as per the JEDEC memory standards and requirement of business units.
- Developed multiple screens and monitors to ensure the health of the dies and meet the yield criteria (DPPM).
- Accountable for checking system level features on design and providing feedbacks to system team to help facilitate system features and to improve system level performance and reliability to meet customer specifications.

Product Engineering Intern, Micron Technology, Milpitas, CA   *May' 2017 – Dec' 2017*

- Power, Performance and Area Optimization of the flash memory chips to configure the chip towards the product criteria.
- Designed silicon test plan and correlated silicon to simulation data. Performed post-silicon validation to validate design.
- Design of Experiments (DOE) to collect data using company's proprietary tools to provide estimation for product life, performance, reliability and to predict failure modes. Documented results and communicated to respective stake holders.
- Documented the design specifications, behavioral description, and timing diagrams.

Graduate Teaching Assistant, Arizona State University, Tempe, AZ   *Oct' 2016 – May' 2017*

- Helped students in performing lab assignments using cadence environment for the course Analog & Digital Circuits.

IC Design Intern, Analog Rails, Tempe, AZ   *May' 2016 – Jul' 2016*

- Designed standard cell library and performed characterization of the cells. Performed RTL verification of the cells.
- Characterized standard cell library creating models for delay, function, constraints and power that efficiently model cell behavior. Developed the Layout of standard cells in 45 nm PDK and performed DRC and LVS checks.

ACADEMIC PROJECTS

MIPS R3000 5 Stage pipelined microprocessor with Data Forwarding & Branch Delay Slot

- Designed and verified MIPS R3000 core with Data Hazard Detection, Data Forwarding, Control Hazard Detection & Branch Delay Slot in System Verilog with an IPC of 0.90. Implemented Parameterized Sequential Multiplier & Divider

RTL to GDS II Design of Lightweight Encryption ("Simon") Engine

- Designed a Verilog RTL behavioral netlist for the generation of 32 bit cipher text using 32 bit plain text and 64 bit key, also designed netlist for the generation of 64 bit key for encrypting 32 bit plaintext during each round.
- Created Layout of the entire cipher using Cadence Encounter. Verified the geometry and connectivity ensuring no setup and hold violations are obtained. Extracted power of entire circuit using Synopsys Primetime Static Timing Analysis.

AWARDS & RECOGNITION

- Promotions, SanDisk High5 Awards, MVP Award and Exceptional Impact Award for various projects at Western Digital.
- Certificate of Recognition for excellent contributions and achieving remarkable milestone at Micron Inc.
- Outstanding Teaching Assistant Award & Tuition Fees Waiver at Arizona State University.
- Gold Medal & Merit based Scholarship for Consistent Academic Performance by Gujarat Technological University.