

Senior Dynamic Memory Controller RTL Engineer

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Hybrid

3900 N Capital of Texas Hwy, Austin, TX, USA
3655 N 1st St, San Jose, CA, USA

Posted 2 Days Ago

R75657

Position Summary

Samsung is a world leader in Memory, LCD and System LSI technologies that has the vision and commitment to invest in the future of technology – demonstrated by the \$17B investment in the new 3nm Fab in Texas and the commitment to invest in dramatically expanding design activities across GPU, System IP and SoC Architecture. We are currently looking for exceptional hardware and software engineers join our System IP team in our Austin, TX R & D Center (SARC) and our Advanced Computing Lab (ACL) in San Jose, CA. Our rapidly growing System IP team develops proprietary coherent interconnect and memory controller deployed in many high volume products. A wealth of opportunities for well qualified candidates.

Role and Responsibilities

Job Description

As a senior RTL design engineer, you will work as part of a memory controller IP design team. You will be tasked with driving the RTL design, performance and power optimization of various sub-blocks of the dynamic memory controller. Solid engineer foundation and RTL design experience is desired for success.

Key responsibilities include:

- Produce quality RTL on schedule meeting PPA goals
- Responsible for key blocks within the Memory Controller
- Engage with others for PPA optimization
- Partner with the physical design and CAD team to resolve implementation level details
- Work closely with design verification to test plan and otherwise ensure proper functionality

- Deliver quality micro-architectural level documentation

Minimum requirements:

- BSEE, Computer Engineer or comparable and 7+ years of experience
- Experience owning and driving the RTL design of various sub-blocks of the memory controller for the high performance digital designs
- Demonstrated experience of successful Architectural through RTL design experience on high performance and high efficiency digital designs
- Detailed knowledge of memory subsystem design
- Detailed knowledge of existing and emerging JEDEC memory standards

Skills and Qualifications

Preferred candidate will possess the following:

- Energetic, curiosity, and passion in logic design
- Good written and verbal communication skills
- Efficient digital design techniques
- Knowledge of interconnect and bus protocols with Arm CHI/ACE interconnect experience preferred
- Knowledge of cache subsystem design and optimization

Compensation for this role will vary among specific regions due to geographic differentials in the labor market, actual pay will be determined considering factors such as relevant skills and experience, and comparisons to other employees in the role. However, compensation in the following regions is expected to be as follows:

Colorado: Compensation is expected to be between \$144,345 to \$223,735

NYC: Compensation is expected to be between \$144,345 to \$223,735

Washington State: Compensation is expected to be between \$166,024 to \$257,366

California: Compensation is expected to be between \$166,024 to \$257,366

Regular full-time employees (salaried or hourly) have access to benefits including: medical, dental, vision, life insurance, 401(k), free onsite lunch, employee purchase program, tuition assistance (after 6 months), paid time off, student loan program, wellness incentives, and many more. In addition, regular full-time employees (salaried or hourly) are eligible for MBO bonus compensation, based on company, division, and individual performance.

#SARC

#ACL

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