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Patrick Harrington 2nd
Talent Acquisition Partner at AMD
Job poster

31 mutual connections

Message

## About the job

#### WHAT YOU DO AT AMD CHANGES EVERYTHING

We care deeply about transforming lives with AMD technology to enrich our industry, our communities, and the world. Our mission is to build great products that accelerate next-generation computing experiences – the building blocks for the data center, artificial intelligence, PCs, gaming and embedded. Underpinning our mission is the AMD culture. We push the limits of innovation to solve the world's most important challenges. We strive for execution excellence while being direct, humble, collaborative, and inclusive of diverse perspectives. This is who we are at our best. One Company. One Team.

AMD together we advance\_

RTL Design Engineer

## The Role

The focus of the role is owning and creating complex circuitry in RTL for development of AMD's graphics processor unit (GPU) resulting in a fast, low power, efficient, best in class ASIC.

## THE PERSON:

• An analytical thinker with problem-solving skills and excellent attention to detail

- · Possesses excellent comprehension, communication, and interpersonal skills
- · Enjoys working in a fast-paced, multi-project team environment using state of the art tools and technology

#### **KEY RESPONSIBILITIES:**

- Collaborate with system and IP level architects to understand the features to be implemented and document the low-level hardware architecture
- · Create design documentation, accounting for interactions with other features and the existing hardware system, both your block and the neighboring blocks
- Implement the design in Verilog or System Verilog, ensuring adherence to our RTL coding guidelines
- · Creating a design that has high-performance, low power, minimum area, and can execute with a very high clock frequency
- · Improve existing designs to improve performance and clock frequency, while reducing area and power
- · Run and analyze reports and resolve issues from: linting, timing, synthesis, and formal verification.
- · Assist debugging test failures in both simulation, emulation, and silicon environments
- Create SystemVerilog coverpoints and assertions to allow verification and full functional coverage of your code. Review code coverage, and work with DV to achieve code coverage closure.

#### PREFERRED EXPERIENCE:

- · Proficient in writing efficient RTL code in Verilog and System Verilog including use of a source control system and RTL linting tools
- Proficient in debugging RTL code using simulation tools, including the ability to determine if the root cause of a failing test is the firmware, hardware, or test
  issue
- Engineering tools experience with VCS, Spyglass, DC, and Formality
- Experience in Graphics IP pipeline is a plus

### **ACADEMIC CREDENTIALS:**

· Bachelors or Masters degree in Computer Engineering/Electrical Engineering; Master degree preferred

Location: Orlando, FL or Austin, TX

At AMD, your base pay is one part of your total rewards package. Your base pay will depend on where your skills, qualifications, experience, and location fit into the hiring range for the position. You may be eligible for incentives based upon your role such as either an annual bonus or sales incentive. Many AMD employees have the opportunity to own shares of AMD stock, as well as a discount when purchasing AMD stock if voluntarily participating in AMD's Employee Stock Purchase Plan. You'll also be eligible for competitive benefits described in more detail here.

AMD does not accept unsolicited resumes from headhunters, recruitment agencies, or fee-based recruitment services. AMD and its subsidiaries are equal opportunity, inclusive employers and will consider all applicants without regard to age, ancestry, color, marital status, medical condition, mental or physical disability, national origin, race, religion, political and/or third-party affiliation, sex, pregnancy, sexual orientation, gender identity, military or veteran status, or any other characteristic protected by law. We encourage applications from all qualified candidates and will accommodate applicants' needs under the respective laws throughout all stages of the recruitment and selection process.

See less ^

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Design Engineer, Orlando, FL

♣ Set alert

### Employer-provided

### Pay range in Orlando, FL

Exact compensation may vary based on skills, experience, and location.

Base salary

\$125,440/yr - \$188,160/yr

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Top applicants

10%

You're in the top 10% of 45 applicants based on your LinkedIn profile

45 Applicants -

1 Applicant in the past day

To maximize your chances of getting this job, be sure to update your profile with the most relevant skills

Most common applicant skills

You have 4 out of the 10 most common skills among all other applicants

- Python (Programming Language)
- Verilog
- ▼ Field-Programmable Gate Arrays (FPGA)
- VHDL

- C (Programming Language)
- MATLAB
- SystemVerilog
- RTL Design
- Application-Specific Integrated Circuits (ASIC)

Applicant seniority level

21 Entry level applicants

5 Senior level applicants

Applicant education level

**70**%

have a Master's Degree (Similar to you)

**14**<sub>9</sub>

have a Bachelor's Degree

9%

have a Master of Business Administration

**7**<sub>%</sub>

have other degrees

Applicants are in these locations

# 1-5 applicants ✓

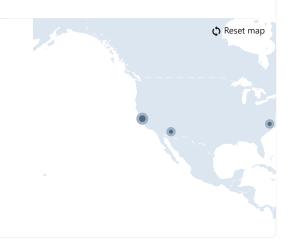
San Francisco Bay Area

# 1-5 applicants

Greater Phoenix Area

# 1-5 applicants

Raleigh-Durham-Chapel Hill Area

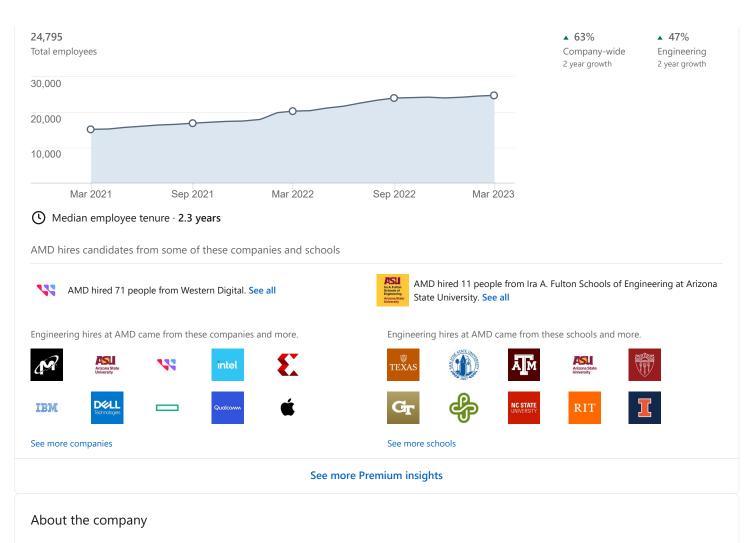


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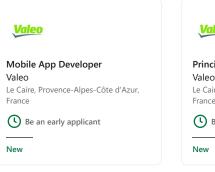


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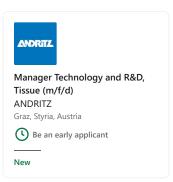
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Calgary, AB

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Junior Microsoft Integration Engineer (Sept 2023) delaware BeLux

Ghent Metropolitan Area



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New



## **UI/UX** Designer

Valeo

Le Caire, Provence-Alpes-Côte d'Azur,





#### ASSISTANT STORE MANAGER

Family Dollar

Elizabethtown, NC



New



# General Manager, BRAC Enterprises Liberia Ltd., BRAC...

Monrovia, Montserrado County, Liberia

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#### **R&D Manager**

Bergamo, Lombardy, Italy



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# Full Stack Developer AVP #222105

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