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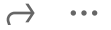
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Senior SOC Integration Design Engineer

Submitted resume

AMD · San Jose, CA (On-site) · 1 week ago · **16 applicants**



\$138,400/yr - \$207,600/yr · Full-time · Mid-Senior level



10,001+ employees · Semiconductor Manufacturing



31 connections · 71 company alumni · 11 school alumni



Skills: Static Timing Analysis, RTL Design, +8 more

Job activity

Application submitted

1 second ago

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Eric Miles · 1st

Talent Acquisition Recruiter at AMD

Job poster

252 mutual connections

Message

About the job

WHAT YOU DO AT AMD CHANGES EVERYTHING

We care deeply about transforming lives with AMD technology to enrich our industry, our communities, and the world. Our mission is to build great products that accelerate next-generation computing experiences – the building blocks for the data center, artificial intelligence, PCs, gaming and embedded. Underpinning our mission is the AMD culture. We push the limits of innovation to solve the world's most important challenges. We strive for execution excellence while being direct, humble, collaborative, and inclusive of diverse perspectives. This is who we are at our best. One Company. One Team.

AMD together we advance_

The Role

The focus of this role is to plan, build, and execute the design of new and existing features for AMD's datacenter/automotive IP.

THE PERSON:

You have a passion for modern, complex processor architecture, digital design in general. You are a team player who has excellent communication skills and experience collaborating with other engineers located in different sites/timezones. You have strong analytical and problem-solving skills and are willing to learn and ready to take on problems.

KEY RESPONSIBILITIES:

- Perform Logic design for integration of hard macros, functional units, subsystems, vendor IPs into SoC designs.
- Perform all aspects of the SoC design flow in high-level design, develop and maintain methodology/flows/checks.
- Work closely with Chip Architecture, Design verification, Physical Design, DFT teams to achieve first tapeout success.
- Work with multi-disciplinary groups to make sure designs are delivered on time and with the highest quality
- Participate in silicon bring-up for features owned

PREFERRED EXPERIENCE:

- Integrating ASIC IP into SOC & block level RTL design.
- Automation using scripting techniques such as PERL, Python or TCL
- Experience running quality checks such as Lint and CDC
- Experience with simulation/debugging and building block level verification suites
- Experience in synthesis, static timing analysis and ECO
- Design interfacing to PD for floor planning and timing closure
- Excellent verbal and written communication skills, ability to develop clear and concise engineering documentation

ACADEMIC CREDENTIALS:

- Bachelors or Masters degree in computer engineering/Electrical Engineering

At AMD, your base pay is one part of your total rewards package. Your base pay will depend on where your skills, qualifications, experience, and location fit into the hiring range for the position. You may be eligible for incentives based upon your role such as either an annual bonus or sales incentive. Many AMD employees have the opportunity to own shares of AMD stock, as well as a discount when purchasing AMD stock if voluntarily participating in AMD's Employee Stock Purchase Plan. You'll also be eligible for competitive benefits described in more detail [here](#).

AMD does not accept unsolicited resumes from headhunters, recruitment agencies, or fee-based recruitment services. AMD and its subsidiaries are equal opportunity, inclusive employers and will consider all applicants without regard to age, ancestry, color, marital status, medical condition, mental or physical disability, national origin, race, religion, political and/or third-party affiliation, sex, pregnancy, sexual orientation, gender identity, military or veteran status, or any other characteristic protected by law. We encourage applications from all qualified candidates and will accommodate applicants' needs under the respective laws throughout all stages of the recruitment and selection process.

[See less](#) ^

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System-on-Chip Design Engineer, San Jose, CA

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Employer-provided

Pay range in San Jose, CA

Exact compensation may vary based on skills, experience, and location.

Base salary

\$138,400/yr - \$207,600/yr

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PREMIUM



See how you compare to other applicants

Top applicants

50% You're in the **top 50% of 16 applicants** based on your LinkedIn profile
16 Applicants -
0 Applicants in the past day

To maximize your chances of getting this job, be sure to update your profile with the most relevant skills

Most common applicant skills

You have **3 out of the 10 most common skills** among all other applicants

- C (Programming Language)
- Very-Large-Scale Integration (VLSI)
- RTL Design
- System on a Chip (SoC)
- ModelSim
- MATLAB
- Verilog
- Application-Specific Integrated Circuits (ASIC)
- VHDL
- Field-Programmable Gate Arrays (FPGA)

Applicant seniority level

10 Entry level applicants

4 Senior level applicants

Applicant education level

73% have a Master's Degree (Similar to you)
27% have a Bachelor's Degree

Applicants are in these locations

5-10 applicants ✓

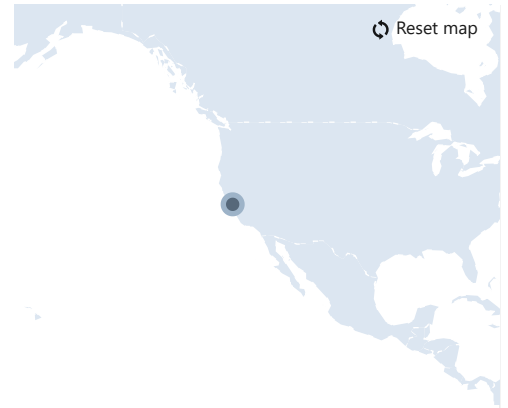
San Francisco Bay Area

1-5 applicants

Greater Bengaluru Area

1-5 applicants

Greater Munich Metropolitan Area



PREMIUM

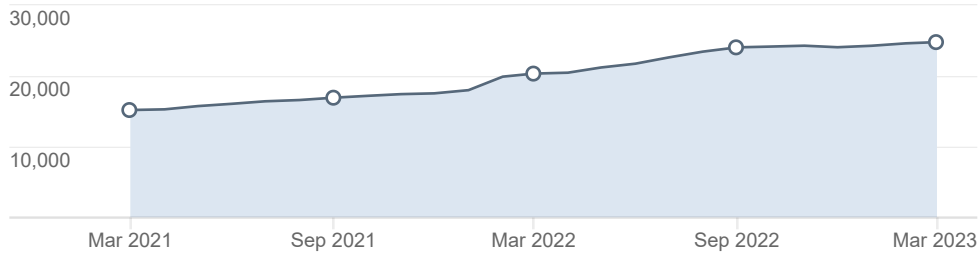


See if AMD is hiring people like you

The latest hiring trends.

24,795

Total employees



▲ 63%
Company-wide
2 year growth

▲ 47%
Engineering
2 year growth

🕒 Median employee tenure · 2.3 years

AMD hires candidates from some of these companies and schools



AMD hired 71 people from Western Digital. [See all](#)



AMD hired 11 people from Ira A. Fulton Schools of Engineering at Arizona State University. [See all](#)

Engineering hires at AMD came from these companies and more.



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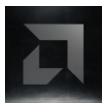
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About the company



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New



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E-Frontiers
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Vacaturebericht Deskundige wonen/omgeving
Lokaal bestuur Hemiksem
Hemiksem, Flemish Region, Belgium

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Information Technology Support Specialist
Cellebrite
Petah Tikva, Center District, Israel

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Manama, Capital Governorate, Bahrain

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New



Deputy Director - Network Operations (WAN)
PepsiCo
Peerancheru, Telangana, India

1 connection


New



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Larsen & Toubro
Jerusalem


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Personal Assistant
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Sensor Test LTE/5G Engineer- IOT
Capgemini Engineering
Greater Bengaluru Area

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Pets at Home
Redhill, England, United Kingdom

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COMECO
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