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Ibrahim Rupawala
Sr. Engineer at SanDisk, a Western Digital Brand

Projects

- Design and verification of 5 Stage pipelined MIPS R3000 microprocessor with Data Hazard Detection, Data Forwarding, Control Hazard Detection & Branch Delay Slot (Course: Constructionist Approach to Microprocessor Design)Design and verification of 5 Stage pipelined MIPS R3000 microprocessor with Data Hazard Detection, Data Forwarding, Control Hazard Detection & Branch Delay Slot (Course: Constructionist Approach to Microprocessor Design)
  Apr 2017 - Jul 2017Apr 2017 - Jul 2017
  - Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
  - • Designed and verified Single Cycle, 5 Stage pipelined and 5 Stage pipelined with forwarding unit MIPS R300 microprocessor in System Verilog with an IPC of 0.90.
    • Developed exhaustive test environments for DUT and achieved an Error Rate = 0.0.
    Compiled and synthesized the design using Genesis2 extension of System Verilog, which allows Perl elaboration of System Verilog. Extracted the Area, Power and Timing Reports for the same.
    • Designed and verified Single Cycle, 5 Stage pipelined and 5 Stage pipelined with forwarding unit MIPS R300 microprocessor in System Verilog with an IPC of 0.90. • Developed exhaustive test environments for DUT and achieved an Error Rate = 0.0.
    Compiled and synthesized the design using Genesis2 extension of System Verilog, which allows Perl elaboration of System Verilog. Extracted the Area, Power and Timing Reports for the same.
- Implementation of Cache Replacement Policy on Gem5 (Course: Advanced Computer Architecture)Implementation of Cache Replacement Policy on Gem5 (Course: Advanced Computer Architecture)
  Apr 2017 - Jul 2017Apr 2017 - Jul 2017
  - Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
  - • Implemented the following cache replacement policy on Gem5: Least Recently Used (LRU), LRU Insertion Policy (LIP), Bimodal Insertion Policy (BIP), Dynamic Insertion Policy (DIP), Static Random Replacement Insertion Policy (SRRIP), Bimodal Random Replacement Insertion Policy (BRRIP) and Dynamic Random Replacement Insertion Policy (DRRIP).
    • Characterized and analysed the impact on Miss Rate and IPC for Benchmarks Bzip2, Mcf and Sjeng implementing all these cache replacement policies for L2 cache using C++.

    Languages: C++
    Tools used: Gem5
    • Implemented the following cache replacement policy on Gem5: Least Recently Used (LRU), LRU Insertion Policy (LIP), Bimodal Insertion Policy (BIP), Dynamic Insertion Policy (DIP), Static Random Replacement Insertion Policy (SRRIP), Bimodal Random Replacement Insertion Policy (BRRIP) and Dynamic Random Replacement Insertion Policy (DRRIP). • Characterized and analysed the impact on Miss Rate and IPC for Benchmarks Bzip2, Mcf and Sjeng implementing all these cache replacement policies for L2 cache using C++. Languages: C++ Tools used: Gem5
- Study of thermal characteristics of Micro-architectural blocks using gem5, McPAT and Hotspot (Course: Advanced Computer Architecture)Study of thermal characteristics of Micro-architectural blocks using gem5, McPAT and Hotspot (Course: Advanced Computer Architecture)
  Apr 2017 - Jul 2017Apr 2017 - Jul 2017

- - • Examined the temperature impact of the Rodinia benchmarks - backprop and srad, and SPEC benchmark - mcf, on the micro-architectural blocks of the simulated ARM-based Quad-core Exynos 5422 Cortex - A15 processor using gem5, McPAT and HotSpot.
    • Reported the top 10 hottest micro-architectural blocks on the core at which each of the application is executed on. Correlated the activity counts and the power consumption of these micro-architectural blocks with the observed temperature trends.

    Tools used: Gem5, McPAT, Hospot
    • Examined the temperature impact of the Rodinia benchmarks - backprop and srad, and SPEC benchmark - mcf, on the micro-architectural blocks of the simulated ARM-based Quad-core Exynos 5422 Cortex - A15 processor using gem5, McPAT and HotSpot. • Reported the top 10 hottest micro-architectural blocks on the core at which each of the application is executed on. Correlated the activity counts and the power consumption of these micro-architectural blocks with the observed temperature trends. Tools used: Gem5, McPAT, Hospot

- Design of hardware accelerator for single source shortest path (SSSP) Dijkstra Algorithm (Course: Hardware Acceleration & FPGA)Design of hardware accelerator for single source shortest path (SSSP) Dijkstra Algorithm (Course: Hardware Acceleration & FPGA)
  Apr 2017 - May 2017Apr 2017 - May 2017
  - - Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
    - Show project
    - - • Designed a hardware accelerator using Synopsys Model Compiler for Dijkstra Algorithm used widely in the applications like segmentation of pixels, routing packets in network protocol and path planning of robots.
        • Optimized the design using architectural optimizations techniques like parallelism. A graph with 52 vertices can be fed into the circuit simultaneously and the outputs can be obtained almost at the same time. With the architectural optimizations applied the hardware accelerator was found to be almost 50 times faster than the software counterpart.
        • Mapped the design into Xilinx Virtex 7 XC7VX485T- 2FFG1761 FPGA and 28nm ASIC target and extracted area, power and timing reports.

        Languages: C
        Tools used: MATLAB, Simulink, Synopsys Synplify Pro, Synopsys Design Compiler, Synopsys VCS, Synopsys Model Compiler, Synopsys High-Level Synthesis Token, • Designed a hardware accelerator using Synopsys Model Compiler for Dijkstra Algorithm used widely in the applications like segmentation of pixels, routing packets in network protocol and path planning of robots. • Optimized the design using architectural optimizations techniques like parallelism. A graph with 52 vertices can be fed into the circuit simultaneously and the outputs can be obtained almost at the same time. With the architectural optimizations applied the hardware accelerator was found to be almost 50 times faster than the software counterpart. • Mapped the design into Xilinx Virtex 7 XC7VX485T-2FFG1761 FPGA and 28nm ASIC target and extracted area, power and timing reports. Languages: C Tools used: MATLAB, Simulink, Synopsys Synplify Pro, Synopsys Design Compiler, Synopsys VCS, Synopsys Model Compiler, Synopsys High-Level Synthesis Token,
- Design and analysis of floating point and fixed point matrix-vector multiplication hardware using FPGA and ASIC (Course: Hardware Acceleration & FPGA)Design and analysis of floating point and fixed point matrix-vector multiplication hardware using FPGA and ASIC (Course: Hardware Acceleration & FPGA)

Mar 2017 - PresentMar 2017 - Present

Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University

- • Designed a 64x64 matrix vector multiplication engine using Symphony Model Compiler (SMC) with interleaving factors of 4 and 16.
  • For the target throughput, explored architectural techniques like Parallelism and Interleaving to achieve better energy efficiency.
  • Redesigned MVM engine for fixed point data format and optimized the same to achieve the average mean square error (MSE) of <0.1%.
  • Implemented these designs into 28nm ASIC using Synopsys High level Synthesis Token with Supply Voltage, Threshold Voltage and Sizing Optimization and compared energy and area efficiency.
  • Mapped these designs into Xilinx Virtex 7 XC7VX485T-2FFG1761 FPGA target with the required frequency.
  • Compared the resource utilization difference and noticed the overhead of doing floating-point arithmetic on FPGAs.

  Tools used: Xilinx Vivado Design Suite, MATLAB, Simulink, Xilinx System Generator, Synopsys Synplify Pro, Synopsys Design Compiler, Synopsys VCS• Designed a 64x64 matrix vector multiplication engine using Symphony Model Compiler (SMC) with interleaving factors of 4 and 16. • For the target throughput, explored architectural techniques like Parallelism and Interleaving to achieve better energy efficiency. • Redesigned MVM engine for fixed point data format and optimized the same to achieve the average mean square error (MSE) of <0.1%. • Implemented these designs into 28nm ASIC using Synopsys High level Synthesis Token with Supply Voltage, Threshold Voltage and Sizing Optimization and compared energy and area efficiency. • Mapped these designs into Xilinx Virtex 7 XC7VX485T-2FFG1761 FPGA target with the required frequency. • Compared the resource utilization difference and noticed the overhead of doing floating-point arithmetic on FPGAs. Tools used: Xilinx Vivado Design Suite, MATLAB, Simulink, Xilinx System Generator, Synopsys Synplify Pro, Synopsys Design Compiler, Synopsys VCS

- Design of hardware kernel for simple recursive algorithm using an optimized number format (Course: Hardware Acceleration & FPGA)Design of hardware kernel for simple recursive algorithm using an optimized number format (Course: Hardware Acceleration & FPGA)
  Mar 2017 - PresentMar 2017 - Present

Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University

- • Designed a fixed-point data format (WTot, TFr) that can well represent the input vector with a quantization error of $|e| \leq 0.005$ for the given recursive algorithm.
  • Designed a floating-point data format (WMan, WExp) for keeping the full precision of 5 significant digits of the results (in decimal) obtained.
  • To save area the architecture was unfolded with an unfolding factor of 1 & 4. Mapped both the designs into Xilinx Virtex 7 XC7VX485T- 2FFG1761 FPGA target.

  Tools used: MATLAB, Synopsys Model Compiler, Synopsys High Level Synthesis Token
  • Designed a fixed-point data format (WTot, TFr) that can well represent the input vector with a quantization error of $|e| \leq 0.005$ for the given recursive algorithm. • Designed a floating-point data format (WMan, WExp) for keeping the full precision of 5 significant digits of the results (in decimal) obtained. • To save area the architecture was unfolded with an unfolding

factor of 1 & 4. Mapped both the designs into Xilinx Virtex 7 XC7VX485T- 2FFG1761 FPGA target. Tools used: MATLAB, Synopsys Model Compiler, Synopsys High Level Synthesis Token

- Implementation of Synthesizable Register file (RF) and Synchronous Read Memory (SRAM) using Genesis2 (Course: Constructionist Approach to Microprocessor Design)Implementation of Synthesizable Register file (RF) and Synchronous Read Memory (SRAM) using Genesis2 (Course: Constructionist Approach to Microprocessor Design)
  Mar 2017 - PresentMar 2017 - Present
  - 
    Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
    - • Designed RTL Code of synthesizable register file having two reads and one write ports using Genesis2. The read ports were designed combinational and the write was designed synchronous.
      • Designed RTL Code of synthesizable SRAM which reads and writes synchronously. The read and write thus be mutually exclusive.
      • Simulated using Synopsys VCS and synthesized the design using Synopsys Design Compiler with given timing constraints and extracted Area, Power and Timing Reports.

      Languages: System Verilog, Genesis2 (Perl Elaboration of System Verilog)
      Tools used: Synopsys VCS, Synopsys Design Compiler
      • Designed RTL Code of synthesizable register file having two reads and one write ports using Genesis2. The read ports were designed combinational and the write was designed synchronous. • Designed RTL Code of synthesizable SRAM which reads and writes synchronously. The read and write thus be mutually exclusive. • Simulated using Synopsys VCS and synthesized the design using Synopsys Design Compiler with given timing constraints and extracted Area, Power and Timing Reports. Languages: System Verilog, Genesis2 (Perl Elaboration of System Verilog) Tools used: Synopsys VCS, Synopsys Design Compiler
- Energy-Delay Characterization of 64-bit simple ALU in 28nm CMOS technology using standard-cell-based design flow (Course: Hardware Acceleration & FPGA)Energy-Delay Characterization of 64-bit simple ALU in 28nm CMOS technology using standard-cell-based design flow (Course: Hardware Acceleration & FPGA)
  Feb 2017 - PresentFeb 2017 - Present
  - 
    Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
    - • Prototyped a simple 64-bit ALU using Synphony Model Compiler (SMC) blocks and verified the functionality in the Simulink environment.
      • Generated the RTL codes and test bench using the Symphony High Level Synthesis token with a 28nm ASIC target and verified the functionality of the same using Modelsim and synthesized the design using Design Compiler (DC).
      • Characterized E-D curve with sizing, VDD and Vth optimization using all HVT, LVT and RVT libraries for the 0.75V, 0.85V and 1V VDD setup files.
      • Calculated the energy values (Energy=Power*Delay) based on the results from the power reports and analyzed optimal energy at each delay point.

      Tools used: MATLAB, Simulink, Xilinx System Generator, Synopsys Synplify Pro, Synopsys Design Compiler, Synopsys VCS

• Prototyped a simple 64-bit ALU using Synphony Model Compiler (SMC) blocks and verified the functionality in the Simulink environment. • Generated the RTL codes and test bench using the Symphony High Level Synthesis token with a 28nm ASIC target and verified the functionality of the same using Modelsim and synthesized the design using Design Compiler (DC). • Characterized E-D curve with sizing, VDD and Vth optimization using all HVT, LVT and RVT libraries for the 0.75V, 0.85V and 1V VDD setup files. • Calculated the energy values (Energy=Power*Delay) based on the results from the power reports and analyzed optimal energy at each delay point. Tools used: MATLAB, Simulink, Xilinx System Generator, Synopsys Synplify Pro, Synopsys Design Compiler, Synopsys VCS

- Implementation of Parameterized Sequential Multiplier and Sequential Divider using Genesis2 (Course: Constructionist Approach to Microprocessor Design)Implementation of Parameterized Sequential Multiplier and Sequential Divider using Genesis2 (Course: Constructionist Approach to Microprocessor Design)
  Feb 2017 - PresentFeb 2017 - Present
  - Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
    - • Designed RTL Code of Sequential Multiplier and Sequential Divider using Genesis2 extension of System Verilog, which allows Perl elaboration of System Verilog.
      • Developed exhaustive test environments for DUT and achieved an Error Rate = 0.0 errors out of 100000 test cases.
      • Simulated using Synopsys VCS and synthesized the design using Synopsys Design Compiler with given timing constraints and extracted Area, Power and Timing Reports.

      Languages: System Verilog, Genesis2 (Perl Elaboration of System Verilog)
      Tools used: Synopsys VCS, Synopsys Design Compiler• Designed RTL Code of Sequential Multiplier and Sequential Divider using Genesis2 extension of System Verilog, which allows Perl elaboration of System Verilog. • Developed exhaustive test environments for DUT and achieved an Error Rate = 0.0 errors out of 100000 test cases. • Simulated using Synopsys VCS and synthesized the design using Synopsys Design Compiler with given timing constraints and extracted Area, Power and Timing Reports. Languages: System Verilog, Genesis2 (Perl Elaboration of System Verilog) Tools used: Synopsys VCS, Synopsys Design Compiler
- Performance Simulation and Evaluation of given Out of order Microprocessors using Gem5 as a processor simulator in full system mode (Course: Computer Architecture)Performance Simulation and Evaluation of given Out of order Microprocessors using Gem5 as a processor simulator in full system mode (Course: Computer Architecture)
  Feb 2017 - PresentFeb 2017 - Present
  - Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
    - • Executed Benchmarks like Bzip2, Mcf and Sjeng on the simulated system and collected performance statistics and use the information to analyze the application as well the system characteristics.
      • Modulated the parameters of the processor like fetch width, decode width commit width, ROB size, Load and Store queue size, Integer and Floating point registers, Predictor size, Local History table size and evaluated the IPC performance of the given 3 Benchmarks.
      • Investigate the effects of various branch prediction schemes (local, global and tournament) on the branch address prediction rate.

Languages: C
Tools used: Gem5
• Executed Benchmarks like Bzip2, Mcf and Sjeng on the simulated system and collected performance statistics and use the information to analyze the application as well the system characteristics. • Modulated the parameters of the processor like fetch width, decode width commit width, ROB size, Load and Store queue size, Integer and Floating point registers, Predictor size, Local History table size and evaluated the IPC performance of the given 3 Benchmarks. • Investigate the effects of various branch prediction schemes (local, global and tournament) on the branch address prediction rate. Languages: C Tools used: Gem5

- Register file Dumping Routine in MIPS assembly language (Course: Constructionist Approach to Microprocessor Design)Register file Dumping Routine in MIPS assembly language (Course: Constructionist Approach to Microprocessor Design)
  Feb 2017 - PresentFeb 2017 - Present
  - Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
    - • Implemented assembly language program (Callable from C program as a C function) that writes the values of the entire register file (all 32 registers) to a fixed set of memory locations. • Ensured that no register values were modified with the function return.

      Languages: MIPS Assembly language, C
      Tools used: MIPS toolchain including gcc compiler, assembler and processor simulator from Imagination Technologies
      • Implemented assembly language program (Callable from C program as a C function) that writes the values of the entire register file (all 32 registers) to a fixed set of memory locations. • Ensured that no register values were modified with the function return. Languages: MIPS Assembly language, C Tools used: MIPS toolchain including gcc compiler, assembler and processor simulator from Imagination Technologies
- Design, Synthesis & APR of a Synchronous 64 Bit MultiplierDesign, Synthesis & APR of a Synchronous 64 Bit Multiplier
  Dec 2016 - PresentDec 2016 - Present
  - Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
    - •Developed Behavioural RTL Code, Gate level netlist using Cadence RTL Compiler, APR netlist using Cadence Encounter. Verified the functionality of all the netlists using Modelsim. •Verified the design for geometry and connectivity errors ensuring no setup or hold violations are obtained.
      •Extracted the power of the design using Synopsys Primetime.

      Languages: Verilog, TCL
      Tools used: Modelsim, Cadence RTL Compiler, Cadence Encounter, Synopsys Primetime•Developed Behavioural RTL Code, Gate level netlist using Cadence RTL Compiler, APR netlist using Cadence Encounter. Verified the functionality of all the netlists using Modelsim. •Verified the design for geometry and connectivity errors ensuring no setup or hold violations are obtained. •Extracted the power of the design using Synopsys Primetime. Languages: Verilog, TCL Tools used: Modelsim, Cadence RTL Compiler, Cadence Encounter, Synopsys Primetime
- Cross Point Memory Array with RRAM Devices (Course: Semiconductor Memory Technologies and Systems)Cross Point Memory Array with RRAM Devices (Course: Semiconductor Memory Technologies

and Systems)
Nov 2016 - PresentNov 2016 - Present

- Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
- •Examined the array size effect on write and read margin. Studied the scaling trend of the RRAM array and the effect of the same on write and read margins.
  •Studied the concept of non-linearity effect and sneak path in the RRAM array.
  •Compared Multi-bit and Single-bit write schemes. Examined the write energy of the entire array and the write energy per bit for both the schemes.

  Languages: Hspice
  Tools used: 32-nm LOW POWER PTM model (http://ptm.asu.edu), Synopsys Waveform Viewer
  •Examined the array size effect on write and read margin. Studied the scaling trend of the RRAM array and the effect of the same on write and read margins. •Studied the concept of non-linearity effect and sneak path in the RRAM array. •Compared Multi-bit and Single-bit write schemes. Examined the write energy of the entire array and the write energy per bit for both the schemes. Languages: Hspice Tools used: 32-nm LOW POWER PTM model (http://ptm.asu.edu), Synopsys Waveform Viewer

- Design & Simulation of Single Ended NMOS Input Folded Cascode Amplifier with Class AB buffer circuit (Course: Advanced Analog Integrated circuits)Design & Simulation of Single Ended NMOS Input Folded Cascode Amplifier with Class AB buffer circuit (Course: Advanced Analog Integrated circuits)
  Nov 2016 - PresentNov 2016 - Present
  - Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
  - •Designed an n-input folded-cascode OTA with a Class AB buffer stage using TSMC 0.25um CMOS technology in Cadence, simulated using Spectre.
    •Biased the amp using a constant-gm bias generator. Designed for open-loop gain of 80dB, GBW >50MHz, phase margin > 60dB and gain margin >15dB. Obtained 1V peak-to-peak swing at the output with a 50 ohm load in parallel with 200pF capacitance
    •Achieved PSRR (at 10kHz) of >80 dB, CMRR of >80 dB (at 10kHz) and limited thermal noise floor to <10nV/sqrtHz. Limited power consumption to 2mW.

    Tools used: Cadence ICFB (Cadence5)
    •Designed an n-input folded-cascode OTA with a Class AB buffer stage using TSMC 0.25um CMOS technology in Cadence, simulated using Spectre. •Biased the amp using a constant-gm bias generator. Designed for open-loop gain of 80dB, GBW >50MHz, phase margin > 60dB and gain margin >15dB. Obtained 1V peak-to-peak swing at the output with a 50 ohm load in parallel with 200pF capacitance •Achieved PSRR (at 10kHz) of >80 dB, CMRR of >80 dB (at 10kHz) and limited thermal noise floor to <10nV/sqrtHz. Limited power consumption to 2mW. Tools used: Cadence ICFB (Cadence5)
- Design and Exploration of STT-RAM Bank using NVSim (Course: Semiconductor Memory Technologies and Systems)Design and Exploration of STT-RAM Bank using NVSim (Course: Semiconductor Memory Technologies and Systems)
  Nov 2016 - PresentNov 2016 - Present
  -

Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University

- •Studied and compared“Total Area”, “Read Latency”, “Write Latency”, “Read Dynamic Energy”, “Write Dynamic Energy”, and “Leakage Power” of SRAM and STT-RAM for 2MB and 16MB Banks.
  •Plotted Area vs Write pulse width, Read latency vs Write pulse width, Write latency vs Write pulse width, Read dynamic energy vs Write pulse width, Write dynamic energy vs Write pulse width, Leakage power vs Write pulse width varying the write pulse width of the STT-RAM.

  Tools used: NVSim simulator (http://nvsim.org)
  •Studied and compared“Total Area”, “Read Latency”, “Write Latency”, “Read Dynamic Energy”, “Write Dynamic Energy”, and “Leakage Power” of SRAM and STT-RAM for 2MB and 16MB Banks. •Plotted Area vs Write pulse width, Read latency vs Write pulse width, Write latency vs Write pulse width, Read dynamic energy vs Write pulse width, Write dynamic energy vs Write pulse width, Leakage power vs Write pulse width varying the write pulse width of the STT-RAM. Tools used: NVSim simulator (http://nvsim.org)

- Design and Simulation of Symmetric Operational Transconductance Amplifier (OTA) (Course: Advanced Analog Integrated circuits)Design and Simulation of Symmetric Operational Transconductance Amplifier (OTA) (Course: Advanced Analog Integrated circuits)
  Nov 2016 - PresentNov 2016 - Present

  Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University

  - •Designed and simulated three versions of OTA: Basic OTA, Enhanced Output Impedance OTA using Cascode, Enhanced Output Impedance two-stage miller compensated OTA with a Common Source Buffer.
    •Implemented the layout of two-stage miller compensated OTA using common centroid and inter digitization techniques.
    •Achieved Power Dissipation of 0.889mW, GBW of 61.2 MHz, DC Gain of 95.01 dB, Phase Margin of 64.85 degree, Slew Rate of 14.09 V/us and input referred thermal noise of 9.8 nV/sqrt(Hz) for two-stage miller compensated OTA.

    Tools used: Cadence ICFB (Cadence5)•Designed and simulated three versions of OTA: Basic OTA, Enhanced Output Impedance OTA using Cascode, Enhanced Output Impedance two-stage miller compensated OTA with a Common Source Buffer. •Implemented the layout of two-stage miller compensated OTA using common centroid and inter digitization techniques. •Achieved Power Dissipation of 0.889mW, GBW of 61.2 MHz, DC Gain of 95.01 dB, Phase Margin of 64.85 degree, Slew Rate of 14.09 V/us and input referred thermal noise of 9.8 nV/sqrt(Hz) for two-stage miller compensated OTA. Tools used: Cadence ICFB (Cadence5)

- Design and Simulation of Voltage Sense Amplifier and Current Sense Amplifier using HSPICE Script and Synopsys Waveform Viewer (Course: Semiconductor Memory Technologies and Systems)Design and Simulation of Voltage Sense Amplifier and Current Sense Amplifier using HSPICE Script and Synopsys Waveform Viewer (Course: Semiconductor Memory Technologies and Systems)
  Nov 2016 - PresentNov 2016 - Present

  Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University

  - •Simulated the curves to understand the basic operation of voltage sense amplifier and current sense amplifier and one resistive ram cell
    •Simulated the curves to find the Bitline Development time, reference voltage Vref and

sensing delay for voltage sense amplifier
•Optimized the voltage sense amplifier design to restrict the sensing delay below 5ns
•Simulated the curves to find the Sensing delay for the current sense amplifier

Languages: Hspice
Tools used: 32-nm LOW POWER PTM model (http://ptm.asu.edu), Synopsys Waveform Viewer •Simulated the curves to understand the basic operation of voltage sense amplifier and current sense amplifier and one resistive ram cell •Simulated the curves to find the Bitline Development time, reference voltage Vref and sensing delay for voltage sense amplifier •Optimized the voltage sense amplifier design to restrict the sensing delay below 5ns •Simulated the curves to find the Sensing delay for the current sense amplifier Languages: Hspice Tools used: 32-nm LOW POWER PTM model (http://ptm.asu.edu), Synopsys Waveform Viewer

- Design of Lightweight Encryption (“Simon”) Engine (Part of Simon and Speck families of lightweight block ciphers developed by U.S. National Security Agency (NSA))Design of Lightweight Encryption (“Simon”) Engine (Part of Simon and Speck families of lightweight block ciphers developed by U.S. National Security Agency (NSA))
  Nov 2016 - PresentNov 2016 - Present
  - Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
    - •Designed a behavioural netlist for the generation of 32 bit ciphertext using 32 bit plaintext and 64 bit key
      •Designed a behavioural netlist for the generation of 64 bit key for encrypting each 32 bit plaintext
      •Verified the functionality of the behavioural netlist using Modelsim and generated the gate level netlist using Cadence RC Compiler. Verified the functionality of the Gate level netlist.
      •Created Layout of the entire cipher using Cadence Encounter. Did Floor Planning, Power Planning, Pin Assignment, Clock Tree Synthesis and Routing to accomplish the same. Verified the geometry and connectivity of the same ensuring no setup and hold violations are obtained. Verified the functionality of the post layout netlist.
      •Extracted the power of the entire circuit using Synopsys Primetime Static Timing Analysis.
      •Pipelined the design to obtain the maximum throughput. Optimized the design to obtain the best Area, Power and Frequency.

      Languages: Verilog, TCL
      Tools used: Modelsim, Cadence RTL Compiler, Cadence Encounter, Synopsys Primetime•Designed a behavioural netlist for the generation of 32 bit ciphertext using 32 bit plaintext and 64 bit key •Designed a behavioural netlist for the generation of 64 bit key for encrypting each 32 bit plaintext •Verified the functionality of the behavioural netlist using Modelsim and generated the gate level netlist using Cadence RC Compiler. Verified the functionality of the Gate level netlist. •Created Layout of the entire cipher using Cadence Encounter. Did Floor Planning, Power Planning, Pin Assignment, Clock Tree Synthesis and Routing to accomplish the same. Verified the geometry and connectivity of the same ensuring no setup and hold violations are obtained. Verified the functionality of the post layout netlist. •Extracted the power of the entire circuit using Synopsys Primetime Static Timing Analysis. •Pipelined the design to obtain the maximum throughput. Optimized the design to obtain the best Area, Power and Frequency. Languages: Verilog, TCL Tools used: Modelsim, Cadence RTL Compiler, Cadence Encounter, Synopsys Primetime
- 16KB 8T SRAM Register File Design using 7 nm (FinFET) Educational PDK (Course: VLSI Design)16KB 8T SRAM Register File Design using 7 nm (FinFET) Educational PDK (Course: VLSI Design)

Oct 2016 - PresentOct 2016 - Present

- Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
  - • Designed a full custom 16 entry, 16 bit wide dynamic register file (RF) with one read port and one write port from schematics to layout using Cadence Virtuoso.
    • Performed Design Rule Check (DRC) and Layout vs Schematic (LVS) checks, obtained the parasitic extraction and performed timing analysis using HSPICE.
    • Optimized the design for Power and Performance and achieved the best energy-delay product and minimum Layout area
    • Designed and Simulated Schematic and Layout of 4x16 Decoder using two 3x8 Decoders, pre-decoder and a post decoder. Performed DRC, LVS and verified the functionality of the same.

    Languages: Hspice
    Tools used: Cadence Virtuoso, Synopsys CosmoScope, Calibre
    • Designed a full custom 16 entry, 16 bit wide dynamic register file (RF) with one read port and one write port from schematics to layout using Cadence Virtuoso. • Performed Design Rule Check (DRC) and Layout vs Schematic (LVS) checks, obtained the parasitic extraction and performed timing analysis using HSPICE. • Optimized the design for Power and Performance and achieved the best energy-delay product and minimum Layout area • Designed and Simulated Schematic and Layout of 4x16 Decoder using two 3x8 Decoders, pre-decoder and a post decoder. Performed DRC, LVS and verified the functionality of the same. Languages: Hspice Tools used: Cadence Virtuoso, Synopsys CosmoScope, Calibre
- Design of 1Transistor, 1 Capacitor DRAM Cell with the Precharge circuit and Sense amplifier (Course: Semiconductor Memory Technologies and Systems)Design of 1Transistor, 1 Capacitor DRAM Cell with the Precharge circuit and Sense amplifier (Course: Semiconductor Memory Technologies and Systems)
  Oct 2016 - PresentOct 2016 - Present
  - Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
    - • Simulated the curves to find the minimum difference between the bit lines for successful read operation
      • Used sub-array technique to increase the voltage difference between the Bitlines, so that read can be done easily.
      • Extracted bit line signal development time Δt (The time during which sense amplifier should be turned on at the moment when the voltage difference is larger than minimum required)
      • Simulated the timing diagram of the DRAM cell in the array and measured the sense amp set time

      Languages: Hspice
      Tools used: 32-nm LOW POWER PTM model (http://ptm.asu.edu), Synopsys Waveform Viewer• Simulated the curves to find the minimum difference between the bit lines for successful read operation • Used sub-array technique to increase the voltage difference between the Bitlines, so that read can be done easily. • Extracted bit line signal development time Δt (The time during which sense amplifier should be turned on at the moment when the voltage difference is larger than minimum required) • Simulated the timing diagram of the DRAM cell in the array and measured the sense amp set time Languages: Hspice Tools used: 32-nm LOW POWER PTM model (http://ptm.asu.edu), Synopsys Waveform Viewer

- Design of Telescopic Cascode Differential Amplifier (Course: Advanced Analog Integrated circuits)Design of Telescopic Cascode Differential Amplifier (Course: Advanced Analog Integrated circuits)
  Oct 2016 - PresentOct 2016 - Present
  - Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
  - • Designed Telescopic Cascode differential amplifier stage with all the necessary biasing circuits with a load of 1pF at the output and tail current less than 40uA.
    • Used Beta Multiplier and Wide Swing Cascode circuit to bias the amplifier
    • Achieved Gain of 71.31 dB, Gain Crossover Frequency of 51.07MHz, CMRR of 94.41 dB, PSRR of 134.6 dB and slew rate of 1.56MV/s

    Tools used: Cadence ICFB (Cadence5)• Designed Telescopic Cascode differential amplifier stage with all the necessary biasing circuits with a load of 1pF at the output and tail current less than 40uA. • Used Beta Multiplier and Wide Swing Cascode circuit to bias the amplifier • Achieved Gain of 71.31 dB, Gain Crossover Frequency of 51.07MHz, CMRR of 94.41 dB, PSRR of 134.6 dB and slew rate of 1.56MV/s Tools used: Cadence ICFB (Cadence5)
- Design, Synthesis & APR of a Synchronous 2 Bit Adder (Course: VLSI Design)Design, Synthesis & APR of a Synchronous 2 Bit Adder (Course: VLSI Design)
  Oct 2016 - PresentOct 2016 - Present
  - Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
  - • Developed Verilog RTL Behavioural Code for the 2 bit adder, Compiled and Simulated the same using Modelsim
    • Developed the RTL Compiler Script using TCL and synthesized the behavioural Verilog code using RTL Compiler thus generated Synthesized Gate Level Netlist
    • Generated APR Netlist using Encounter. Did Floor Planning, Power Planning, Pin Assignment, Clock Tree Synthesis and Routing to accomplish the same. Verified and debugged the design

    Languages: Verilog, TCL
    Tools used: Modelsim, Cadence RTL Compiler, Cadence Encounter, Synopsys Primetime
    • Developed Verilog RTL Behavioural Code for the 2 bit adder, Compiled and Simulated the same using Modelsim • Developed the RTL Compiler Script using TCL and synthesized the behavioural Verilog code using RTL Compiler thus generated Synthesized Gate Level Netlist • Generated APR Netlist using Encounter. Did Floor Planning, Power Planning, Pin Assignment, Clock Tree Synthesis and Routing to accomplish the same. Verified and debugged the design Languages: Verilog, TCL Tools used: Modelsim, Cadence RTL Compiler, Cadence Encounter, Synopsys Primetime
- Design & Simulation of Low Level D – Latch using 7nm (FINFET) educational PDK (Course: VLSI Design)Design & Simulation of Low Level D – Latch using 7nm (FINFET) educational PDK (Course: VLSI Design)
  Sep 2016 - PresentSep 2016 - Present
  - Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University

- ▪ • Created standard Cell DLLx3 using 7nm educational PDK
  • Generated the layout of the cell and performing DRC and LVS checks on the cadence virtuoso environment
  • Generated PEX Netlist and comparing the setup and hold time for the pre-layout and post-layout simulations using the HSPICE Netlist

  Languages: Hspice
  Tools used: Cadence Virtuoso, Synopsys CosmoScope, Calibre
  • Created standard Cell DLLx3 using 7nm educational PDK • Generated the layout of the cell and performing DRC and LVS checks on the cadence virtuoso environment • Generated PEX Netlist and comparing the setup and hold time for the pre-layout and post-layout simulations using the HSPICE Netlist Languages: Hspice Tools used: Cadence Virtuoso, Synopsys CosmoScope, Calibre

- Design of CMOS Beta -multiplier based constant-gm current reference current mirrors (Course: Advanced Analog Integrated circuits)Design of CMOS Beta -multiplier based constant-gm current reference current mirrors (Course: Advanced Analog Integrated circuits)
  Sep 2016 - PresentSep 2016 - Present
  - ▪ 

    Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
  - ▪ • Designed three versions of beta-multiplier based current reference generator with the help of wide swing cascode biasing using CMOS TSMC 0.25u design library kit.
    • Measures current across the range of power supplies, plotted transconductance gm for different temperatures and plotted bias voltage for the wide range of power supplies to understand and compare the different circuits.

    Tools used: Cadence ICFB (Cadence5)
    • Designed three versions of beta-multiplier based current reference generator with the help of wide swing cascode biasing using CMOS TSMC 0.25u design library kit. • Measures current across the range of power supplies, plotted transconductance gm for different temperatures and plotted bias voltage for the wide range of power supplies to understand and compare the different circuits. Tools used: Cadence ICFB (Cadence5)
- Static & Dynamic Analysis of an SRAM cell using 32nm high performance PTM model (Course: Semiconductor Memory Technologies and Systems)Static & Dynamic Analysis of an SRAM cell using 32nm high performance PTM model (Course: Semiconductor Memory Technologies and Systems)
  Sep 2016 - PresentSep 2016 - Present
  - ▪ 

    Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
  - ▪ • Simulated an HPICE command to calculate the Static Noise Margin (SNM) of an SRAM cell using butterfly curve during HOLD, READ & WRITE operation
    • Plotted the curves for SNM vs VDD & SNM vs Strength of the Pull down transistors and understood the relationship between the same
    • Plotted the timing waveform for the Dynamic READ operation and calculated the critical charge required to flip the bits stored in the SRAM Cell.

    Languages: Hspice
    Tools used: 32-nm HIGH POWER PTM model (http://ptm.asu.edu), Synopsys Waveform Viewer• Simulated an HPICE command to calculate the Static Noise Margin (SNM) of an SRAM cell using butterfly curve during HOLD, READ & WRITE operation • Plotted the

curves for SNM vs VDD & SNM vs Strength of the Pull down transistors and understood the relationship between the same • Plotted the timing waveform for the Dynamic READ operation and calculated the critical charge required to flip the bits stored in the SRAM Cell. Languages: Hspice Tools used: 32-nm HIGH POWER PTM model (http://ptm.asu.edu), Synopsys Waveform Viewer

- Design and Simulation of Differential to Single ended Amplifier (Cadence Virtuoso, Analog Design Environment)Design and Simulation of Differential to Single ended Amplifier (Cadence Virtuoso, Analog Design Environment)
  Mar 2016 - May 2016Mar 2016 - May 2016
  - • Designed and analyzed differential to single ended amplifier and measure various parameter including differential and common mode gain, CMRR & PSRR.
    • Achieved the DC gain of 25dB with Open loop swing of 100mV (peak to peak).
    • CMRR of 58.27dB and PSRR of 62.35dB was obtained

    Tools used: Cadence ICFB (Cadence5)
    • Designed and analyzed differential to single ended amplifier and measure various parameter including differential and common mode gain, CMRR & PSRR. • Achieved the DC gain of 25dB with Open loop swing of 100mV (peak to peak). • CMRR of 58.27dB and PSRR of 62.35dB was obtained Tools used: Cadence ICFB (Cadence5)
- Design and Simulation of 8-bit full custom modulo adder in 32 nm PDK (Course: Digital Systems and Circuits)Design and Simulation of 8-bit full custom modulo adder in 32 nm PDK (Course: Digital Systems and Circuits)
  Apr 2016 - PresentApr 2016 - Present
  - Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
  - • Designed schematics and layouts of 1-bit Full Adder with mirror adder configuration and master-slave D-flipflop with True Single Phase Clock (TSPC) Logic
    • Designed 8-bit Modulo Adder by connecting all the adders and D-flipflops based on pipeline structure.
    • Achieved Energy Delay Product of 61.96 ps*pJ , layout area of 180.20 µm2 & Delay of 533ps
    • The goal of this project is to minimize the Energy-Delay Product (EDP) and Layout Area.

    Languages: Hspice
    Tools used - Cadence Virtuoso, Calibre, Spectre, Hercules, StarRC, Synopsys CosmoScope
    • Designed schematics and layouts of 1-bit Full Adder with mirror adder configuration and master-slave D-flipflop with True Single Phase Clock (TSPC) Logic • Designed 8-bit Modulo Adder by connecting all the adders and D-flipflops based on pipeline structure. • Achieved Energy Delay Product of 61.96 ps*pJ , layout area of 180.20 µm2 & Delay of 533ps • The goal of this project is to minimize the Energy-Delay Product (EDP) and Layout Area. Languages: Hspice Tools used - Cadence Virtuoso, Calibre, Spectre, Hercules, StarRC, Synopsys CosmoScope
  - Other creatorsOther creators
    - 
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- Design and Simulation of two stage Miller compensated Operational Amplifier (Cadence Virtuoso, Analog Design Environment)Design and Simulation of two stage Miller compensated Operational Amplifier (Cadence Virtuoso, Analog Design Environment)
  Apr 2016 - PresentApr 2016 - Present
  - Associated with Ira A. Fulton Schools of Engineering at Arizona State UniversityAssociated with Ira A. Fulton Schools of Engineering at Arizona State University
  - • Designed a 2-stage Fully Differential Operational Amplifier with Unity gain Miller compensation and RHP zero cancellation using CMOS TSMC 0.3um process.
    • Achieved the DC gain of 91.08dB with Unity Gain Frequency of 0.59MHz, Phase Margin of 62.1 degree and Output swing of 1V (peak to peak).

    Tools used: Cadence ICFB (Cadence5)• Designed a 2-stage Fully Differential Operational Amplifier with Unity gain Miller compensation and RHP zero cancellation using CMOS TSMC 0.3um process. • Achieved the DC gain of 91.08dB with Unity Gain Frequency of 0.59MHz, Phase Margin of 62.1 degree and Output swing of 1V (peak to peak). Tools used: Cadence ICFB (Cadence5)
- Automatic Spy Robot Using PIC Controller PIC18F4550 (Course: Senior Design Project)Automatic Spy Robot Using PIC Controller PIC18F4550 (Course: Senior Design Project)
  Apr 2013 - May 2013Apr 2013 - May 2013
  - Associated with Gujarat Technological University, AhmedabadAssociated with Gujarat Technological University, Ahmedabad
  - Show project
  - • Developed Wireless Controlled Robotic Vehicle which can be operated through a range of 100 meters using 433 MHz RF transmitter and receiver.
    • Used PROTEUS ISIS Schematic Capture Design Suite for developing the hardware related to the robot, SERIAL TERMINAL for transmitting control signals to the robot from the Computer, MPLAB IDE 8.53 Integrated Development Environment for the development of embedded application on PIC.

    Languages: PIC Assembly language
    Tools used: PROTEUS ISIS Schematic Capture Design Suite, MPLAB IDE 8.53
    • Developed Wireless Controlled Robotic Vehicle which can be operated through a range of 100 meters using 433 MHz RF transmitter and receiver. • Used PROTEUS ISIS Schematic Capture Design Suite for developing the hardware related to the robot, SERIAL TERMINAL for transmitting control signals to the robot from the Computer, MPLAB IDE 8.53 Integrated Development Environment for the development of embedded application on PIC. Languages: PIC Assembly language Tools used: PROTEUS ISIS Schematic Capture Design Suite, MPLAB IDE 8.53

- Accessibility
- Talent Solutions
- Community Guidelines
- Careers
- Marketing Solutions
- Privacy & Terms
- Ad Choices
- Advertising
- Sales Solutions
- Mobile
- Small Business
- Safety Center

- Questions?

  Visit our Help Center.

- Manage your account and privacy

  Go to your Settings.

Select Language العربية (Arabic)

Status is online

Messaging You are on the messaging overlay. Press enter to open the list of conversations.

Compose message

You are on the messaging overlay. Press enter to open the list of conversations.

See and edit how you look to people who are not signed in, and find you through search engines (ex: Google, Bing).

Creating a profile in another language makes it easier for local business contacts and recruiters to find you on LinkedIn.

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