Alex Siyoung Park

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PROFESSIONAL SUMMARY

Industry experience in fields of flash memory algorithm development, flash product development, product characterization, data analysis, process integration, and semiconductor device physics. Expert in semiconductor flash memory in both development and sustaining activities, including cell operating algorithm development, SSD qualification, statistical data/yield analysis and physical/electrical failure analysis. Organized and detail-oriented problem solver who enjoys the challenges and creative freedom of working in a dynamic, hands-on R&D environment.

TECHNICAL SKILLS

Flash Memory & CMOS │SSD Development │ Scripting & Data Analysis | Project Management

PROFESIONAL EXPERIENCE

SanDisk, a Western Digital Brand, Milpitas, CA **Dec.2012 to Present**
Principal Device Engineer

Technical 2D/ 3D NAND device lead for NAND memory development and SSD product supporting.

- 2D/ 3D memory development, process integration and characterization for performance, endurance, data retention and power efficiency improvement.
- Manage NAND flash device parameter optimization for SLC, MLC, TLC and QLC to meet customer spec and reliability requirement.
- Work with various internal and external SSD customers to develop different SSD products.
- Involve new NAND memory technology and spec with cross-functional teams to align the next generation of SSD requirements and priorities.
- NAND/ SSD characterization, qualification, and failure analysis for product yield improvement.
- Develop innovative systems designs, technologies, and architectures to support product roadmap.

Micron Technology, Boise, ID **Jan.2011 to Nov.2012**
Memory Cell and Process Integration Engineer

ReRAM development through all phases of the technology life cycle including initial technology development, array characterization, product algorithm development and final technology qualification.

- Develop Cu-based ionic source NV-CBRAM to replace the conventional NVM & DRAM.
- Demonstrate CBRAM that satisfies scalable, high density, switching speed, cycling endurance, data retention, and power-consumption criteria.
- Experience in the various reliability testing and failure analysis to identify & resolve production issue of CBRAM emerging memory with complex test method.
- Involve in both front-end-of-line (FEOL) and back-end-of-line (BEOL) process integration.

NIST and Johns Hopkins University, MD **Jan.2010 to Dec.2010**
Research Fellow

Team lead in the nanofabrication using nanoimprint technology and 3D structure for plasmonic devices.

- 3D self-assembly nanometer scale electronic and bio-device fabrication on silicon semiconductor materials using a method of nanoimprint lithography.
- Involve the design and fabrication of single crystal silicon based flexible photovoltaic solar cells structured via electron beam lithography technology.
- Demonstrate optical, sensory and biomedical applications with nanoscale 3D plasmonic devices.

Samsung Semiconductor, South Korea (Intern) **May.2005 to Sep.2005**
DRAM Device and Process Integration Engineer

Worked in advanced dielectric material for DRAM to improve device scalability and reliability.

- Involve in 65nm DRAM technology development in the reliability test and failure analysis.
- Develop the advanced transistor and capacitor structure of DRAM to scale down further.

Nano-electronic lab at Ohio State University, Columbus, OH **Dec.2013 to Dec.2009**
Research Associate

- Lead Si/SiGe 3D Tunnel FET (TFET) development to replace conventional CMOS technology.
- Develop Si-based quantum dot devices and logic architectures with nanoscale structure.
- Work with Resonant inter-band tunnel devices (RITD) to develop millimeter-wave detectors.

TECHNICAL EXPERTISE

Python, TIBCO Spotfire, JMP, Cadence, SPICE, L-EDIT, MATLAB, C, and device measurement/ fabrication tools

EDUCATION

The Ohio State University, Columbus, OH

PhD in Electrical and Computer Engineering	**Dec.2009**
MS in Electrical and Computer Engineering	**Jun.2006**
BS in Electrical and Computer Engineering	**Sep.2003**

PAPERS & PUBLICATION

Authored and co-authored 21 papers in journals and conferences