Contact

(480)-284-9270 (Mobile)
irupawal@asu.edu

www.linkedin.com/in/irupawala (LinkedIn)

Top Skills

Cadence Virtuoso
Cadence Encounter
Digital Circuit Design

Languages

Hindi (Native or Bilingual)
Arabic (Limited Working)
English (Full Professional)
Urdu (Professional Working)
Gujarati (Native or Bilingual)

Certifications

The Complete SQL Bootcamp
Learn C++ Programming -Beginner to Advance- Deep Dive in C++
Complete Python Bootcamp: Go from zero to hero in Python 3
Data Structures and Algorithms Specialization

Honors-Awards

Gold Medal for consistent performance in academics
Merit Based Award

Ibrahim Rupawala

Staff Engineer at SanDisk, a Western Digital Brand
San Jose

Summary

Sr Engineer working on cutting edge 3D NAND Flash Non-Volatile Memory

Technical Skills:

--> Digital Logic Design, FPGA/ASIC Design, RTL Design, Physical Design, Verification
--> Static Timing Analysis (STA), Dynamic Timing Analysis (DTA), Setup time, Hold time.
--> VCS functional simulation, gate level simulation, RTL simulation.
--> Synthesis, Floor-planning, Place & route, Clock distribution
--> UVM verification (basics), Constrained random testing.
--> System Verilog assertion-based verification & Functional coverage.

* Programming Languages:
C++, Java for test dev,TCL, Perl for scripting, Python for Data Analysis & Visualization.

* Hardware Description Languages:
Verilog, System Verilog, UVM (basics).

* EDA/Simulation Tools:
Cadence (Virtuoso, Encounter (Floor-planning, Place & route, Clock distribution), Spectre,RC Complier), Synopsys (PrimeTime, HSPICE, Hercules, Star RC, Design Compiler, VCS), Xilinx (ISE, VivadoDesign Suite), Matlab (Simulink), Mentor Graphics (Calibre, Modelsim), Gem5 processor simulator.

* Lab Tools:
Oscilloscope, Probe-Station & Memory Testers

Related Coursework:

VLSI Design, System Verilog Verification, Hardware Acceleration & FPGA, Computer Architecture, Digital Systems & Circuits, Constructionist approach to microprocessor design, Semiconductor Memory Technology.

Experience

Western Digital
Staff Software Engineer
February 2018 - Present (4 years 4 months)
Milpitas

Micron Technology
Non Volatile Engineering Product Intern
May 2017 - December 2017 (8 months)
Milpitas

Arizona State University
10 months

Graduate Teaching Assistant
October 2016 - May 2017 (8 months)
Tempe, Arizona

Graduate Service Assistant
August 2016 - December 2016 (5 months)
Tempe, Arizona

Analog Rails
Design Intern
May 2016 - October 2016 (6 months)
Tempe, Arizona

Tirupati Corporation - India
Technical Engineer
June 2013 - May 2015 (2 years)

Technical Support for the various products manufactured and sold by company. Collaborating with the Research and Development Team and Sales

& Marketing team to design electrical accessories according to the need of the clients.

Bharat Sanchar Nigam Limited
Engineering Trainee
June 2012 - July 2012 (2 months)
Surat, India

Underwent Industrial Training in GSM technology at BSNL (Largest Telecom Service Provider in India). Understanding the concepts of CDMA, GSM, network architecture, communication channel, cell division, call processing, PCM principles & multiplexing of telecommunication signals, fibre optic communication technologies and packet switching technologies.Practical experience on how the telephone exchange works.

Education

Ira A. Fulton Schools of Engineering at Arizona State University
Master’s Degree, Electrical and Electronics Engineering · (2016 - 2018)

Gujarat Technological University, Ahmedabad
Bachelor’s Degree, Electronics Engineering · (2009 - 2013)