B0:D0:F1x[93:90] - DRAM Controller - Primary Timings

| 93 | | | | | | | | 92 | | | | | | | | 91 | | | | | | | | 90 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | - | - | x | x | x | x | x | - | - | - | x | x | x | x | x |
| TRP | | | | TRCDW | | | | TRCDR | | | | TRAS | | | | | | | TRFC | | | | | | | | TRC | | | | |

B0:D0:F1x[97:94] - DRAM Controller - Secondary Timings

| 97 | | | | | | | | 96 | | | | | | | | 95 | | | | | | | | 94 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | x | x | x | - | x | x | x | - | x | x | x | - | x | x | x | - | - | x | x | - | x | x | x | - | x | x | x | - | - | - | - |
| | TDOE | | | | TRRD | | | | TWTP | | | | TWTR | | | | | TREXT | | | TRTP | | | | TRTW | | | | | | |

B0:D0:F1x[63:60] - DRAM Controller

| 63 | | | | | | | | 62 | | | | | | | | 61 | | | | | | | | 60 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x | x |
| | | | | | | | | | | | | | | | | TREF | | | | | | | | | | | | | | | |

B0:D0:F1x[73:70] - DRAM Controller - Channel B config (DIMM0 + DIMM1) - DIMM0 is furthest from the socket

| 73 | | | | | | | | 72 | | | | | | | | 71 | | | | | | | | 70 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | x | - | - | - | - | x | - | - | - | - | - | - | - | - |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | Half CAS Latency_B | | | | | | | | | | DQS Pull Down, 0 = Dis, 1 = En | | | | | | | | |

B0:D0:F1x[77:74] - DRAM Controller - Channel A config (DIMM2 + DIMM3)

| 77 | | | | 76 | | | | 75 | | | | 74 | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | x | - | - | - | - | x | - | - | - | - | - | - | - | - |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | Half CAS Latency_A | | | | | DQS Pull Down, 0 = Dis, 1 = En | | | | | | | | |

B0:D0:F1x[7F:7C] - DRAM Controller

| 7F | | | | | | | | 7E | | | | | | | | 7D | | | | | | | | 7C | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | x | x | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | Auto Precharge Write? | | Auto Precharge Read? | | | | | | | | | | | | | | | | | | | | | | | | | |

B0:D0:F1x[83:80] - DRAM Controller

| 83 | | | | | | | | 82 | | | | | | | | 81 | | | | | | | | 80 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | x | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| | | CR | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | Command Rate | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

B0:D0:F1x[87:84] - DRAM Controller

| 87 | | | | | | | | 86 | | | | | | | | 85 | | | | | | | | 84 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | - | - | - | - | - | - | - | - | x | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| | | | | | | | | | | | | | | AP | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | Auto Precharge | | | | | | | | | | | | | | | | | |

B0:D0:F1x[A3:A0] - DRAM Controller - DIMM_B0 CFG1

| A3 | | | | | | | | A2 | | | | | | | | A1 | | | | | | | | A0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | x | - | x | x | x | x | - | x | x |
| | | | | | | | | | | | | | | | | | | | | | | | D | | CAS | | | B | | L | |

D: DLL reset, 0 - Normal, 1 - Reset

B: Burst Mode, 0 - Sequential, 1 - Interleave

L: Burst Length, 010 = 4

CAS: 010 - 2, 110 - 2.5, 011 - 3, bit 6 is half latency toggle

Set bits 21, 20 and [12:9] to 0 when accessing

DIMM_B1 is [AB:A8], DIMM_A0 is [B3:B0]

B0:D0:F1x[A7:A4] - DRAM Controller - DIMM_B0 CFG2

| A7 | | | | | | | | A6 | | | | | | | | A5 | | | | | | | | A4 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | x | x |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | S | D |

S: Drive Strength Mode, 0 = Normal, 1 = Weak

D: DLL, 0 = Enable, 1 = Disable

Set bit 21 to 1, 20 and [12:3] to 0 when accessing

DIMM_B1 is [AF:AC], DIMM_A0 is [B7:B4]

B0:D0:F1x[FF:FC] - DRAM Controller

| FF | | | | | | | | FE | | | | | | | | FD | | | | | | | | FC | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | x |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SB |

SuperBypass

| B0:D0:F1x[FB:F8] - DRAM Controller | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| FB | | | | | | | | FA | | | | | | | | F9 | | | | | | | | F8 | | | | | |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | x | - | - |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | SR | | |
| | | | | | | | | | | | | | | | | | | | | | | | | Data Scavenged Rate | | | | | | | |

| B0:D0:F2, 40h, 44h, 48h, 4Bh?, bit 0 -> 1 = DIMM is installed - DIMM_B0, DIMM_B1, DIMM_A0, DIMM_A1? |
|---|

| B0:D0:F4 - DRAM Controller 4 | | |
|---|---|---|
| DIMM_B0 | Drive Strength: 65h, 71h | Slew Rate: 64h |
| DIMM_B1 | Drive Strength: 67h, 73h | Slew Rate: 66h |
| DIMM_A0 | Drive Strength: 7Dh, 81h | Slew Rate: 7Ch |