1/31/17.

Lab #4: Voltage Multiplication

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(95)

Purpose: To analyze and design a voltage multiplier.

Equipment: Protoboard, Oscilloscope, Arbitrary Waveform Generator, BNC cables, 1N4001 diodes, 0.15μF capacitors.

Procedure

(1) Build a basic voltage doubler and observe its behavior at several points in the circuit.

(2) Add a second clamping section to the circuit to increase the magnitude of the peak voltage, and another peak-detection voltage will be added for DC ~~to~~ offset.

(3) Build a 3-stage voltage doubler and observations were made at several points in the circuit.

(4) Take some measurements and comparisons & document data.

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(1) Build a basic voltage doubler.

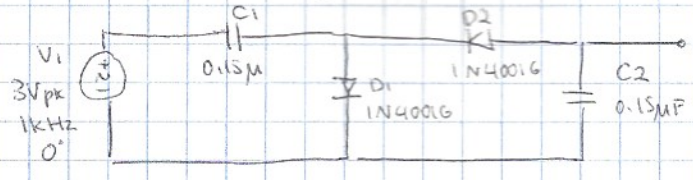


Fig 1 - Basic voltage doubler.

Using the AWG, we created the voltages V1 and V D1 (voltage across D1). (Clamped)
We also measured the voltage across capacitor C2. (Peak-Detector)

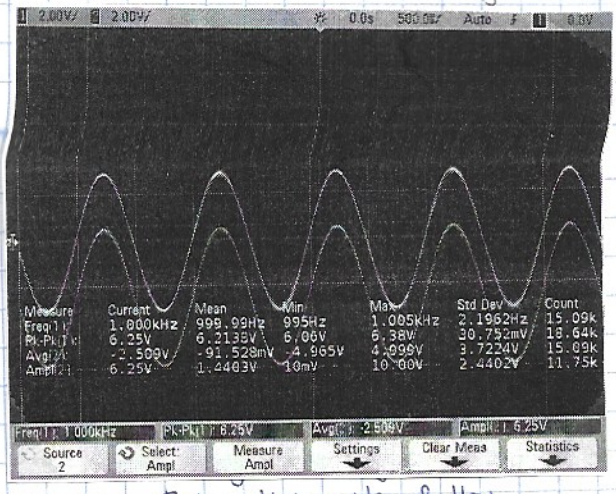


Fig 2 - Voltage VD1 & VD1

VD1 shows an avg voltage of -2.509V. This shows a -3V DC offset and the active diode voltage resulting in -2.509V. The graph shows the clamped voltage acting as DC offset.

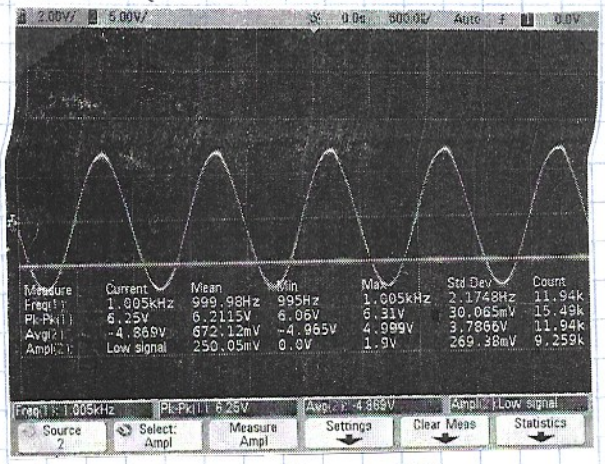


Fig 3 - Voltage V1 and VC2.

Vc2 is observed as -4.869V avg. Taking into account the negative DC offset from the clamped voltage, the result is -2.59V + -3Vpeak + 0.7x2 = -4.89V

~ 0.43% error...?

We then used the simulation capability of MultiSim to show transient analysis of these signals during the first two periods from power-up, starting from fully discharged capacitors.

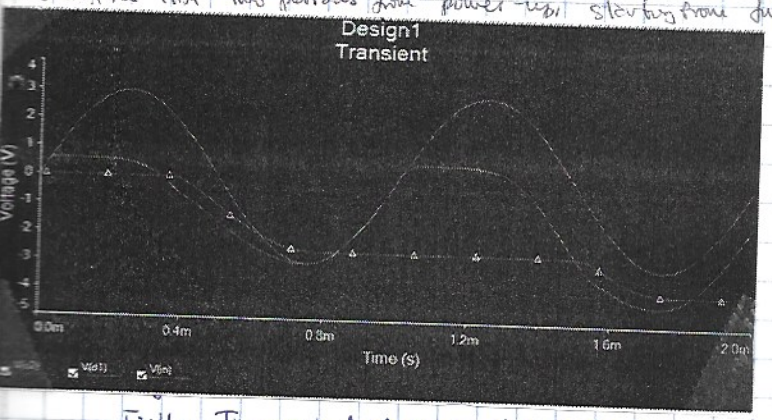


Fig 4 – Transient Analysis of Voltage Doubler.

tiene, it is observable how the capacitors are adjusting to the voltages. Since the circuit depends on the diode's biases, it may take a couple periods for the clamping voltage to reach −3V and the peak detector voltage to reach −6V.

We then attached a potentiometer (100kΩ) across C2 and recorded the voltage across the parallel combination. As we adjusted the potentiometer setting to achieve a 250mV ripple. From that, we measured the potentiometer resistance at this setting.

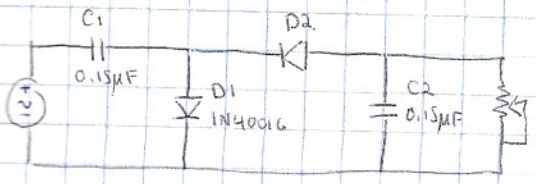


Fig 5 – Voltage Doubler w/ Potentiometer.

After the pot was adjusted to get 250mV ripple as shown in the left fig,

its resistance was measured.
This is the size load that the voltage doubler is able to regulate when the external circuit (represented by the pot) can only provide ±250mV inputs.

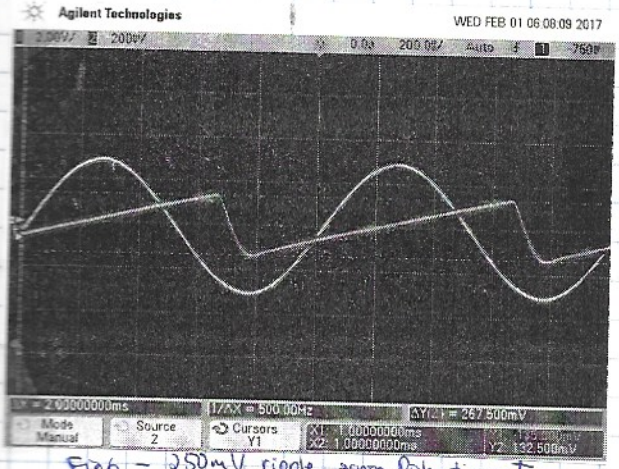


Fig 6 – 250mV ripple across Potentiometer

$R_{pot} = 102k\Omega$

$V_{pk,min} = -135mV$

$V_{DC,offset} = -4.3V$

$I_{pot} = \frac{V_{pk,min} + V_{DC,off}}{R_{pot}} = -43.58\mu A.$

This is the current (peak) flowing through the potentiometer.

(2) – Add a

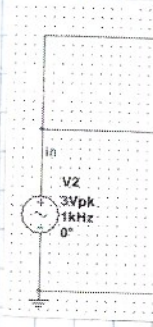


Fig 7 –

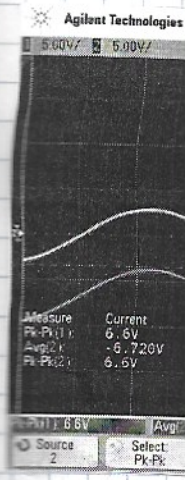


Fig 8 – 2nd s

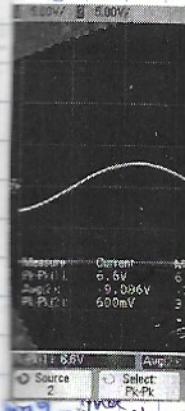


Fig 9 – 2nd stage

Add a 2nd clamping circuit & peak-detector circuit.

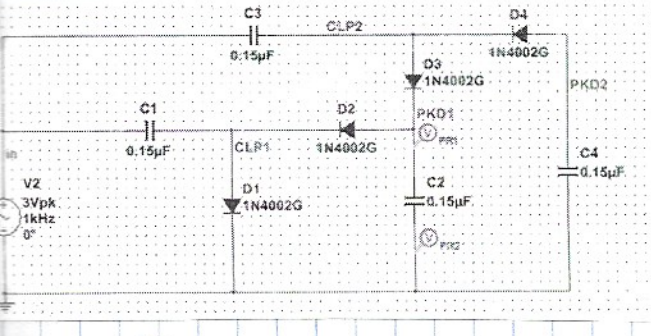


Fig 7 – 2 stage voltage multiplier.

Record scope traces showing its performance, one showing point between C3 & D3 (CLP2) and one showing the point between D4 & C4 (PKD2). displayed alongside the input.

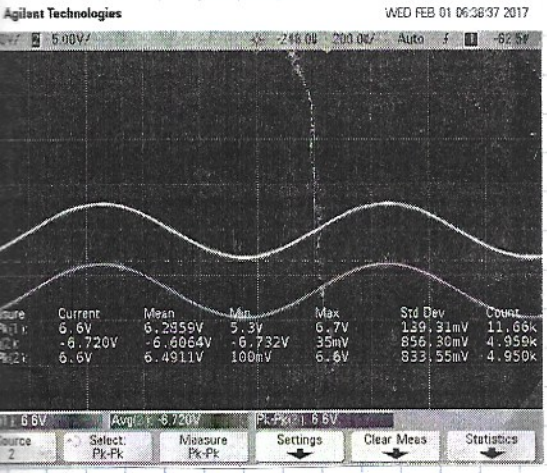


Fig 8 – 2nd stage clamped voltage

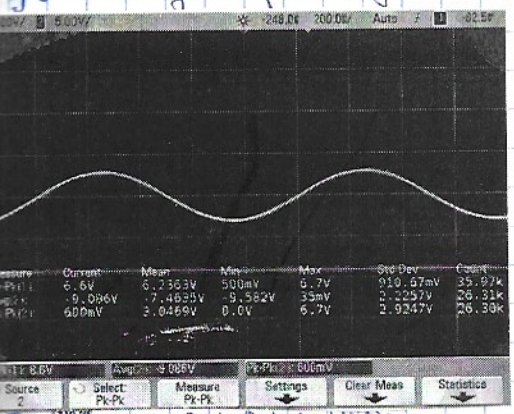
The clamped voltage in the 2nd stage is referenced by the peak-detector voltage of the 1st stage.
As a result, the clamped voltage V_{CLP2} ~~received~~ received a DC offset equivalent to V_{pkd1}.

In figure 8, the avg is -6.72 V.
From 1st stage, V_{CLP1} has DC offset $= -2.59$ V
$V_{PKD1} = -4.869$ V.
Assuming the clamped voltages 1st & 2nd stage receive the same amount of charge,

$$V_{CLP2} = V_{CLP1} + V_{PKD1} = -7.459\text{ V}$$
$$-(3 - \text{active diode}) + V_{PKD1}$$

Peak voltage in 2nd stage $= -9.086$V.
$= V_{pk}$ – active diode + DC offset (V_{CLP2})

~~With increasing stages, the peak voltage~~



97 – 2nd stage peak-detector voltage.

(3) - 3-Stage Voltage Multiplier

Build a 3-stage . . . Record V_{CLP3} & V_{PKD3}.

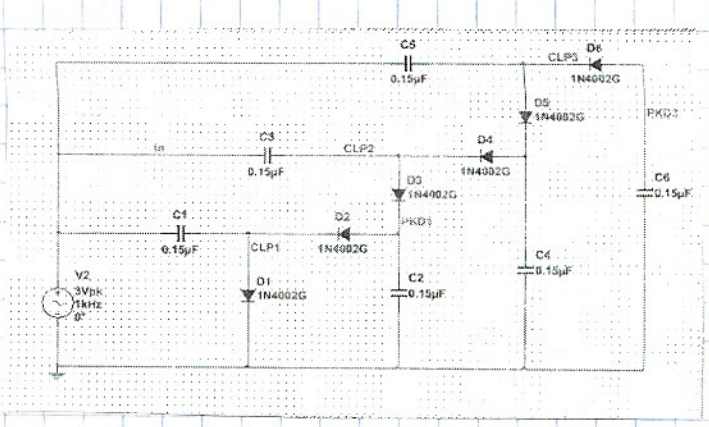


Fig 10 - 3Stage Voltage Multiplier.

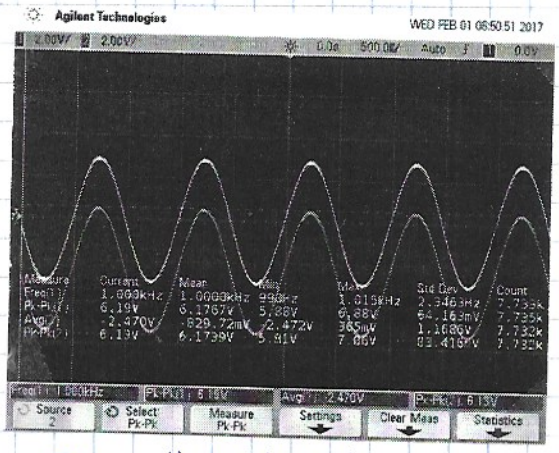


Fig 11 - V_1 and ~~V_{PKD3}~~ V_{CLP3}

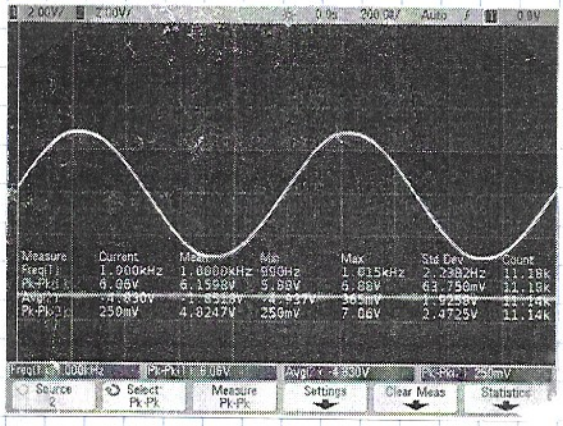


Fig 12 - V_1 and V_{PKD3}.

Discharge circuit and charged input signal to a square wave.

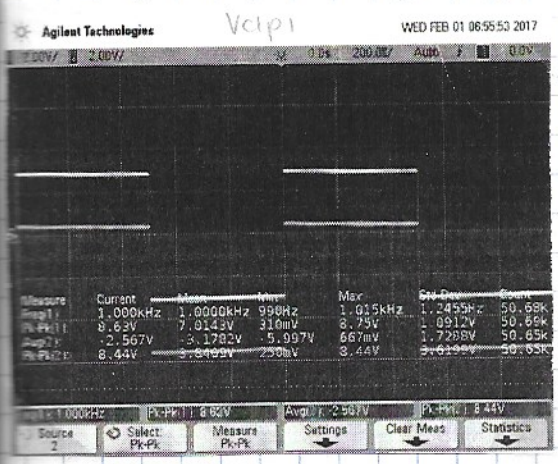


Fig 13 - VCLP1

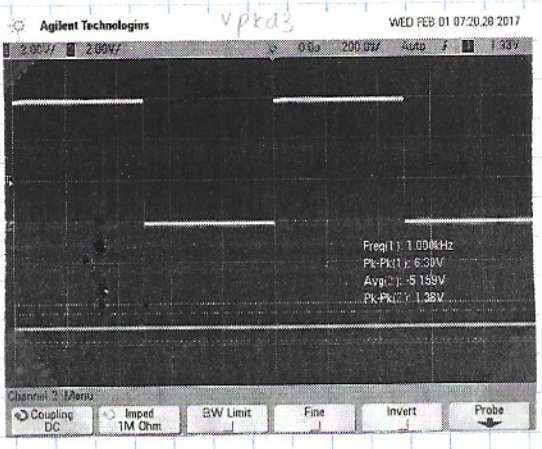


Fig 14 - VPKD3.

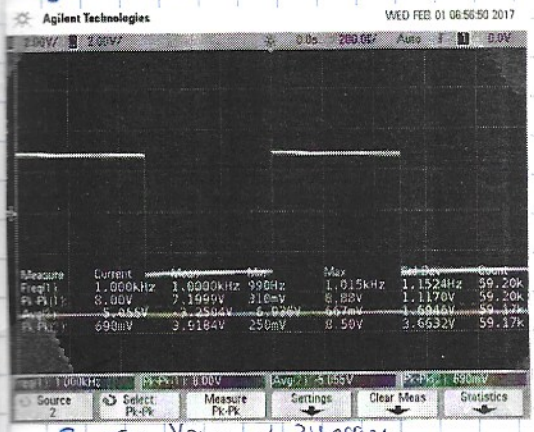


Fig 15 - VPKD3 w/ 3V offset.

The sinewave & squarewave of the 1st stage VCLP show similar avg voltages. However, the square wave has a bigger pk-to-pk voltage of 8.44V as compared to the sinewave of 6.25V.

This is suspected to be due to the capacitor as it experiences sudden changes in input. As the input becomes lower than the capacitor voltage, the charges in the capacitor won't hold and acts like a DC source. Hence, an offset is simulated. Compared to the sinewave, the change is more abrupt and it acts as a stronger source for a short amount of time to adjust ...? This explains the noise/jump in Vpk-pk.

Both with and without DC offsets showed similar avg voltages. The noticeable difference is that the signal w/ 3V offset showed periodic spikes in voltage as the signal ~~goes~~ changes from HIGH → LOW (6V → 0V).

(10) use the simulator to do transient analysis. Assume capacitors are fully discharged at time 0 and run the simulation for the first 16 periods of the input waveform.

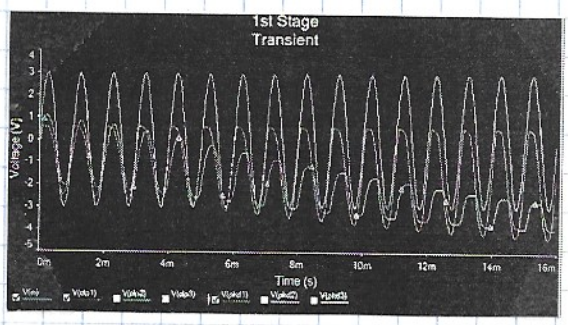


Fig 16 - Stage 1 Transient w/ 0.15μF Capacitor

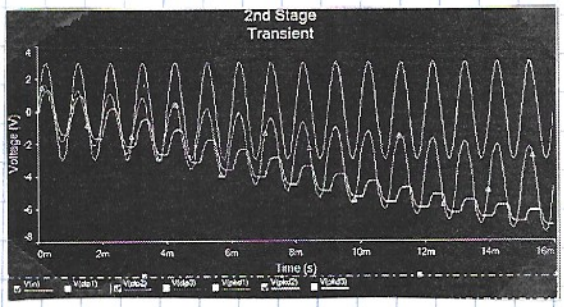


Fig 17 - Stage 2 Transient w/ 0.15μF capacitors

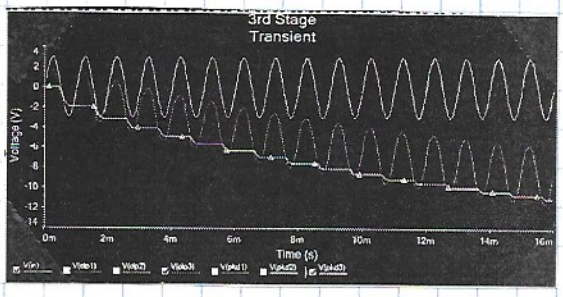


Fig 18 - Stage 3 Transient w/ 0.15μF Capacitor.

Then, replace the 0.15μF capacitors w/ ~~0.1~~ 4.7μF capacitors and repeat

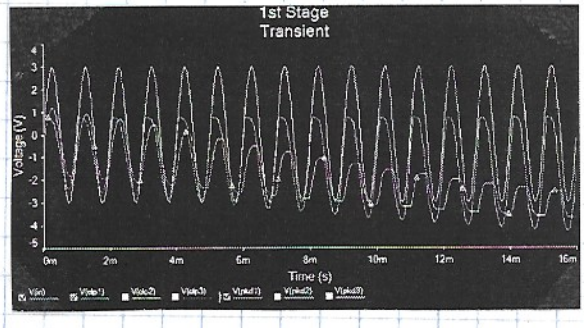


Fig 19 - Stage 1 Transient w/ 4.7μF Capacitor

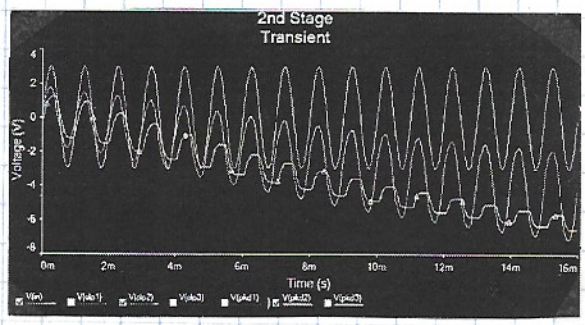


Fig 20 - Stage 2 Transient w/ 4.7μF Capacitor

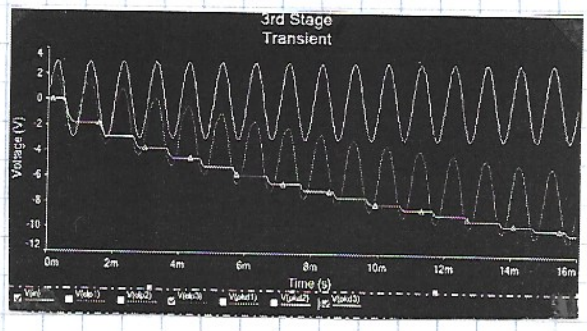


Fig 21 - Stage 3 Transient w/ 4.7μF Capacitor

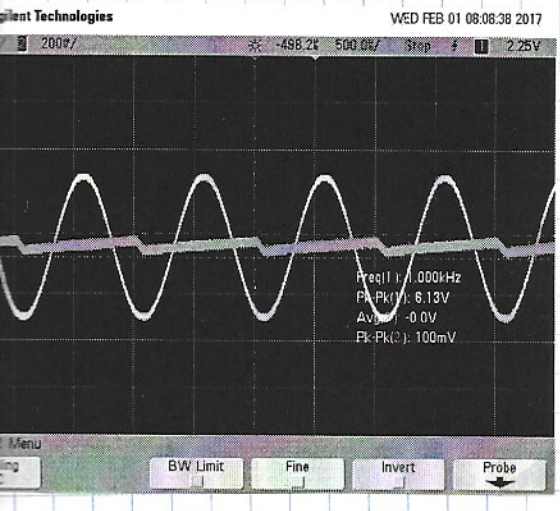
Comparing the 2 sets of analysis, it is observed that bigger capacitances resulted in a less negative clamping and peak-detected voltages, as time gets infinitely large.

This meant larger capacitances contributed to smaller offsets for the upper levels.

With the same graphs, V_{pk-pk} also oscillated w/ higher pk-pk values. This may be due to the larger capacitances being able to store and dissipate more charges.

we added a potentiometer to the real circuit across C6.

ow want to have a tolerance of 100mV at this point. 100kΩ was too small, however. we added a 680kΩ resistor in series w/ the potentiometer, summing to 780kΩ.



The measured R = 0.769MΩ
- 1.4% error from 780kΩ

$I_{pot} = -6.17\mu A$

$V_{DC,off} = -4.7\,V$

$V_{pk,min} = -41.250\,mV$

) 2z — 100mV Ripple w/ added Resistance

o 50% margin, we measured & calculated voltage & current ratings for a 5-stage ge multiplier.

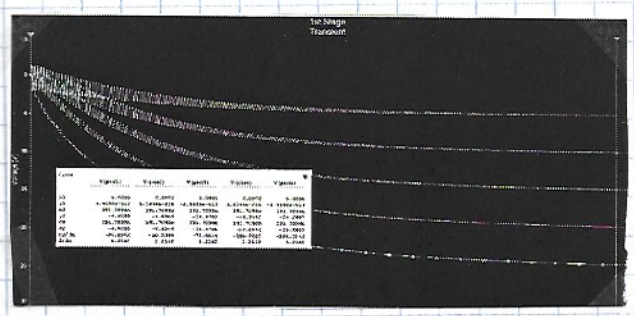


Fig 23 — Voltages for all 5 stages with respect to time

$|24.295 \times 1.5| = 36.44V$

(5th stage)

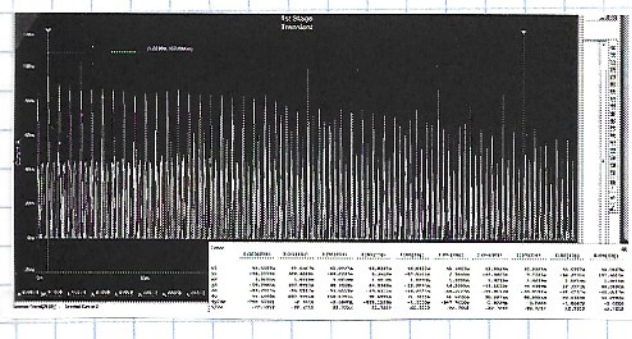


Fig 24 — Currents for all 5 stages with respect to time

$|107.8995 \times 1.5| = 161.85mA$

(1st stage)

Conclusion

The experiment demonstrated the characteristics of a voltage amplifier w/ changing variables. Before that, the basic construction of this type of voltage amplifier was introduced. The voltage amplifier used in this experiment was made up of Clamping and Peak-Detector Circuits. Oscilloscope captures showed the characteristics of these circuits. The peak-detector voltage showed a voltage amplification of 2 − (active diode voltage). The 1-stage circuit showed a -2.5 V DC offset by the clamped voltage that resulted in a -4.864V output.

Following the introduction, more stages were then added on top of the already present circuit. The noted data showed a trend: the whole upper stage was referenced by VPKD from the previous stage, creating an offset.

The circuit was also simulated w/ a square wave input. A difference in pk-pk voltage w/ the square wave noted a spike in pk-pk voltage compared to the sinusoidal input. This may have been due to those delays of diodes switching in between biases and capacitors discharging.

Further transient analysis was simulated to find the relation between the capacitance and the voltage amplification. It was concluded that larger capacitors resulted in a smaller amplified voltage as the measurement from bigger capacitors show less negative offset.

A potentiometer was then used to mimic the an external circuit. This part decided on calculating the amount of resistance the current the external load requires for a certain amount of ripple tolerance that it can handle.

The last part of understanding why the circuit doesn't blow up. A 50% margin was used to calculate voltage & current ratings of a 5-stage voltage amplifier. The largest magnitude of voltage & current were used and multiplied by 150% to obtain a rating. 50% margin is the minimum. Can be more or less depending on company

1/31/17