3EJ4 Lab 3

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**Q1:**

图表, 折线图, 散点图

描述已自动生成图表, 散点图

描述已自动生成

1. Figure of simulation and measurement.

The voltage ratio of Vo/Vsig becomes constant at about 1 when the voltage is greater than -3V. This is because all BJT works at linear region at this stage and the circuit acts as a CC amplifier.

1. Calculation:

All BJT have to work in linear region, so Vbe =0.6V. In lab 1, beta is equal to 117. Vbeon = 0.6V.

Input value should be -3V < Vsig < 5.4V.

Output value should be -3.5V < Vo <4.8V.

1. In simulation, Vsig is 0.5V. In measurement, Vsing is 0.4822V.

**Q2:**

In simulation, degree is -0.00008467 deg and gain is 0dB.

In measurement, gain is 1.2 dB and the degree is very close to 0.

This is because the ratio Vo/Vsig is very close to 1, and log(1) is 0. In measurement, the ratio of Vo/Vsig is 1.15, so we can say the simulation and measurement agree to each other.

**Q3:**

1. According to textbook:

图示

描述已自动生成

With Io = Ic

With beta approach to infinity, Io will approximately equal to Iref.

For situation when Q2 does not have the same Vec as Q1 ( Vo not equal to Veb), early voltage Va2 and output resistance ro2 will also affect Io. The complete formula is:

1. When Iref is 0.1mA, Io is 0.104mA which is 1.04Iref.

When Iref is 1mA, Io is 0.975mA which is 0.975Iref.

1. In calculation when Iref = 0.1mA, Vec is 8.95V at Q2 and 0.58V at Veb. Substitute Va = 138V and beta = 123. Io will be 0.104mA, which is very close to the simulated value.

In calculation when Iref = 1mA, Vec is 0.25V at Q2 and 0.66V at Veb. Substitute Va = 138V and beta = 123. Io will be 0.98mA, which very close to the simulated value.

Note: early voltage and beta value are from lab 1.

**Q4:**

1. The input resistance Rin is 389.12ohm. Gain is 1.042A/A
2. The output resistance is 1.58Mohm.
3. Note that h12 have different value in different frequency. At 100Hz it is 0.705u V/V. It is 1.41u V/V at 200Hz.

图示

中度可信度描述已自动生成

**Q5:**

1. In simulation, the differential mode gain is 70.07dB.
2. The offset voltage is 10.4mV
3. The gain in measurement is 59.2dB. Although it is smaller than the simulation result, we still see they agree to each other because there are uncertainty in measurement like noise.

**Q6:**

At 11207.402Hz, the gain is 3dB less and the phase -45 deg compare to that at 100Hz.

**Q7:**

The differential upper 3dB frequency without mirror load (in lab 2) is about 8.3MHz, which is much larger than 11.2kHz with mirror load.

The reason why using current mirror load have smaller fH is that the BJT at the load will have capacitance inside it. It increases the total capacitance at the output which result in a lower frequency because . Pure resistor will not increase the total capacitance at output, so the resistor load will immediately reduce the DC gain at output.

**Q8:**

In lab 2 with resistor load, GBW = fH \* gain = 8.3MHz \* 9.58 = 79.5MHz

In lab 3 with mirror load, GBW = fH \* gain = 11.2kHz \* 3189 = 35.7MHz