**Integrated System Architectures**

FREQUENTLY ASKED QUESTIONS

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PLEASE: read carefully the pdfs available on “Portale della Didattica”, several answers to your problems are already written in the documentation. Moreover, the tools very often give you important information on the command line with some details about errors, warnings, … please read them.

**Q) The tool (simulator, synthesizer, …) gives strange errors about libraries or files which are not part of the project**

A) This can happen if you are using special characters or spaces in the directories or files you are working with. Please avoid special characters and spaces in the names of directories and files.

**Q) The tool (simulator, synthesizer, …) does not start.**

A) Under /software/scripts you find all the initialization scripts, issue the command

source <init\_file>

each of these script files sets-up the environment for launching the tool

**Q) Design Compiler does not find the target library/components.**

A) Make sure you have created the “.synopsys\_dc.setup” file (the name starts with the ‘.’, dot, character). If you copy&paste the text from the pdf be aware of underscore ‘\_’ and space characters.

**Q) The tool states it cannot create the file (netlist, saif, vcd, …)**

A) Usually this happens when you try to write a file in a directory and the directory does not exist. Please check/create the directory before issuing the command.

**Q) Encounter is not able to find the VDD and GND pins.**

A) Usually this happens when you create from the scratch your configuration file. You have to download it from “Portale della Didattica” and modify it instead.

**Q) The tool cannot find a file or an element I created, but the element exists.**

A) Usually, this happens if you mix the case of characters when naming files, data, components, elements, … Please note that VHDL is not case sensitive, whereas Verilog is. As a good design rule avoid mixing the case of characters, choose your own rules and be consistent with them.

**Q) Modelsim/Questasim is not accepting all the options for switching activity annotation.**

A) The options passed to *vsim* must be all on the same command line. In the pdf they appear on different lines just due to the limited number of characters per line the document style can handle.

**Q) The command(s) shown in the pdf give an error**

A) Probably you made a ‘Copy-Paste’ from the pdf to the shell/tool/editor, please check the characters are correct (especially underscore ‘\_’ and spaces).

**Q) Design compiler crashes during the compile phase**

A) Usually, this happens when you have a combinational loop in your design. Try to remove the timing constraints and compile the unconstrained design. The compile command should give you some hints to locate where the combinational loop is.