Integrated Systems Architectures

Design of a RISC-V-lite processor Assignment

1 Assignment

The output of this lab is the following:

1. Design the RISC-V-lite processor as a synchronous circuit by defining the architecture and then detailing each block with a block scheme and a timing diagram[1].
2. Describe in VHDL or in SystemVerilog the RISC-V-lite processor you defined in the previous step.
3. Verify the correct behaviour of the processor by running the C program (*maxx*),which is available on "Portale della didattica".
4. Synthesize the HDL and verify that the netlist still behaves as your RTL description.
5. Place and route your design and very that is still behaves as your RTL description.
6. Modify the architecture by adding SSRAMs as instruction and data memories.
7. Repeat the previous steps (except place and route).

[1] Rember to use the usual good design rules: positive edge triggered only, no latches, no logic on the asynchronous reset, no internal clock dividers, ...