Integrated Systems Architectures

Verification and UVM
Assignment

1 Assignment

The output of this lab is the following:

1. Try the ALU verification example and understand how it works.
2. Stemming from the ALU verification example, build a System-Verilog verification environment for the mantissa multiplier you developed in lab2.
3. Stemming from the ALU verification example, build a System-Verilog verification environment for the fpu used in lab2.
4. Try the UVM adder example and understand how it works.
5. Modify the reference model to become a subtracter and verify the UVM environment behaviour in this case.
6. Stemming from the ALU verification example and UVM example, build a UVM environment to verify the fpu used in lab2.