

## Assignment - Timer

Create a timer with 3 inputs: *clk*, *rst*, and *end\_time* that counts from 0 to *end\_time* on every clock cycle and leaves the *timer\_done* signal high when it completes. Use the *rst* input to reset the timer after it has completed. The timer should also display the *current\_time* on every clock cycle.

Please use a two-process FSM by defining various states and an *always\_ff* and *always\_comb* block to handle clocked signals, and output signals/next\_state logic respectively.

After you complete your design, simulate it in Modelsim by following the Modelsim instructions. Create a testbench with inputs of 18, 1000, and 2048 and submit some rudimentary screenshots of the timer finishing for each of them.

Please send Isaac the completed work by our meeting time next Monday, February 3, at 9:00PM.