Once you have your *design_name*.sv and *testbench_name_tb*.sv files completed, create a *testbench_name_tb*.do file that is a script for ModelSim commands. If your design uses more files, remember to add them in the compile stage where the comment indicates.

Paste the following code block into *testbench_name_tb.*do:

```
setenv LMC_TIMEUNIT -9
vlib work
vmap work work

# compile
vlog -work work "testbench.sv"
vlog -work work "testbench_name_tb.sv"
# add more files here if necessary!

vsim -classdebug -voptargs=+acc +notimingchecks -L work work.testbench_name_tb -wlf
testbench_name_tb.wlf

# wave
add wave -noupdate -group TOP -radix binary testbench_name_tb/*


run -all
```

Save *testbench_name_tb*.do in the same folder with your other SystemVerilog files.

Go back to the terminal and source the ModelSim environment by pasting this command into the Terminal:

```
source /vol/eecs392/env/modelsim.env
```

Run the command (making sure you are in the same folder as the SystemVerilog and .do files):

```
vsim -do testbench_name_tb.do
```