



UNIVERSIDADE FEDERAL DO RIO GRANDE DO NORTE
CENTRO DE TECNOLOGIA
DEPARTAMENTO DE ENGENHARIA DA COMPUTAÇÃO E AUTOMAÇÃO



Tutorial QUARTUS

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Tutorial QUARTUS

Baixando e Instalando

Baixando e Instalando

Acesse a página:

www.altera.com/downloads/downloads-center

The screenshot shows the Altera download center interface. At the top, there are three tabs: "Select by Version" (highlighted with a purple arrow), "Select by Device", and "Select by Software". Below the tabs, there is a "Devices" section on the left with a list of Cyclone series: Cyclone IV E, Cyclone IV GX, Cyclone IV, Cyclone III LS, Cyclone III, Cyclone II (highlighted with a purple arrow), Cyclone I, and MAX Series. To the right of the devices list is a table with two columns: "Quartus Edition" and "Version Listing". The table is divided into two sections: "Subscription Edition" and "Web Edition". The "Subscription Edition" section lists versions from 13.0 down to 6.1, with some versions having service packs. The "Web Edition" section lists versions 13.0, 13.0, and 12.1. A purple arrow points to the "Web Edition" section, and a text box labeled "Versão gratuita!" (Free version!) is positioned next to it.

Quartus Edition	Version Listing
Subscription Edition	13.0, Service Pack 1
	13.0
	12.1, Service Pack 1
	12.1
	12.0, Service Pack 2
	12.0, Service Pack 1
	12.0
	11.1, Service Pack 2
	11.1, Service Pack 1
	11.1
	11.0, Service Pack 1
	10.1, Service Pack 1
	10.0, Service Pack 1
	9.1, Service Pack 2
	9.1, Service Pack 1
	9.1
	9.0
8.1	
8.0	
7.2	
7.1	
7.0	
6.1	
Web Edition	13.0, Service Pack 1
	13.0
	12.1, Service Pack 1

Versão gratuita!

Baixando e Instalando

The screenshot displays the Intel Download Center website. The browser address bar shows the URL `dl.altera.com/13.0/?edition=web`. The website header includes the Intel logo, navigation links (FPGA, PRODUCTS, SOLUTIONS, SUPPORT, ABOUT, BUY), a login button, and a search bar. A sidebar on the left lists categories: Design Software, Embedded Software, Archives, Licensing, Programming Software, Drivers, Board System Design, Board Layout and Design, and Legacy Software. The main content area lists available downloads:

- ☒ **Quartus II Help**
Size: 355.7 MB MD5: 5513707B3BE573CEBFA11656EB05DACC
- ☐ **SoC Embedded Design Suite (EDS)**
Size: 1.0 GB MD5: 76F94B628BA25783CFEBF80E59448D8A
- ☐ **Linux Support Package Binary File**
Size: 387.0 MB MD5: 9CC7736BE69B51C318CEBC51A4B9553B
- ☐ **Linux Support Package Source File**
Size: 818.3 MB MD5: 58788F0DA87F549333E9432BE82681C3

A purple arrow points to the **Download Selected Files** button. Below this button are links for System Requirements, Documentation Links, Software Support, and Legal Notice. The footer contains site links, regional information (USA, 日本, 中国), and social media links.

Desça mais um pouco

Baixando e Instalando

Akamai DLM3 Download Manager: 4 files in total.








The files you selected are being downloaded to the directory you chose. You can pause and resume the download at any time. After the download is complete, you can usually download the files with the

Baixe os 4 arquivos

Após a conclusão do *download* ...

[Hide direct links](#)

1. [QuartusSetupWeb-13.0.0.156.exe](#) (run after download)

 1- Introdução	08/08/2017 21:15	Microsoft PowerP...	1.947 KB
 Controle_Petróleo	08/08/2017 21:18	Microsoft PowerP...	8.787 KB
 26278759_File000009_605374385	09/08/2017 17:21	Adobe Acrobat D...	60 KB
 Main_Document	10/08/2017 11:18	Adobe Acrobat D...	229 KB
 QuartusSetupWeb-13.0.0.156	10/08/2017 13:58	Aplicativo	1.599.891 KB
 ModelSimSetup-13.0.0.156	10/08/2017 14:10	Aplicativo	798.086 KB
 27440899_File000001_621724551	10/08/2017 14:10	Adobe Acrobat D...	122 KB

Clique nos links de arquivo individual para fazer o download usando o seu navegador.

http://download.altera.com/akdlm/software/acdsinst/13.0/156/ib_insta...
13.0.0.156.exe

http://download.altera.com/akdlm/software/acdsinst/13.0/156/ib_insta...
13.0.0.156.exe

Duplo clique para iniciar a instalação



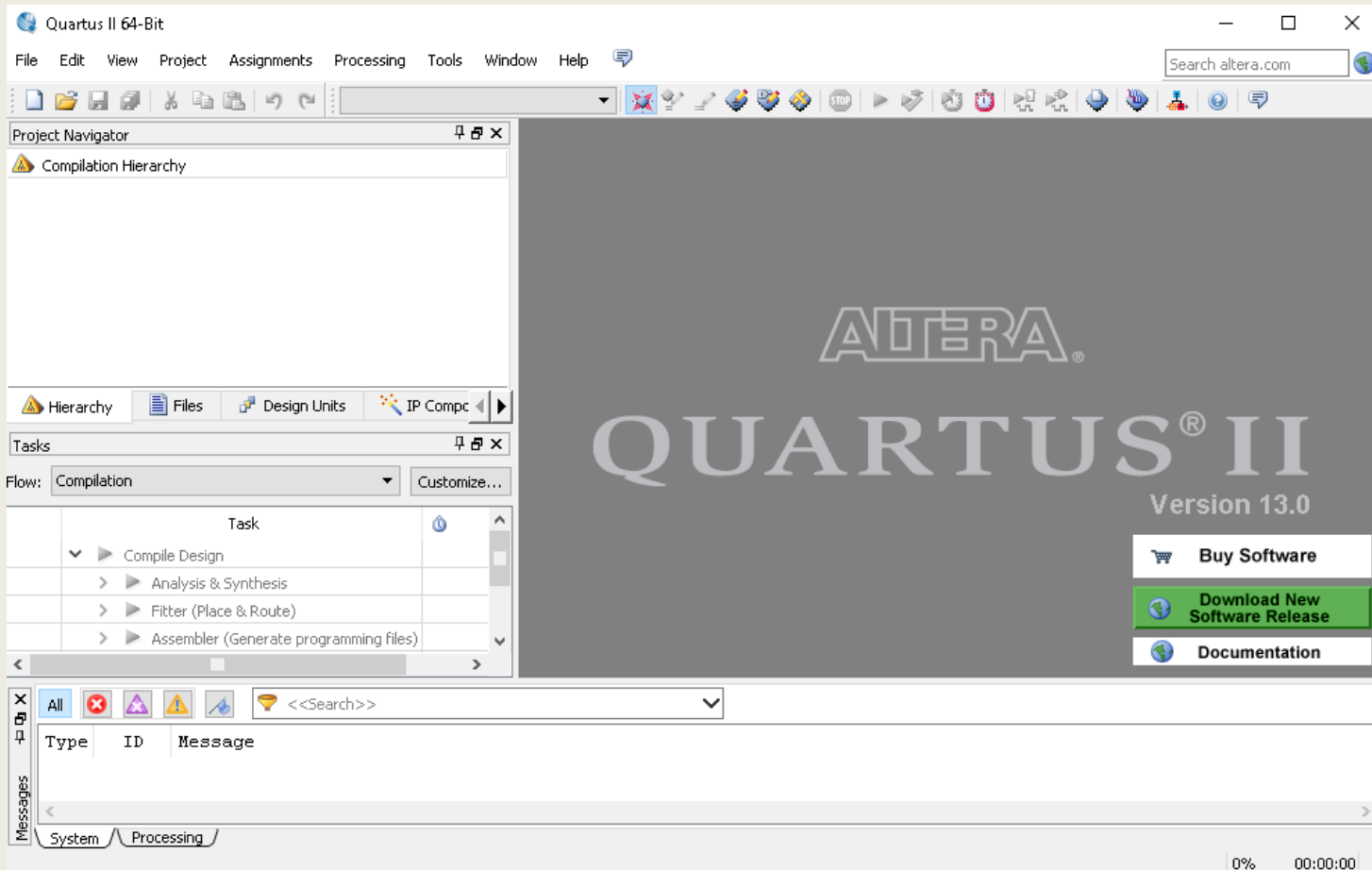
Aí é só: Next -> Agree -> Next -> Next ->

Tutorial QUARTUS

Simulando um circuito digital

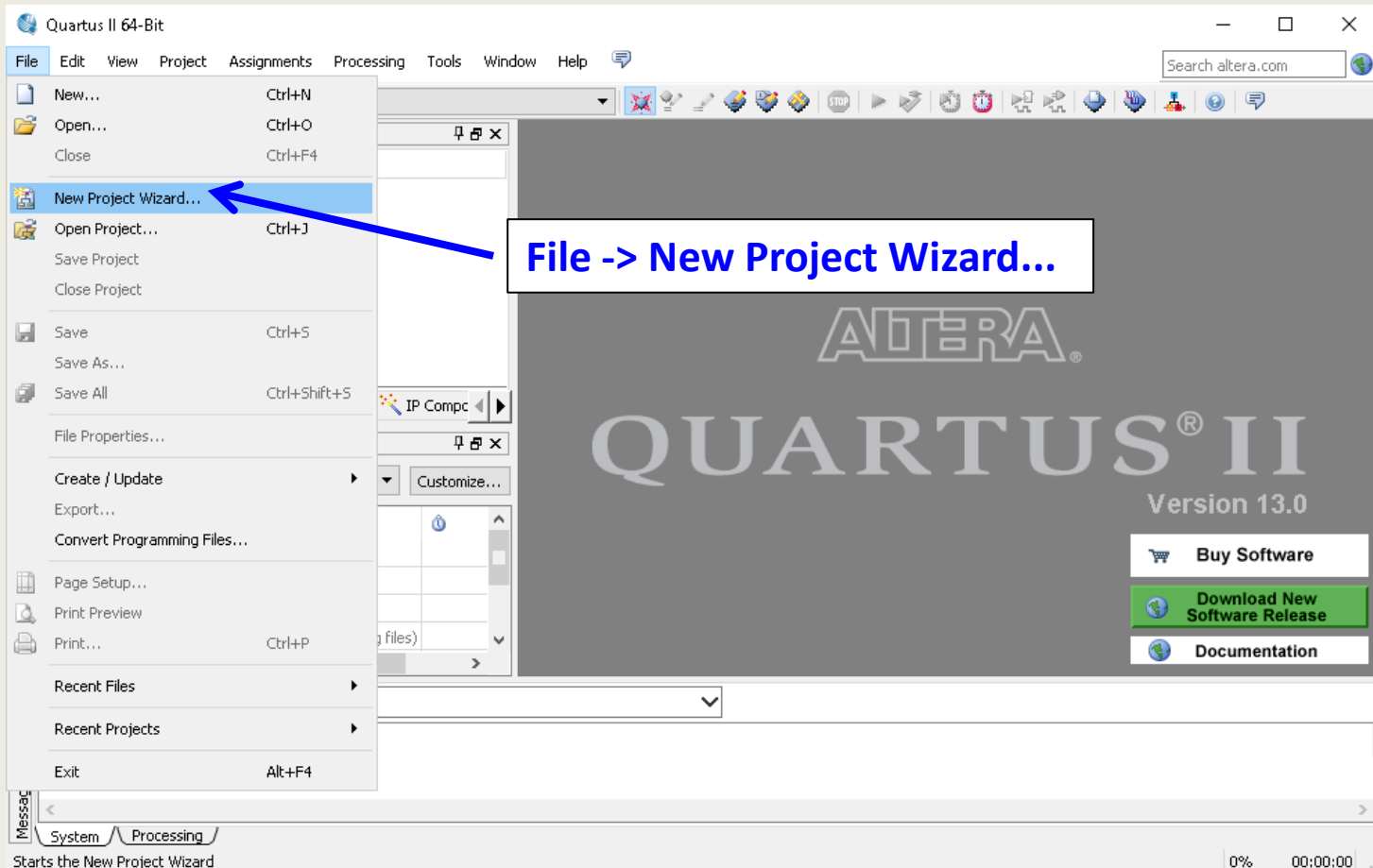
Simulando um circuito digital

Tela inicial do Quartus II Web Edition v 13.0



Simulando um circuito digital

1º passo: Crie um projeto

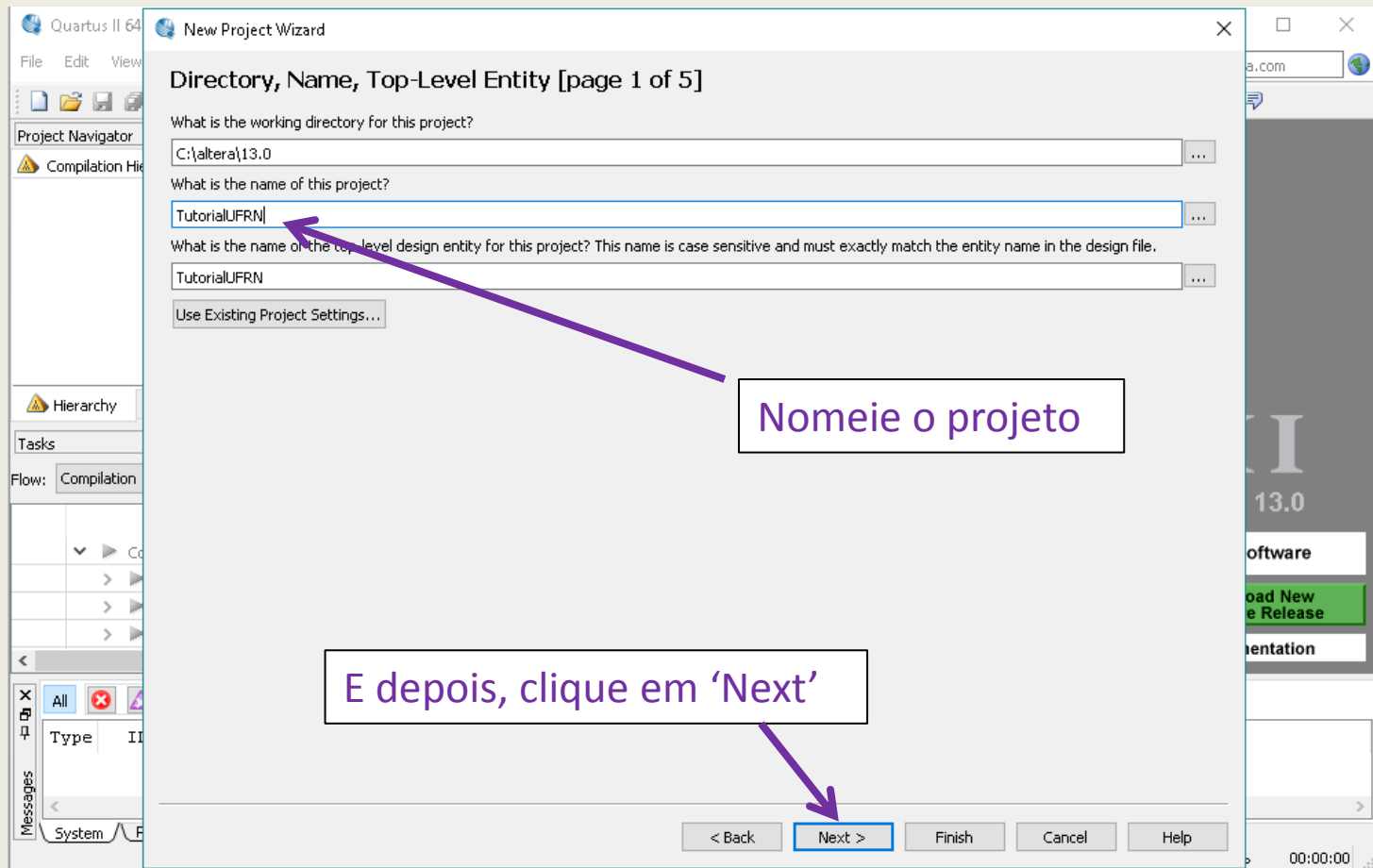


Simulando um circuito digital

1º passo: Crie um projeto

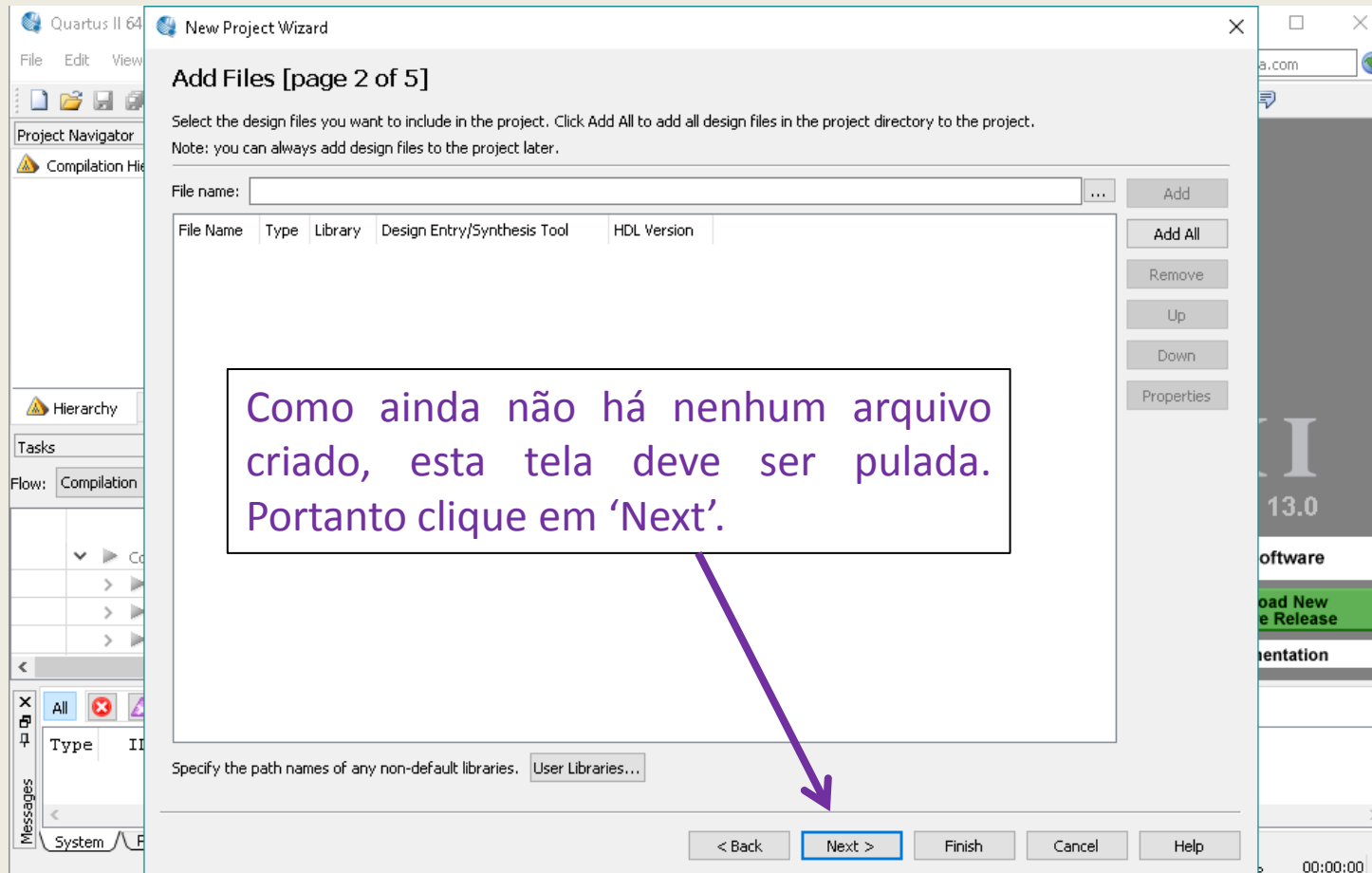
File > New Project Wizard

Clique em 'Next' logo em seguida



Simulando um circuito digital

1º passo: Crie um projeto



Simulando um circuito digital

1º passo: Crie um projeto

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

Device Family
Family: Cyclone II
Devices: All

Target device
☐ Auto device selected by the Fitter
☒ Specific device selected in 'Available devices' list
☐ Other: n/a

Show in 'Available devices' list
Package: Any
Pin count: Any
Speed grade: Any

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL	GL
EP2C35F484C7	1.2V	33216	322	483840	70	4	16
EP2C35F484C8	1.2V	33216	322	483840	70	4	16
EP2C35F484C9	1.2V	33216	322	483840	70	4	16
EP2C35F672C6	1.2V	33216	475	483840	70	4	16
EP2C35F672C7	1.2V	33216	475	483840	70	4	16
EP2C35F672C8	1.2V	33216	475	483840	70	4	16
EP2C35F672C9	1.2V	33216	475	483840	70	4	16

Companion device
HardCopy:
☐ Limit DSP & RAM to HardCopy device resources

< Back Next > Finish Cancel Help

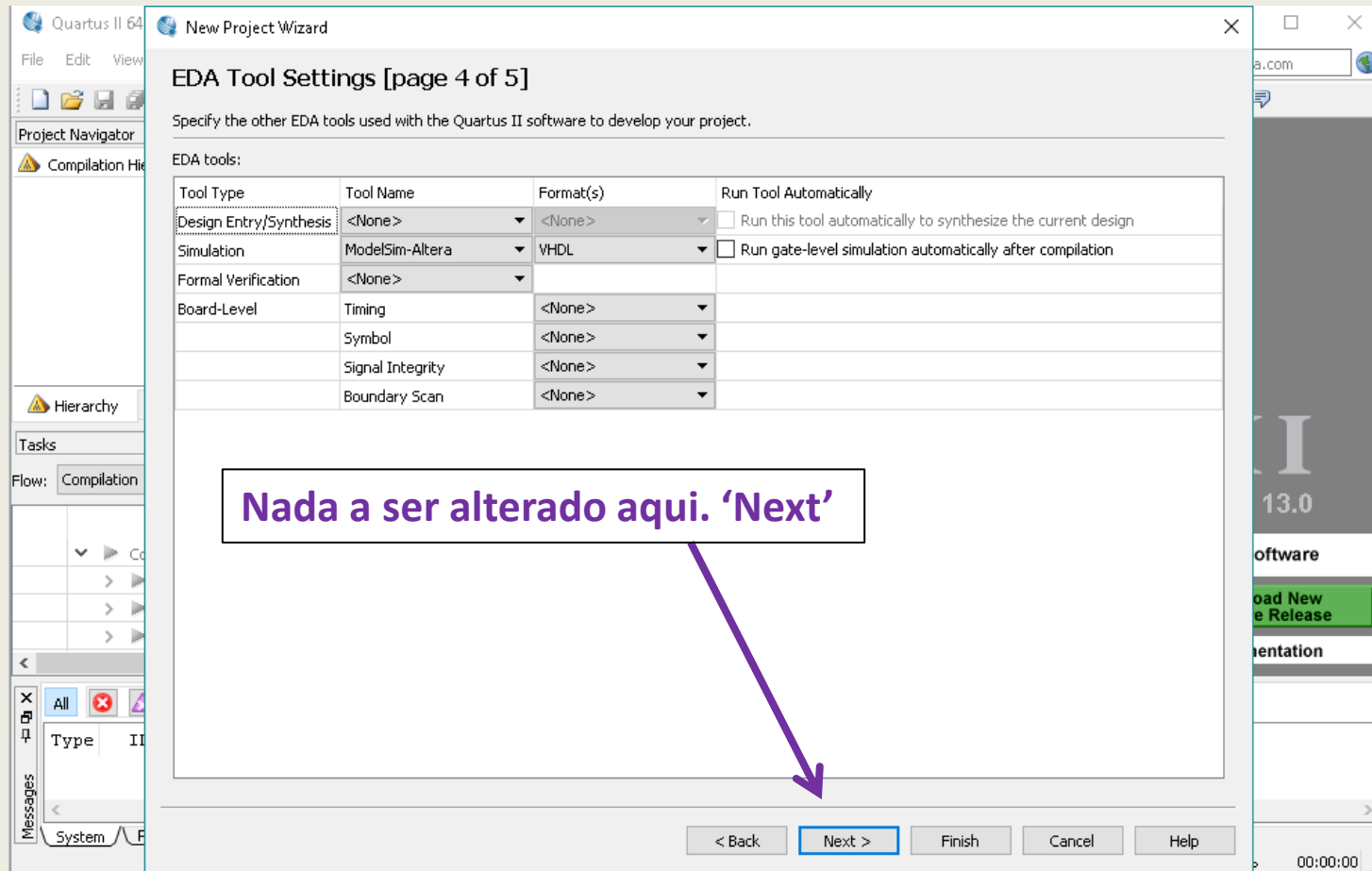
Seleção da família do FPGA DE2 que é a Cyclone II

E aqui, selecione o dispositivo EP2C35F672C6

E depois, 'Next'

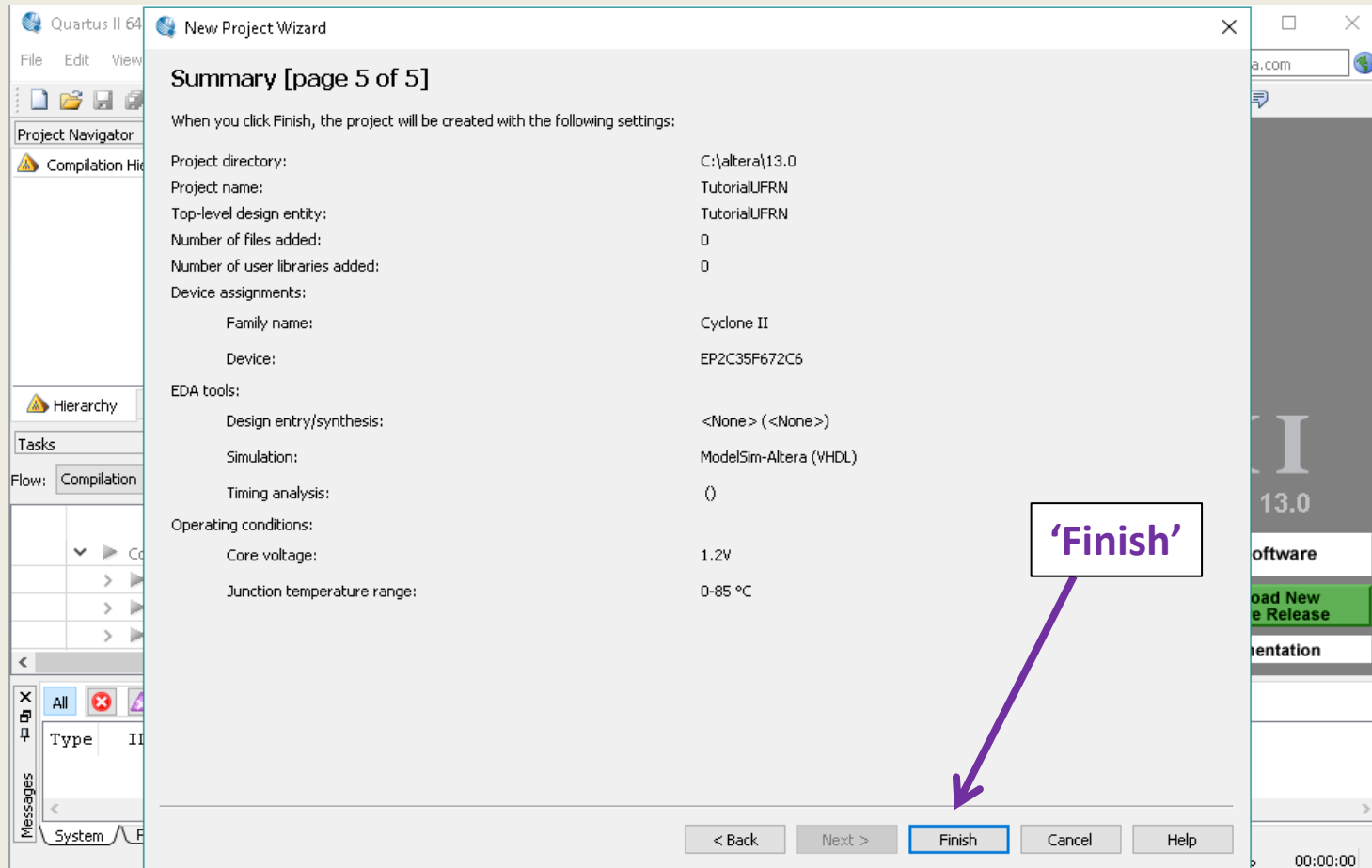
Simulando um circuito digital

1º passo: Crie um projeto



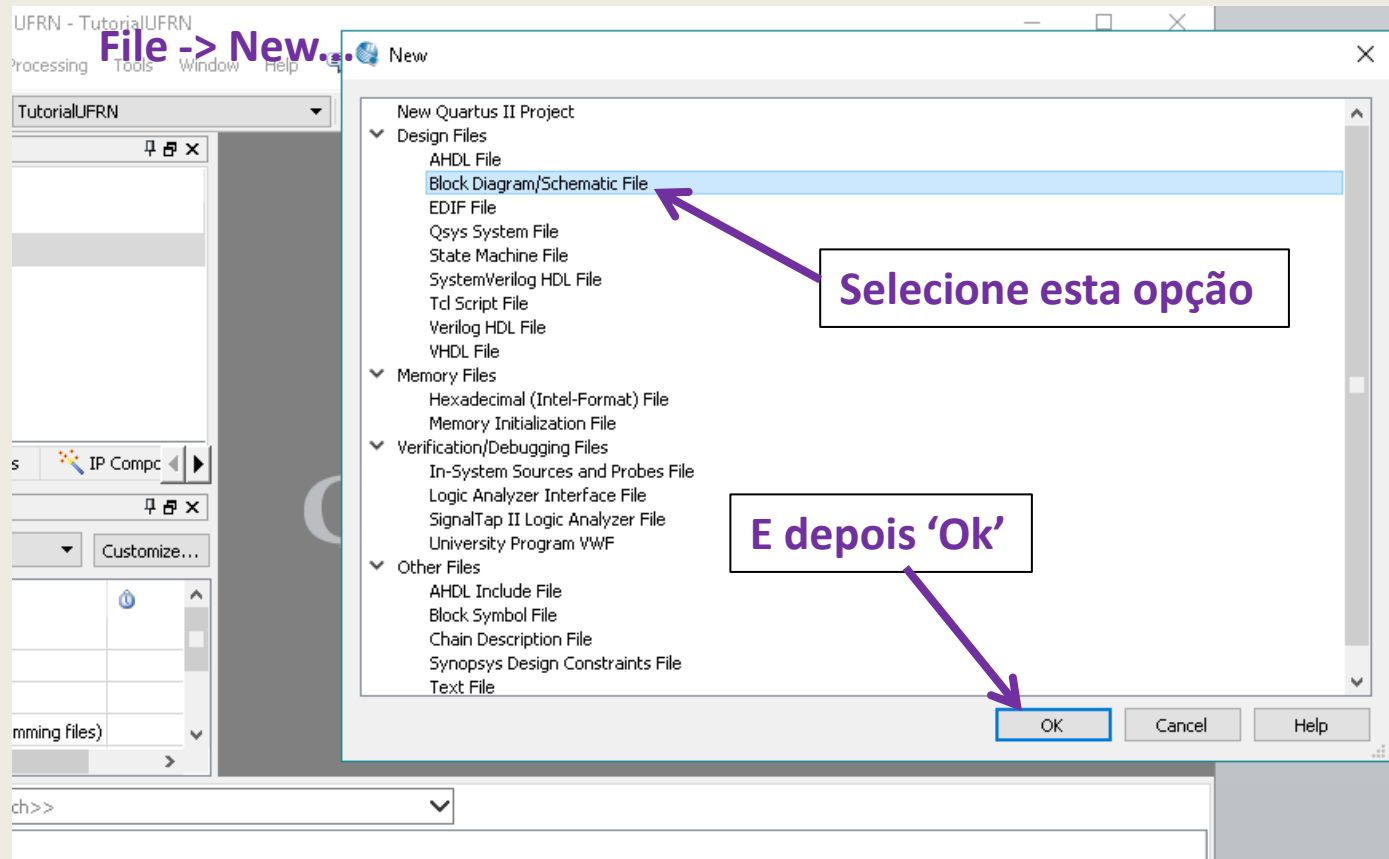
Simulando um circuito digital

1º passo: Crie um projeto



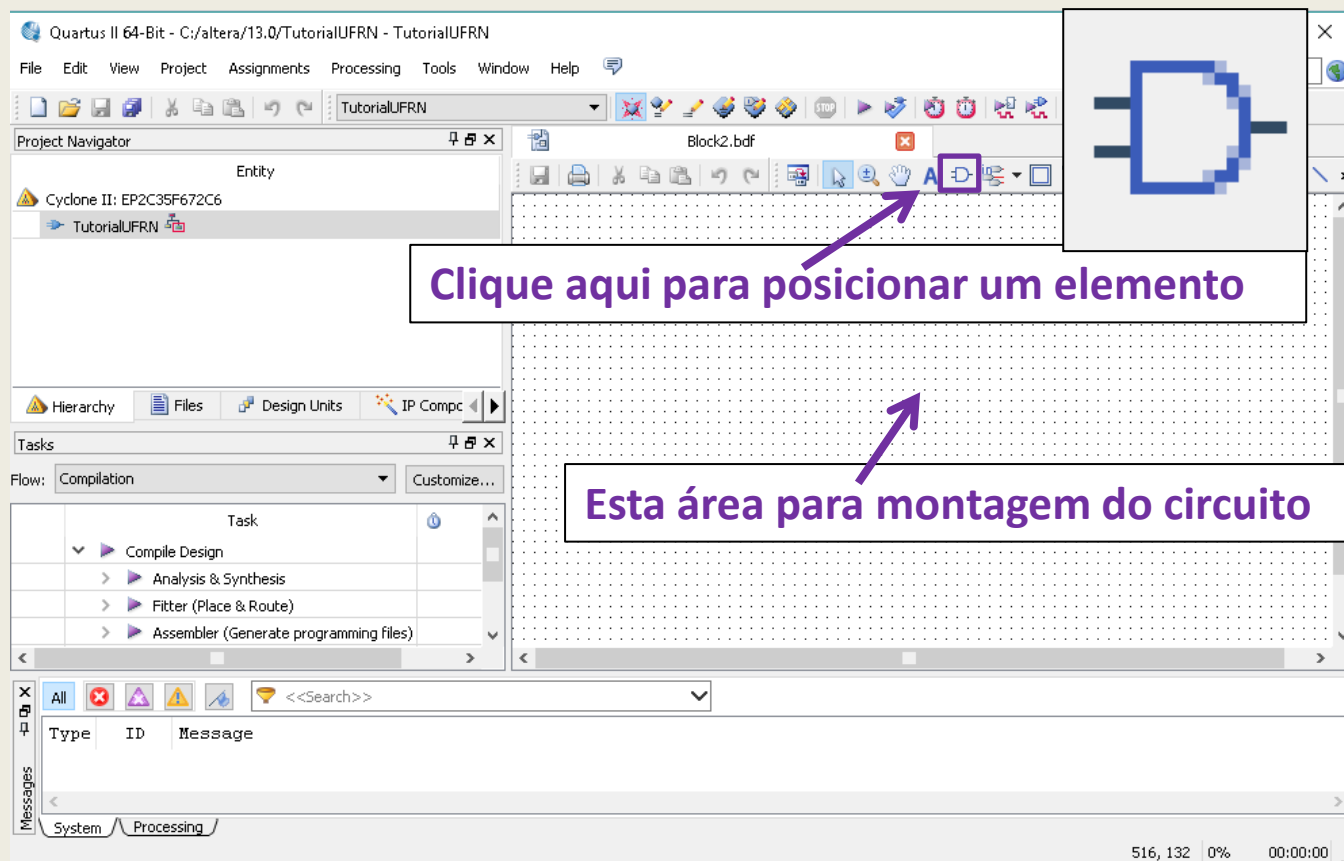
Simulando um circuito digital

2º passo: Construa o circuito



Simulando um circuito digital

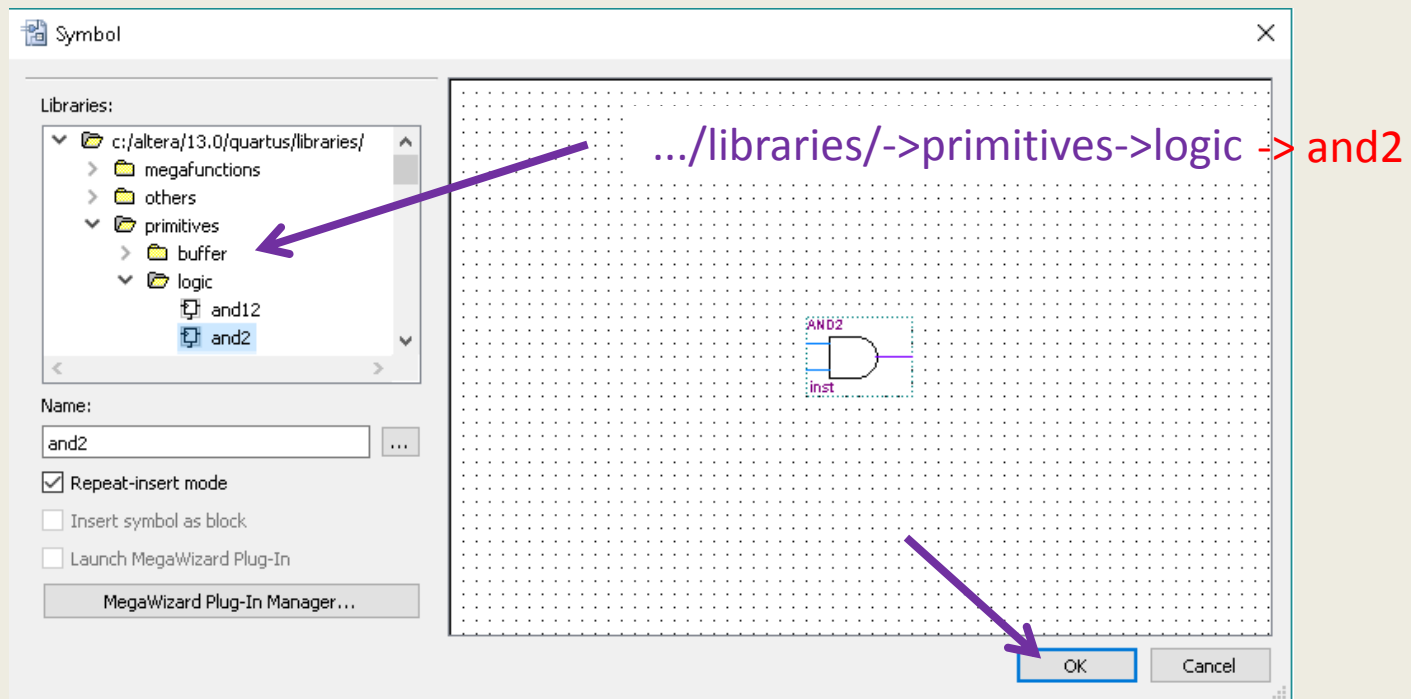
2º passo: Construa o circuito



Simulando um circuito digital

2º passo: Construa o circuito

Vamos fazer um circuito simples com porta AND de duas entradas



Simulando um circuito digital

2º passo: Construa o circuito

Quartus II 64-Bit - C:/altera/13.0/TutorialUFRN - TutorialUFRN

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity

Cyclone II: EP2C35F672C6

TutorialUFRN

Block2.bdf*

Clique aqui

in Input

out Output

io Bidir

inst

Agora vamos adicionar as entradas e saídas ao elemento.

Filter (Place & Route)

Assembler (Generate programming files)

Messages

Type ID Message

System Processing

564,262 0% 00:00:00

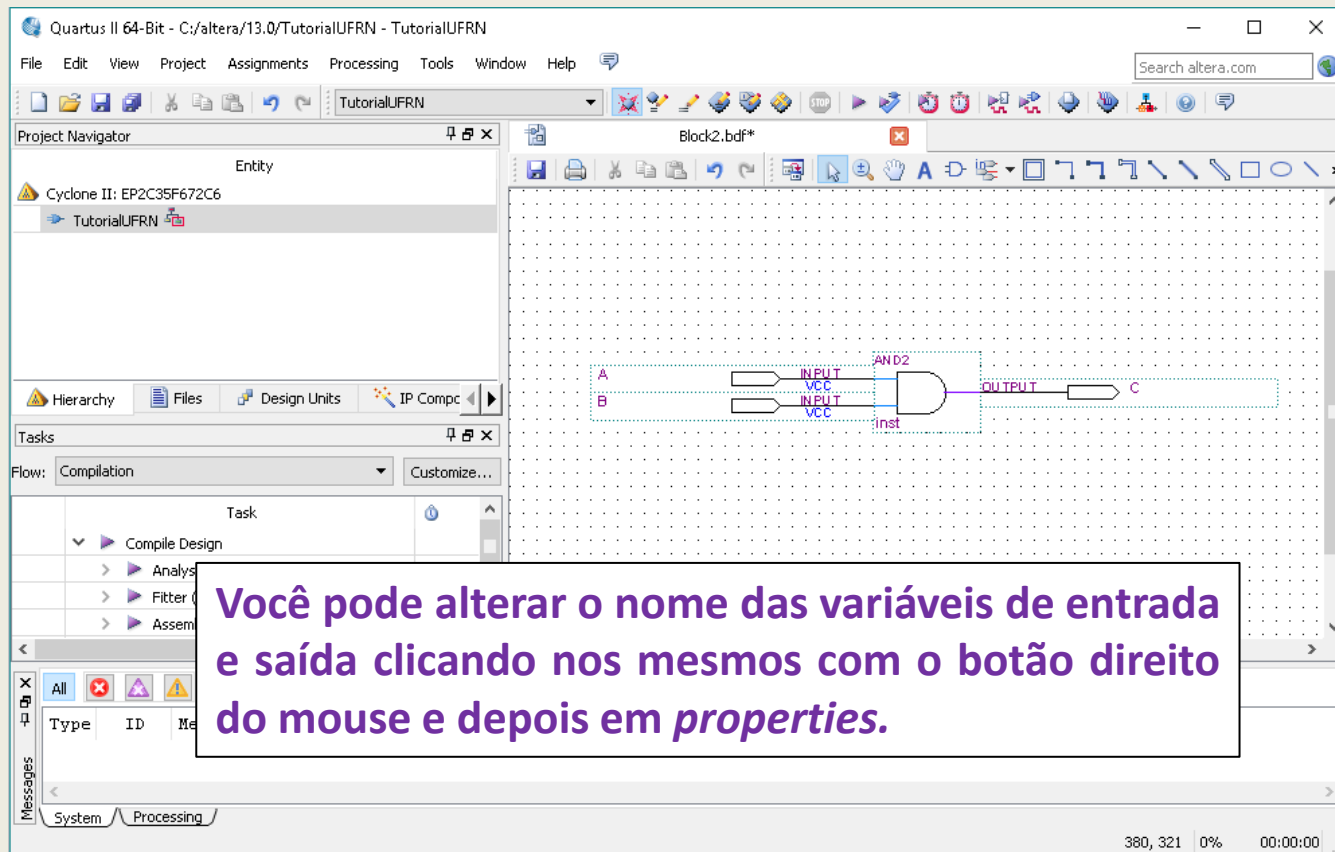
Entrada

Saída

Bidirecional

Simulando um circuito digital

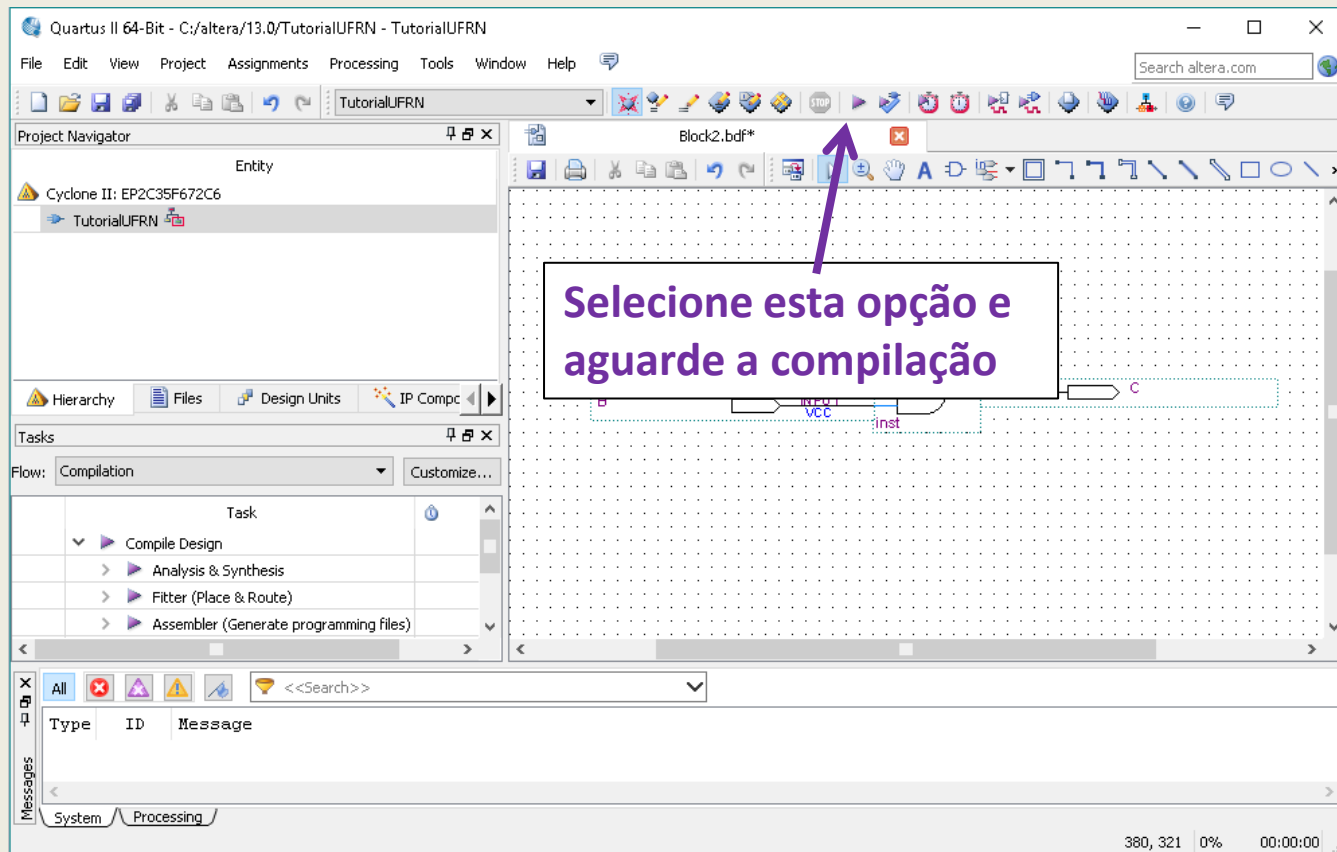
2º passo: Construa o circuito



Você pode alterar o nome das variáveis de entrada e saída clicando nos mesmos com o botão direito do mouse e depois em *properties*.

Simulando um circuito digital

3º passo: Compile o seu projeto



Simulando um circuito digital

3º passo: Compile o seu projeto

The screenshot displays the Quartus II 64-Bit IDE interface. The main window shows the 'Project Navigator' on the left, listing the project 'TutorialUFRN' and the device 'Cyclone II: EP2C35F672C6'. The 'Table of Contents' pane in the center lists the compilation flow steps: Flow Summary, Flow Settings, Flow Non-Default Global Settings, Flow Elapsed Time, Flow Overview, Flow Log, Analysis, Filter, Assembly, Timing, EDA Netlist Writer, Flow Messages, and Flow Suppressed Messages. The 'Flow Summary' window on the right provides a detailed overview of the compilation process, including the flow status, version, revision name, top-level entity name, family, device, timing models, and various resource usage statistics.

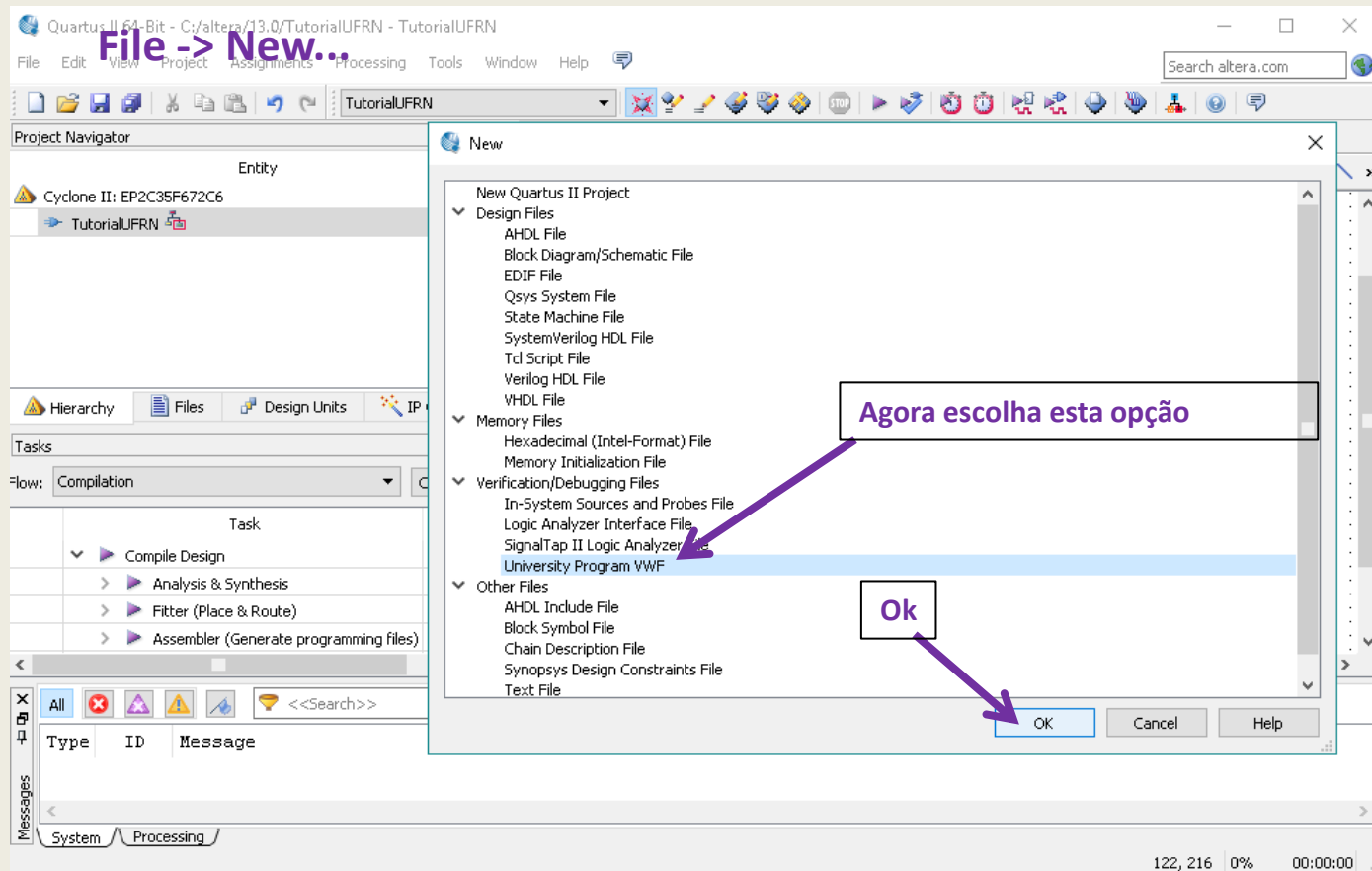
Flow Summary	
Flow Status	Successful - Fri
Quartus II 64-Bit Version	13.0.0 Build 156
Revision Name	TutorialUFRN
Top-level Entity Name	TutorialUFRN
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Total logic elements	1 / 33,216 (< 1 %)
Total combinational functions	1 / 33,216 (< 1 %)
Dedicated logic registers	0 / 33,216 (0 %)
Total registers	0
Total pins	3 / 475 (< 1 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

The 'Messages' window at the bottom shows the following message:

```
293000 Quartus II Full Compilation was successful. 0 errors, 12 warnings
```

Simulando um circuito digital

4º passo: Preparando simulação



Simulando um circuito digital

4º passo: Preparando simulação

The screenshot shows the 'Simulation Waveform Editor' window. The 'Edit -> Value' menu is open, and the 'Overwrite Clock...' option is highlighted with a red box. Below the menu, the 'Clock' dialog box is open, showing the 'Base waveform on time period' settings. The 'Period' is set to 1.0 us, 'Offset' is 0.0 us, and 'Duty cycle (%)' is 50. The 'OK' button is also highlighted with a red box.

Selezione uma entrada e depois
Edit -> Value

Base waveform on time period

Period: 1.0 us

Offset: 0.0 us

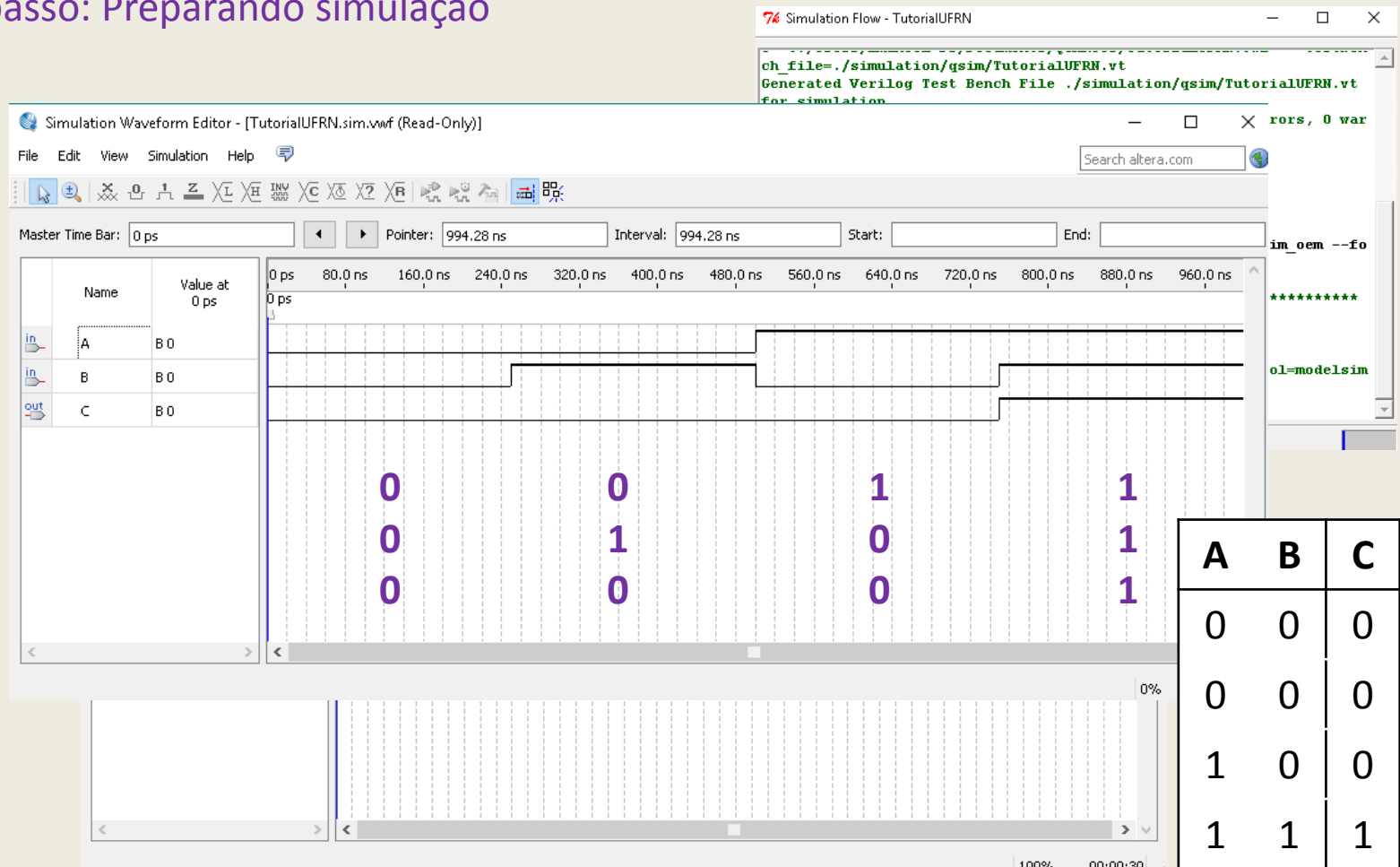
Duty cycle (%): 50

OK Cancel

Symbol	Function	Shortcut
X	Forcing Unknown (X)	Ctrl+Alt+X
0	Forcing Low (0)	Ctrl+Alt+0
1	Forcing High (1)	Ctrl+Alt+1
Z	High Impedance (Z)	Ctrl+Alt+Z
L	Weak Low (L)	Ctrl+Alt+L
H	Weak High (H)	Ctrl+Alt+H
INV	Invert	Ctrl+Alt+I
C	Count Value...	Ctrl+Alt+V
X	Overwrite Clock...	Ctrl+Alt+K
B	Arbitrary Value...	Ctrl+Alt+B
R	Random Values...	Ctrl+Alt+R

Simulando um circuito digital

4º passo: Preparando simulação

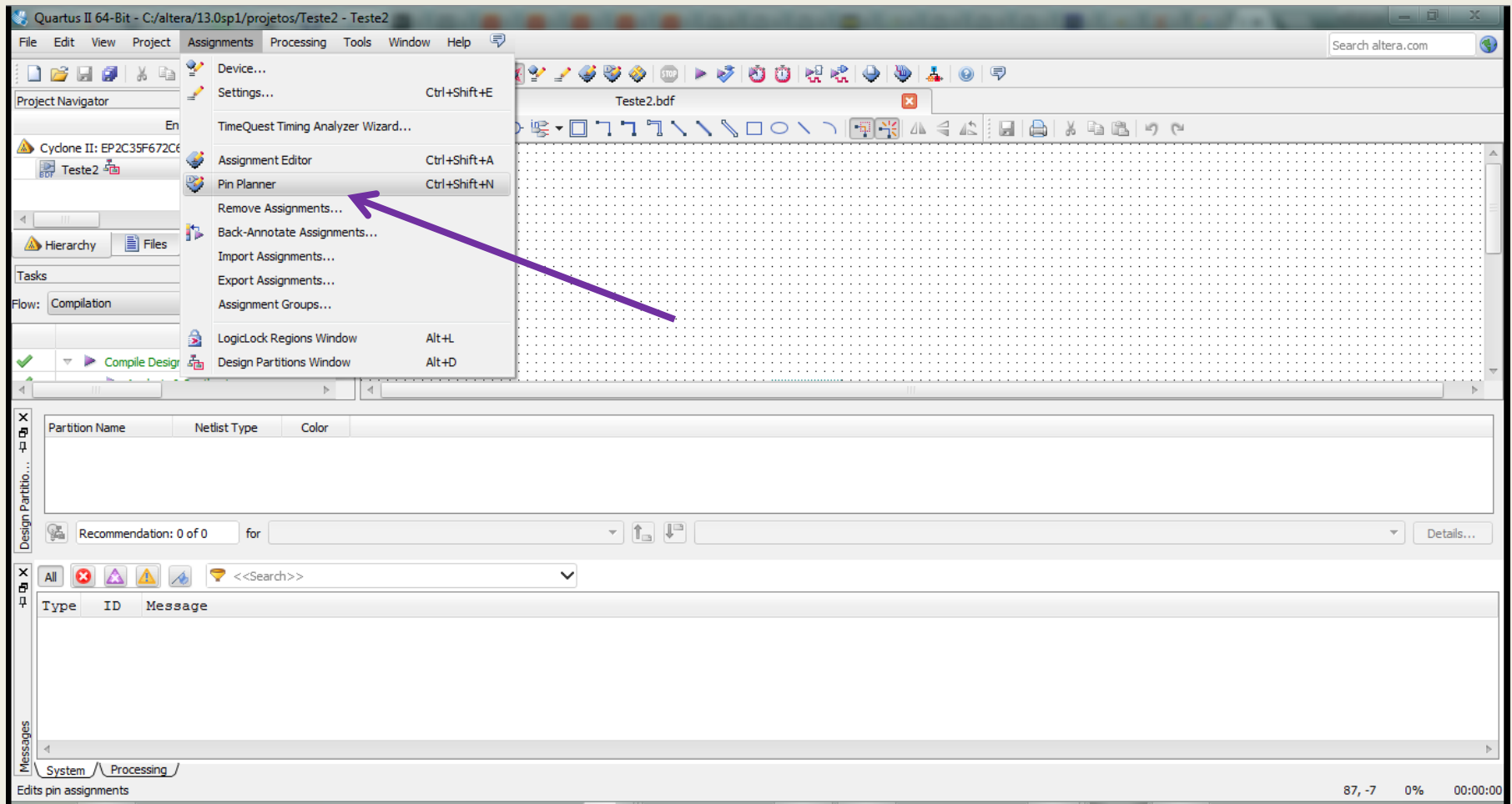


Tutorial QUARTUS

Gravando um circuito digital na placa Altera DE2

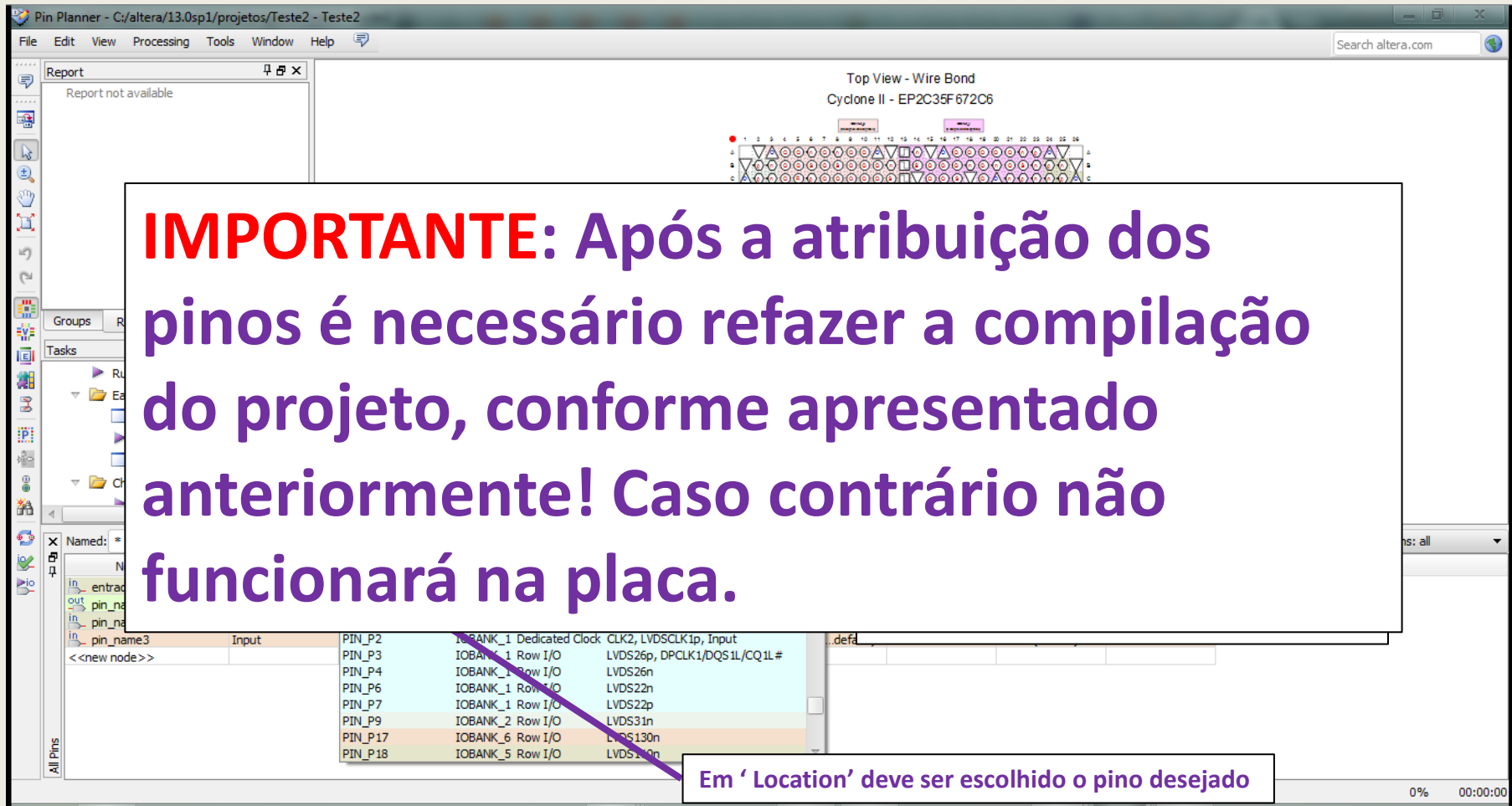
Gravando um circuito digital na placa Altera DE2

1º passo: Mapeamento das entradas e saídas
Assignments > Pin Planner



Gravando um circuito digital na placa Altera DE2

2º passo: Mapeamento das entradas e saídas



The screenshot shows the Pin Planner interface for a Cyclone II - EP2C35F672C6 device. The 'Top View - Wire Bond' is displayed. A large text overlay in the center reads: **IMPORTANTE:** Após a atribuição dos pinos é necessário refazer a compilação do projeto, conforme apresentado anteriormente! Caso contrário não funcionará na placa.

Below the overlay, the 'All Pins' table is visible, showing the mapping of user-defined pin names to the device's internal pins and I/O banks.

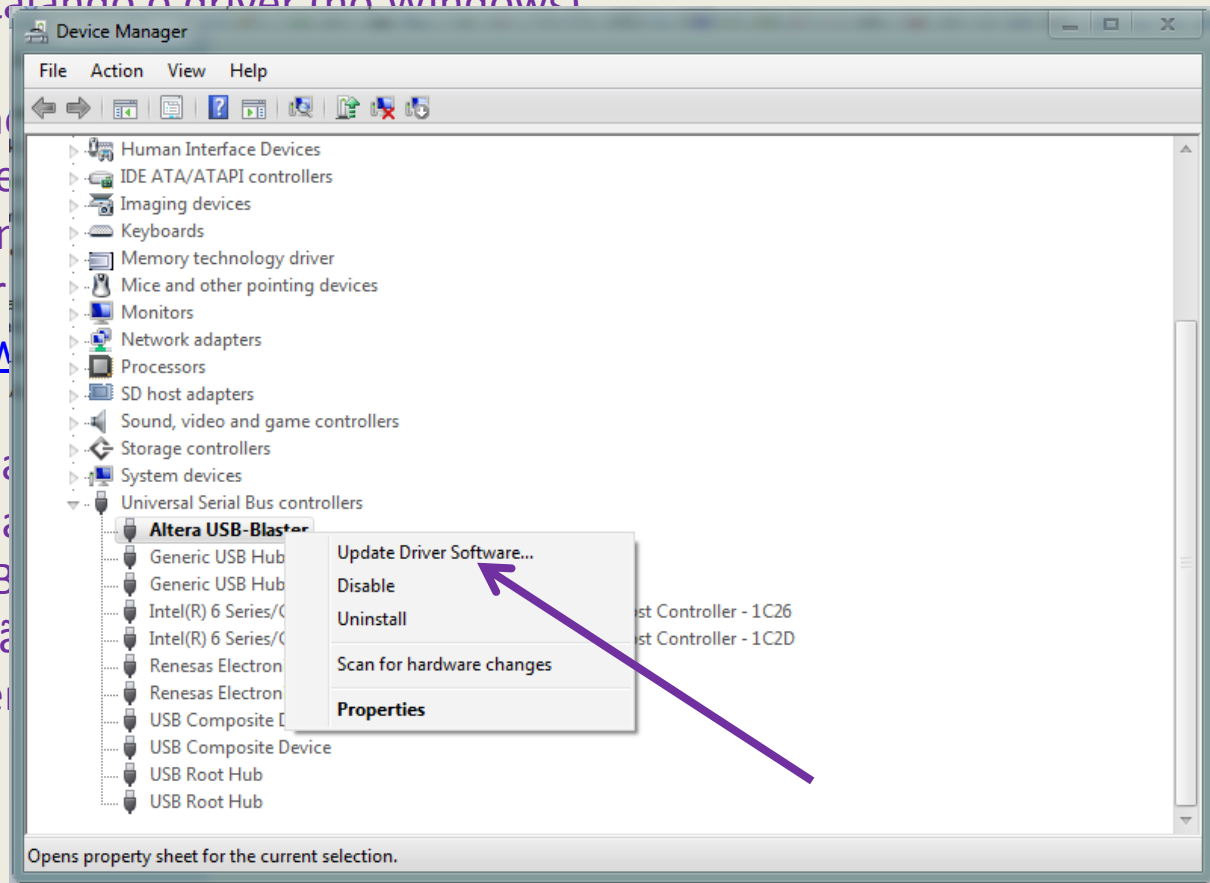
Pin Name	Direction	Internal Pin	I/O Bank	Signal
entrada	Input	PIN_P2	IOBANK_1	Dedicated Clock CLK2, LVDSCLK1p, Input
pin_name1	Output	PIN_P3	IOBANK_1	Row I/O LVDS26p, DPCLK1/DQS1L/CQ1L#
pin_name2	Input	PIN_P4	IOBANK_1	Row I/O LVDS26n
pin_name3	Input	PIN_P6	IOBANK_1	Row I/O LVDS22n
		PIN_P7	IOBANK_1	Row I/O LVDS22p
		PIN_P9	IOBANK_2	Row I/O LVDS31n
		PIN_P17	IOBANK_6	Row I/O LVDS130n
		PIN_P18	IOBANK_5	Row I/O LVDS130n

At the bottom right, a small box contains the text: Em 'Location' deve ser escolhido o pino desejado.

Gravando um circuito digital na placa Altera DE2

3º passo: Instalando o driver (no Windows)

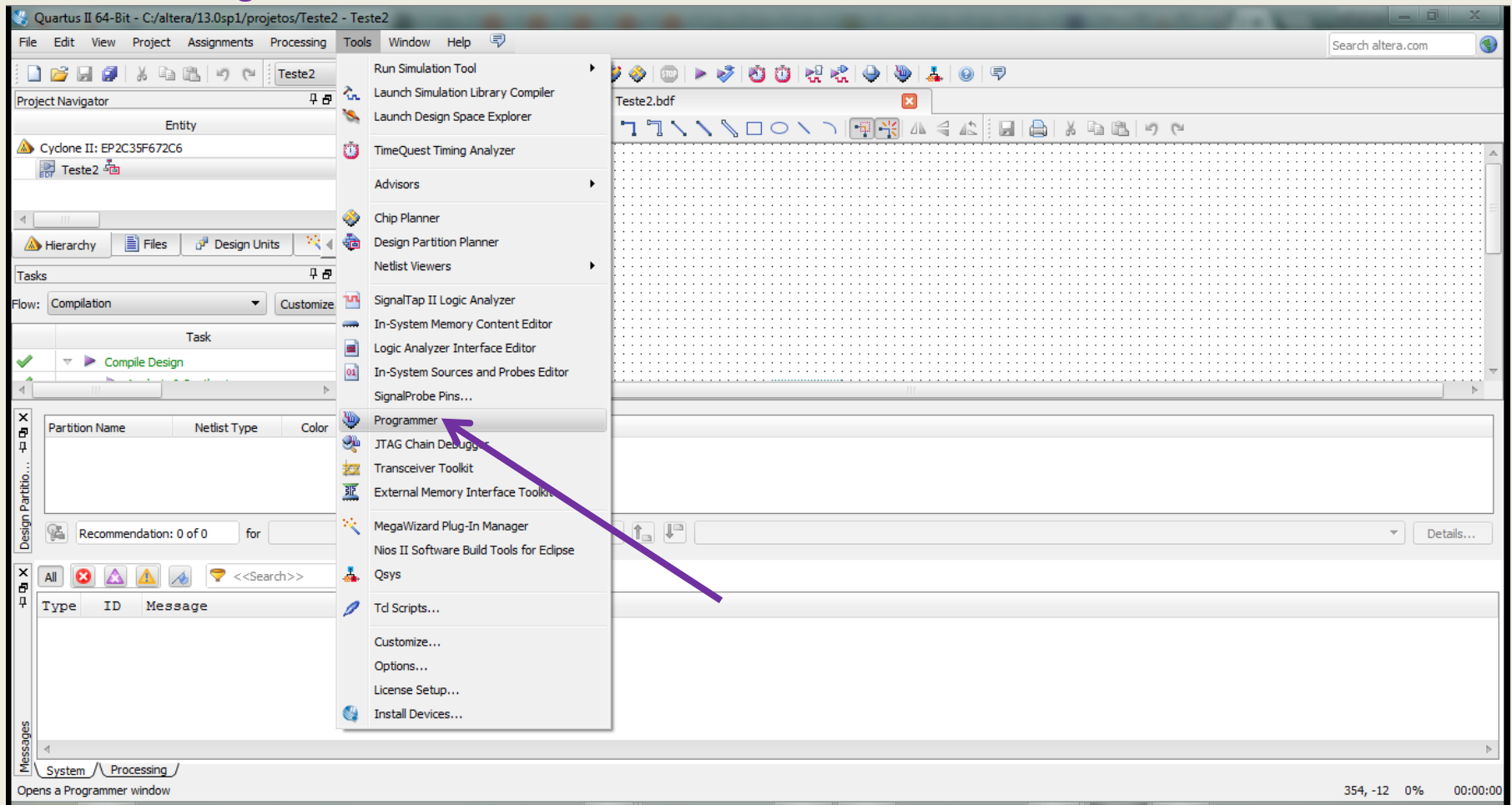
- Primeiramente, aguarda-se o Windows reconhecer o dispositivo.
- É necessário baixar o driver de <https://www.altera.com/drivers/usb/usb-blaster.zip>
- Em seguida, instalar o driver.
- Para instalar o driver, clicar com o botão direito no dispositivo e selecionar a opção 'Atualizar driver'.



Gravando um circuito digital na placa Altera DE2

4º passo: Gravando o projeto na placa

Tools > Programmer

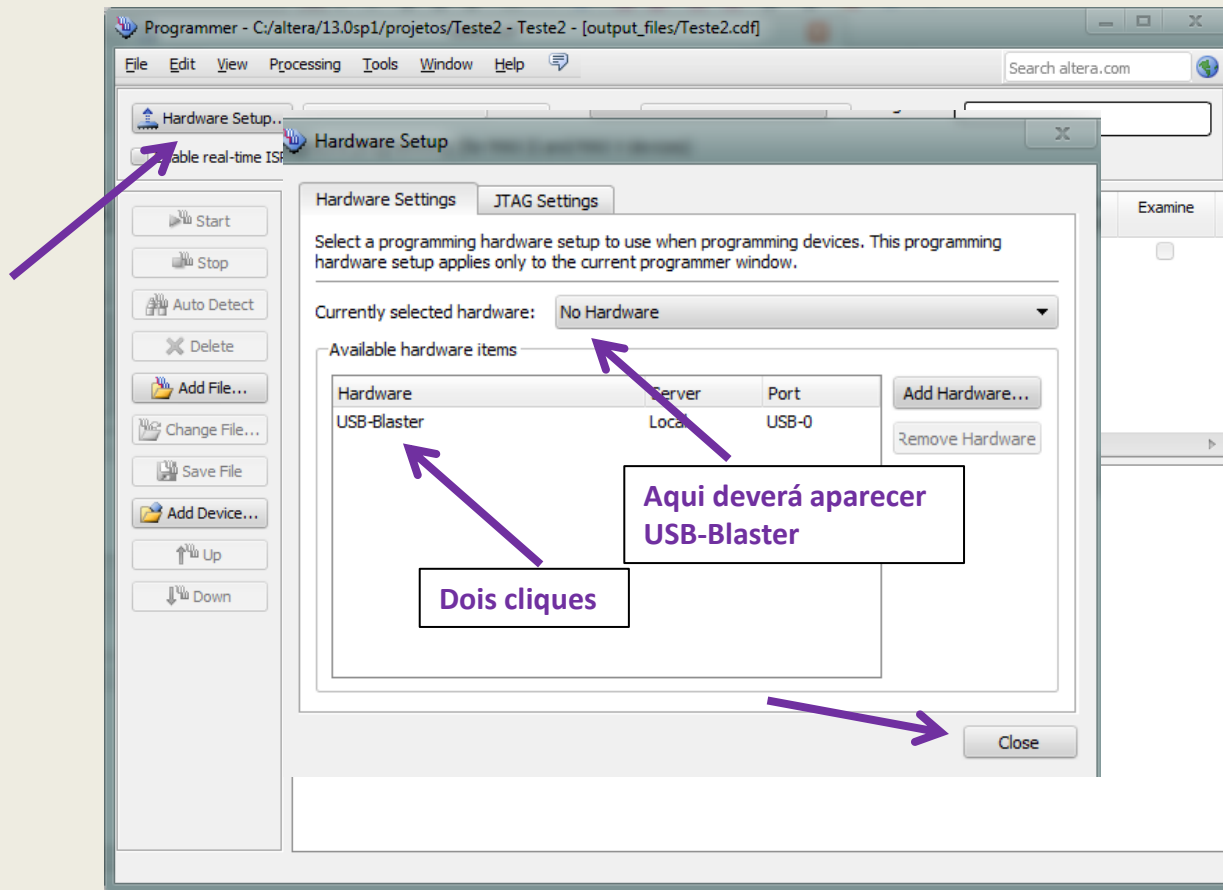


Gravando um circuito digital na placa

Altera DE2

4º passo: Gravando o projeto na placa

Clicar em Hardware Setup e escolher USB-Blaster

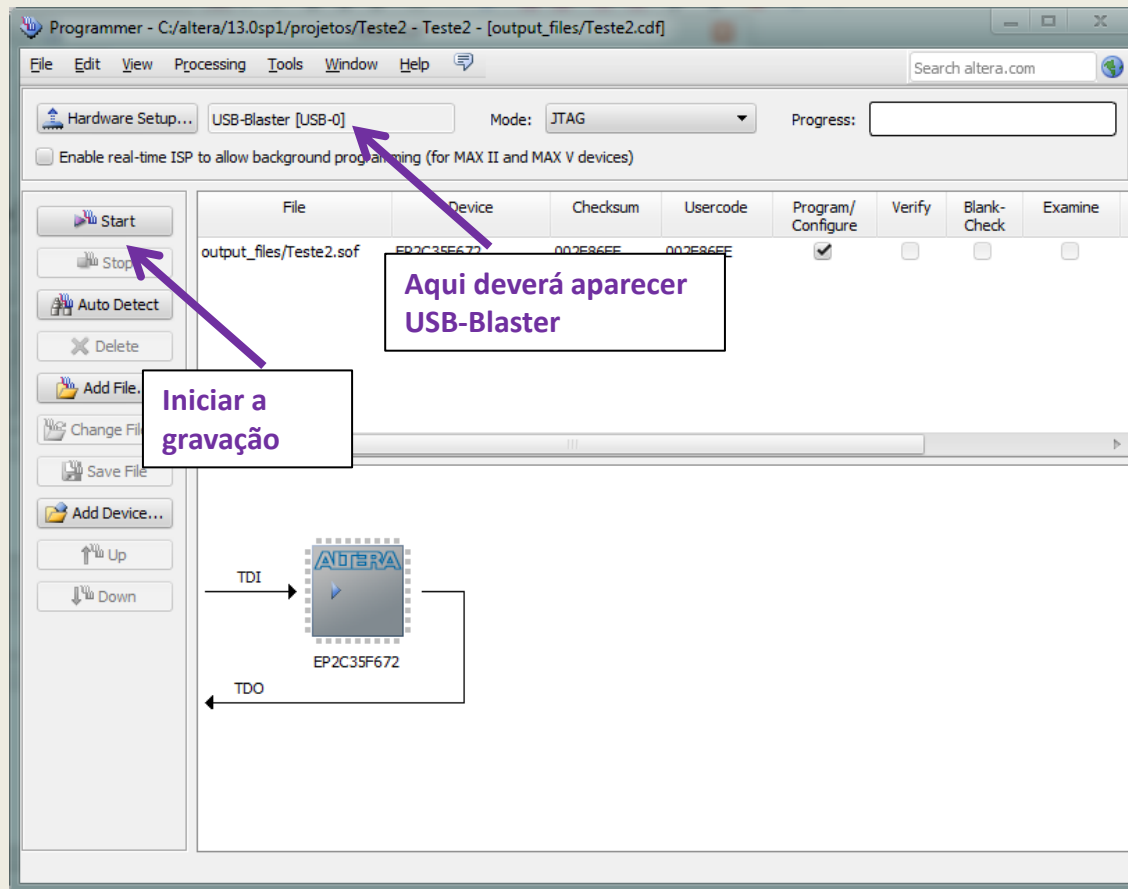


Gravando um circuito digital na placa

Altera DE2

4º passo: Gravando o projeto na placa

Clicar em Hardware Setup e escolher USB-Blaster



Gravando um circuito digital na placa Altera DE2

4º passo: Gravando o projeto na placa
Clicar em Hardware Setup e escolher USB-Blaster

