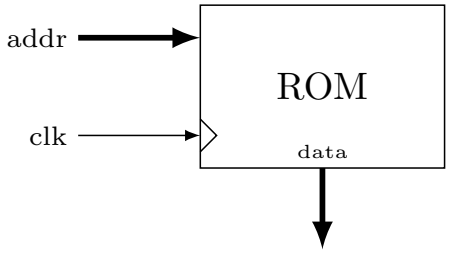
Universidade Federal do Rio Grande do Norte
Centro de Tecnologia - CT
Departamento de Engenharia Elétrica - DEE

Disciplina: ELE1717 - Sistemas Digitais
Curso: Engenharia Mecatrônica

Material de suporte - Memória ROM




```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity rom256_16b is
    port (
        clk  : in  std_logic;
        addr : in  std_logic_vector( 7 downto 0);
        data : out std_logic_vector(15 downto 0)
    );
end rom256_16b;

architecture ckt of rom256_16b is
    type memoria_rom is array (0 to 255) of std_logic_vector (15 downto 0);
    signal ROM : memoria_rom := (0      => X"0017",
                                 1      => X"3008",
                                 2      => X"0103",
                                 others => X"0000");
begin
    process (clk) begin
        if rising_edge(clk) then
            data <= ROM(conv_integer(addr));
        end if;
    end process;
end ckt;
```

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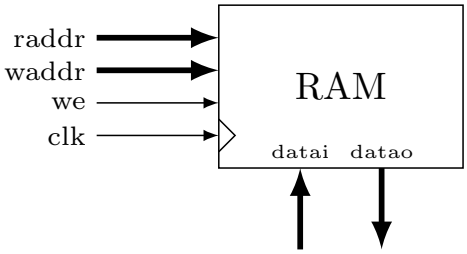
Material de suporte - Memória RAM




```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity ram256_16b is
  port (
    clk   : in  std_logic;
    we    : in  std_logic;
    raddr : in  std_logic_vector( 7 downto 0);
    waddr : in  std_logic_vector( 7 downto 0);
    datai : in  std_logic_vector(15 downto 0);
    datao : out std_logic_vector(15 downto 0)
  );
end ram256_16b;

architecture ckt of ram256_16b is

   type memoria_ram is array (0 to 255) of std_logic_vector (15 downto 0);
   signal RAM : memoria_ram := (0      => X"0017",
                                1      => X"3008",
                                2      => X"0103",
                                others => X"0000");
begin

    process (clk) begin
        if rising_edge(clk) then
            if we = '1' then
                RAM(conv_integer(waddr))<=datai;
            end if;
            datao <= RAM(conv_integer(raddr));
        end if;
    end process;

end ckt;
```