

Domain name server hierarchy

The domain name system is used to convert user-friendly domain names into IP addresses. The mapping from a specific domain name to a specific IP address is stored on an **authoritative name server**. This information is maintained by the person or organisation who manages the domain name.

When a domain name look-up is performed, many servers in the domain name server hierarchy may be used. Put the following steps into order so they correctly describe the look-up sequence.

Available items

The TLD name server is contacted and returns the details of the authoritative name server.

A server known as a recursive DNS resolver (or caching server) is contacted.

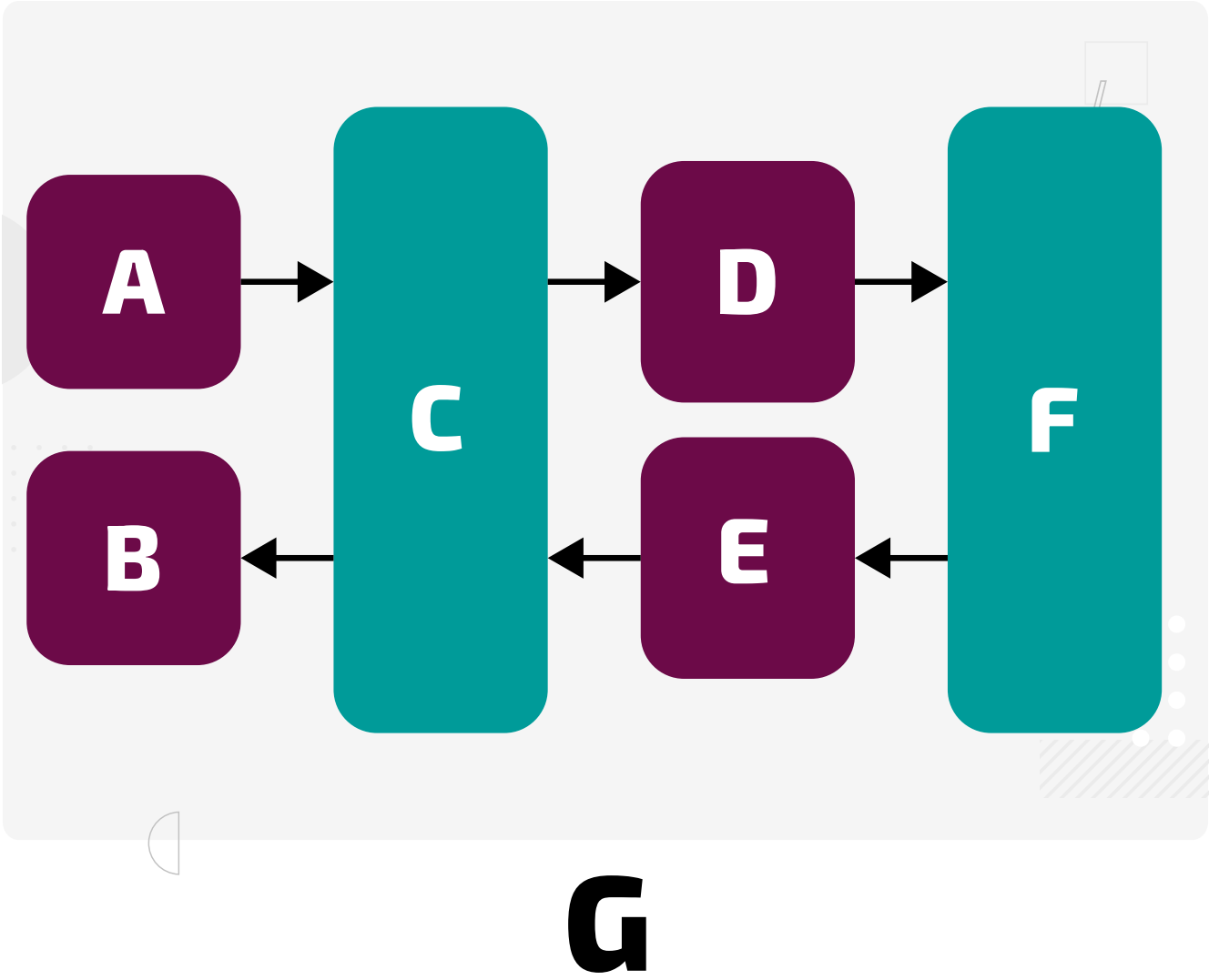
A root server is contacted and returns the details of the top level domain (TLD) name server.

If the recursive DNS resolver has the relevant IP address, it is returned to the client.

The authoritative name server is queried and returns the IP address.

Identify the machine architecture

The following diagram represents a well known computer architecture. The labels have not yet been added to identify the components, along with the label of the architecture itself. Identify the architecture and select the correct labels to complete the diagram.



☐

G	Harvard architecture
A	Input devices
B	Output devices
C	Processor
D	Instruction memory
E	Data memory
F	Secondary Storage

☐

G	Von Neumann architecture
A	Input devices
B	Output devices

☐

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C	Processor
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G	Harvard architecture
A	Output devices
B	Input devices
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D	Instruction memory
E	Data memory
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☐

G	Von Neumann architecture
A	Input devices
B	Output devices
C	Processor
D	Instruction memory
E	Data memory
F	Address bus

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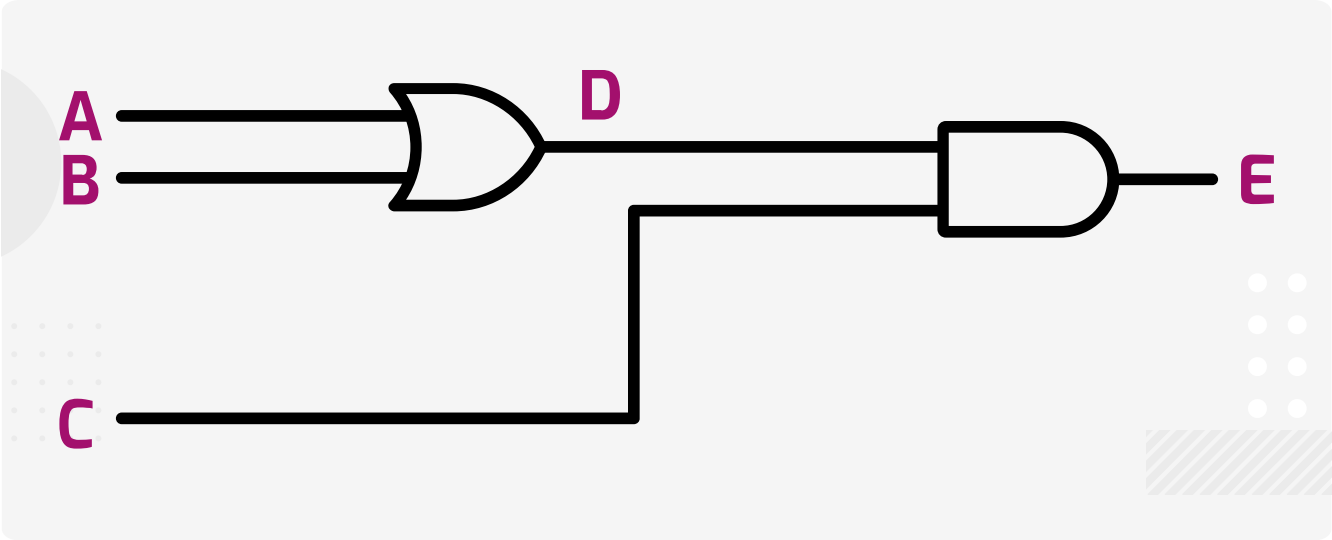
Von Neumann architecture 3

John von Neumann proposed a general purpose computer that is sometimes referred to as the "three box model". Which of the following statements provides a correct definition of a von Neumann machine?

- ☐ A processor, main memory, and secondary storage linked by a system bus
- ☐ A processor, main memory, and I/O controllers linked by a system bus
- ☐ A processor, cache, and main memory linked by a system bus
- ☐ A processor, clock, and main memory linked by a system bus

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Truth table for logic circuit 1



Circuit diagram

Fill in the missing values in columns **D** and **E** in the truth table for the logic circuit diagram above, given the following inputs:

A	B	C	D	E
0	0	0	0	0
0	0	1	0	0
0	1	0	1	0
0	1	1	1	1
1	0	0	<div></div>	0
1	0	1	1	1
1	1	0	<div></div>	<div></div>
1	1	1	1	1

Items:

0

1

Special purpose registers

Which sentence below best describes dedicated (special-purpose) registers?

- ☐ Registers that have a specific role in the fetch-execute cycle.
- ☐ Registers that is defined in software and can be customised by the user.
- ☐ Registers that are used to store the results of intermediate calculations.
- ☐ Registers that hold memory addresses.

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IP addresses 3

A Level



An IP address is split into two parts. The first part is the network ID and the second part is the host ID.

If the length of the network ID is 24 bits, how many hosts can there be on the network?

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Expression for problem 2

A library system needs to indicate if a user is allowed to borrow a book. The decision is based on several criteria.

- No one can borrow a book if they have an unpaid fine on their account.
- The maximum number of books a user can borrow is six unless they are an A level student or they have been waiting for the book for more than four weeks.

The following inputs represent the listed conditions:

D - TRUE if there is an unpaid fine on the account

M - TRUE if the account has 6 or more books on loan

S - TRUE if the account belongs to an A level student

W - TRUE if the book was requested more than 4 weeks ago

The output **B** will be **TRUE** if the student is allowed to borrow the book.

Choose the correct Boolean expression to match the logic of the problem statement.

- ☐ $B = \neg D \wedge (W \vee S \vee M)$
- ☐ $B = \neg D \wedge (W \vee S \vee \neg M)$
- ☐ $B = \neg D \vee (W \vee S \vee \neg M)$
- ☐ $B = \neg D \vee (W \vee S \vee M)$

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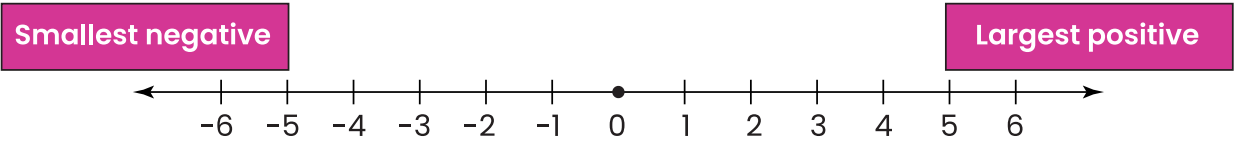
Two's complement: smallest to largest

GCSE A Level Higher

P P P P P P

The integers shown below are represented using **two’s complement**.

The smallest number is defined as the **negative number that is furthest away from 0** on the number line, and the largest number is defined as the **positive number that is furthest away from 0** on the number line.



A number line

Put the following two's complement numbers into order from **smallest** to **largest**. The smallest number should appear at the top of the list and the largest number at the bottom of the list.

Available items

11111111

01111111

01001110

11001110

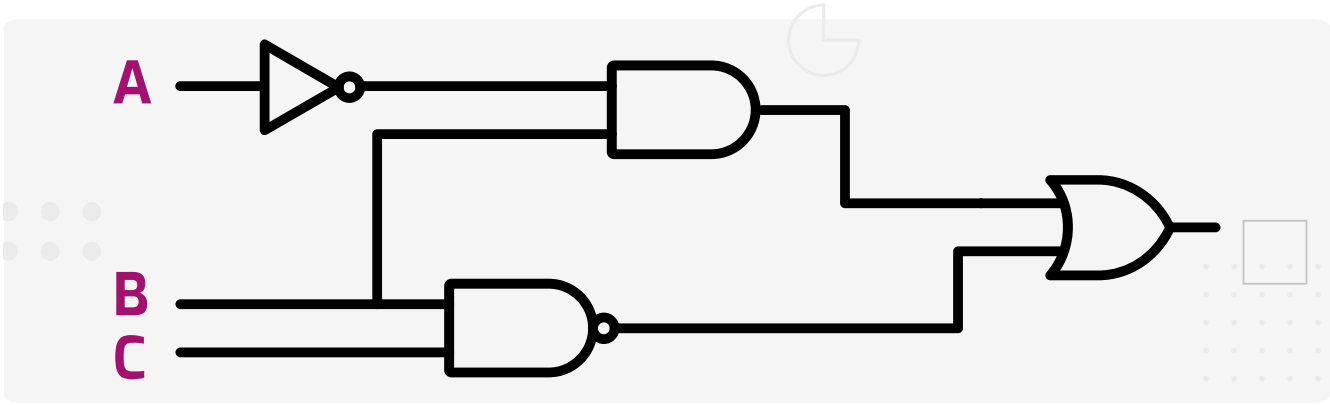
10000000

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Expression for logic circuit 1

A Level
c c

Construct the correct Boolean expression for this circuit diagram:



A circuit diagram

?

The following symbols may be useful: A, B, C

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Whole numbers: addition 1

GCSE A Level



What is the result of adding 111110_2 and 10101_2 ?

Both values are **whole numbers** (unsigned binary integers). Express your answer as 8-bit whole number in binary.



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