

Bus types



Match the bus type to its purpose. Drag a label into each row of the table below to correctly identify the bus described.

Bus	Purpose
<div></div>	Carries data to and from the processor, main memory, and input/output controllers
<div></div>	Carries the locations of stored data from the processor to main memory and input/output controllers
<div></div>	Carries signals that coordinate the operation of the components

Items:

Control

Data

Address

Bus types

There are 3 buses that make up the system bus: the data bus, address bus and control bus. Each of them carries signals appropriate to their purpose.

Which bus is the only one to carry signals **in one direction**?

Label a system diagram 1

The diagram in **Figure 1** below illustrates the connection between the core components of a computer system. Determine the correct label for each component by studying the connections carefully.

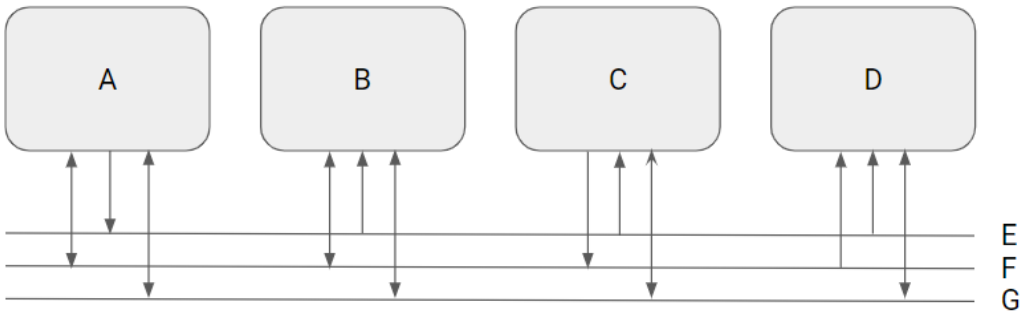


Figure 1: An unlabelled system diagram

Component	Label
A	<input type="text"/>
B	<input type="text"/>
C	<input type="text"/>
D	<input type="text"/>
E	<input type="text"/>
F	<input type="text"/>
G	<input type="text"/>

Items:

Address bus

Input controller

Control bus

Main memory

Output controller

Processor

Data bus

System bus communication



Below is a list of examples of computer system communications. Label each communication correctly depending on whether it would be serviced by the **address bus**, **control bus**, or **data bus**.

Bus	Description
<input type="text"/>	Data 01001010 being transferred from processor to main memory
<input type="text"/>	Bus busy signal
<input type="text"/>	Memory location 10110010 being sent from the processor to an I/O controller
<input type="text"/>	Interrupt request
<input type="text"/>	Instruction 10001110 being transferred from main memory to the processor

Items:

Address

Control

Data

Registers



Every processor has a set of registers. Some of them are general purpose registers and others have a specific purpose. From the following list, match each description to the appropriate register.

Bus	Description
<div></div>	Holds the address of the next instruction to be executed by the processor
<div></div>	Holds the instruction that the processor is currently executing
<div></div>	Holds the address of the memory location (in main memory) that the processor needs to access, either to read from (i.e., load data) or write (i.e., store data) to
<div></div>	Holds the data (data values or instructions) that are read from or written to the main memory
<div></div>	Holds the immediate result of an instruction executed by the ALU
<div></div>	Holds information about the result of the last instruction that the ALU executed

Items:

CIR

MBR (MDR)

PC

SR

MAR

ACC

FDE cycle components 3

What is the role of the CIR in the fetch-decode-execute cycle?

- ☐ The CIR stores the address of the instruction that needs to be fetched from the main memory so that it is decoded
- ☐ The CIR stores the address of the next instruction to be executed so that it can be fetched from the main memory
- ☐ The CIR stores temporarily data that need to be read from or written to the main memory
- ☐ The CIR stores the instruction to be decoded so that it is not overwritten by additional data fetched to the MBR(MDR)



Stages of FDE cycle 4

Select one statement that describes one operation that happens in the **fetch phase** of the fetch-decode-execute cycle.

- ☐ The arithmetic and logic unit (ALU) carries out the instruction.
- ☐ The address of the next instruction to be executed is copied to the memory address register (MAR).
- ☐ The instruction held in the current instruction register (CIR) is split into operand and opcode.
- ☐ The result of the instruction is stored in a general-purpose register or the accumulator.

FDE cycle components 4

The status register is one of the special purpose registers that have a specific role to play in the fetch-decode-execute cycle.

Select the option that describes how the status register may be used.

- ☐ Indicates if a calculation has produced an overflow error.
- ☐ Handles the interrupt that may occur due a hardware failure.
- ☐ Add the carry bit produced during the calculation of adding two numbers.
- ☐ Ensure that if a negative number is produced, it is not used as a divisor.



Stages of FDE cycle 3



Rearrange the operations below in the order they are performed during the **fetch** stage of the fetch-decode-execute cycle.

Available items

The contents of the PC are copied to the MAR

The fetched instruction is transferred to the processor using the data bus

The fetched instruction is saved in the MBR/MDR

At the same time, the contents of the PC are incremented by one

The contents of the MAR are used to access the correct location in memory

The contents of the MBR/MDR are copied to the CIR

Stages of FDE cycle 5

The instruction **LOAD 9** has been read from main memory into the Current Instruction Register (CIR). What does the control unit do next?

- ☐ Fetches the next instruction
- ☐ Executes the instruction **LOAD 9**
- ☐ Decodes the instruction **LOAD 9** so that the correct signals for this operation can be issued.

