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2.1 Simple execution, without data forwarding techniques

f)

Clock cycles	174
Instructions	61
Average CPI	2.852

Stalls: - Data	$101+0+0=101$
- Structural	0
- Branch Taken	8 101

- g) Branch not taken, visto que é sempre realizado o fetch da instrução SW \$9, mult(\$0), mesmo quando o branch é realizado.

2.2 Application of data forwarding techniques

c)	Clock cycles	136
	Instructions	61
	Average CPI	2.230

Stalls: - Data	63+0+0=63
- Structural	9
- Branch Taken	8+101=109

- d)
$$\text{SpeedUp} = \frac{2.852 \times 61}{2.230 \times 61} \approx 1.2789$$

 Houve uma melhoria em termos de performance.

2.3 Source code optimization: minimization of data and structural hazards

- a) Attach a copy of the new assembly program. código em anexo (Prag3)

c)	Clock cycles	174 127
	Instructions	61
	Average CPI	2.852 2.082

Stalls:	- Data	45+0+0=45
	- Structural	9
	- Branch Taken	8

- d)
$$\text{SpeedUp} = \frac{2.852 \times 61}{2.082 \times 61} \approx 1.3698$$

 Houve uma melhoria face ao anterior.

2.4 Source code optimization: loop unrolling

- a) Attach a copy of the new assembly program.

Código em anexo (Prog4)

- c)

Clock cycles	97
Instructions	43
Average CPI	2.256

Stalls: - Data	69+0+0=69
- Structural	9
- Branch Taken	2

- d)

$$\text{SpeedUp} = \frac{2.852 \times 61}{2.256 \times 43} \approx 1.7934$$

Houve uma melhoria a qualquer outro anterior.

2.5 Source code optimization: branch delay slot

- a) Attach a copy of the new assembly program.

Código em anexo (Prog5)

- d)

Clock cycles	110
Instructions	61
Average CPI	1.803

Stalls: - Data	36+0+0=36
- Structural	9
- Branch Taken	0

- e)

$$\text{SpeedUp} = \frac{2.852 \times \cancel{61}}{1.803 \times \cancel{61}} \approx 1.5818$$

Houve uma melhoria em relação ao 2.1 e 2.2. Contudo, é mais eficiente fazendo loop unrolling.

Table 1: Pipeline time diagram, with data forwarding techniques.

[illegible]

Table 2: Pipeline time diagram, with minimization techniques to reduce the data and structural hazards.

INSTRUCTIONS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40			
lw \$12, 0(\$1)	FD	X	M	N																																							
addi \$5, \$1		FD	X	M	N																																						
addi \$1, \$1, 8			FD	X	M	N																																					
mul \$12, \$12, \$1				FD	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
add \$9, \$9, \$12					FD	X																																					
bne \$6, \$5, loop						FD	X																																				
sw \$9, mult(\$1)							FD	X																																			

Table 4: Pipeline time diagram: usage of branch delay slot techniques to reduce the control hazards.

INSTRUCTIONS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40			
lw \$12,0(\$1)	FD							X	MW			FD																															
addi \$5,\$5,1	F							D	X	MW		F																															
doaddi \$1,\$1,8								F	D	X	MW																																
dmul \$12,\$12,\$1								F	D	X	X	X	X	X	X	MW	F																										
lwr \$6,\$5,loop																																											
doadd \$9,\$9,\$12																																											
																	</																										