Isabella Nicole Zaens

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EDUCATION

The University of Texas at Austin   August 2022 - May 2026
B.S. Electrical and Computer Engineering

Relevant Coursework
Upcoming Spring 2025: Analog Circuits Lab, Embedded Systems Design Lab, Data Science Lab
Completed: Computer Architecture, Embedded Systems, Algorithms, Digital Logic, Circuit Analysis and Design, Probability and Random Processes, Linear Systems and Signals, Vector Calculus, Discrete Mathematics

EXPERIENCE

Incoming Product Engineering Intern, Texas Instruments   May 2025 - August 2025

Product Test Engineering Intern, AMD   May 2024 - August 2024
- Conducted system-level testing for next-generation Radeon GPUs, ensuring functionality and performance standards
- Debugged and characterized products to assess performance, process, and test sensitivities
- Performed yield analysis using industry-standard tools to support yield debug and failure analysis
- Developed multiple scripts and tools to automate release notes generation and publication

Research Assistant, ReNeu Robotics Lab   September 2023 - August 2024
- Developed embedded software for an EMG-driven hand exoskeleton that aids in spinal cord injury rehabilitation
- Optimized performance of data acquisition system using C++, EtherCAT, ESI, and SOEM
- Created documentation and wiring diagrams to help build a new exoskeleton
- Developing a new version of the exoskeleton by researching and integrating advanced hardware and software

PROJECTS

Two-Player Space Invaders
- Developed a two-player Space Invaders game on a TM4C microcontroller using C++ and ARM assembly
- Implemented version control and peer-programming techniques for code efficiency and collaborative development
- Designed custom game controller PCB, sampled analog joysticks (ADC), displayed on LCD
- Incorporated interrupts for dynamic sound effects, outputted through DAC

LC-3b Simulator
- Developed LC-3b simulator using C and LC-3b programming languages, microcode, and a control store
- Equipped with instruction execution, branching, virtual memory management, and interrupt and exception handling
- Added support for four types of exceptions: unaligned access, protection, page fault, and unknown opcode
- Modified existing datapath, state diagram, and microsequencer

FPGA-Based Stopwatch and Timer
- Designed a programmable stopwatch/timer on the Basys3 FPGA with four counting modes using RTL methodology
- Developed a high-level state machine and datapath architecture to control operations and optimize efficiency
- Implemented in Xilinx Vivado using behavioral modeling, clock division techniques, and a 7-segment display

SKILLS AND CERTIFICATIONS

Software: C/C++, Java, Python, Verilog, ARM Assembly, MATLAB, SQL, R, HTML/CSS, Javascript, Tableau
Hardware: Circuitry, Oscilloscopes, FPGA, PCB Design
Tools: Unix/Linux, Keil, VSCode, Vivado, KiCad, EAGLE, AD2 Waveforms, AutoCAD, Fusion 360
Certifications: Google Data Analytics