Isabella Nicole Zaens

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EDUCATION

University of Texas at Austin **Aug. 2022 - May 2026**
B.S. in Electrical and Computer Engineering *Austin, TX*

RELEVANT COURSEWORK

Graduate CMOS VLSI Design, Tactile Sensing for Robotics
Undergraduate Computer Architecture, Digital Logic Design, Operating Systems, Data Science Lab, Embedded Systems Design Lab, Linear Systems and Signals, Discrete Mathematics

PROFESSIONAL EXPERIENCE

Incoming Digital IC Design Engineering Intern **May 2026 - Aug. 2026**
Texas Instruments *Dallas, TX*

High-Voltage Driver and Bias Test Engineering Intern **May 2025 - Aug. 2025**
Texas Instruments *Dallas, TX*
- Developed a C++ diagnostic program for the handler interface board of an isolated DC/DC module on ETS-364 ATE
- Characterized restart behavior and body diode of isolated DC/DC modules across temperature for product qualification
- Executed high voltage/temperature tests on half-bridge driver lead frames, analyzing leakage current and arcing behavior
- Automated repetitive tasks with Python scripts, improving accuracy and workflow efficiency

GPU System-Level Test Engineering Intern **May 2024 - Aug. 2024**
AMD *Austin, TX*
- Executed system-level tests in Java on the V93K ATE for Radeon GPUs for production and characterization flows
- Characterized performance by generating Schmoo plots across voltage, frequency, and temperature corners
- Examined GPU IP blocks, including PCIe, VCE/VCN, and memory controller, to support silicon debug and validation
- Automated test flows and release notes generation using Python, Bash, and Gradle, reducing manual workload

Undergraduate Research Assistant **Sep. 2023 - Aug. 2024**
Rehabilitation and Neuromuscular (ReNeu) Robotics Lab *Austin, TX*
- Researched and developed embedded software for an EMG-driven hand exoskeleton to assist spinal cord injury patients
- Optimized EMG data acquisition using C++, EtherCAT, ESI, and SOEM, enabling real-time signal processing
- Integrated advanced hardware and software to improve exoskeleton performance based on research findings

PROJECTS

SoC SSP and WISHBONE Bus Controller – RTL Design
- Designed an 8-bit synchronous serial port (SSP) in Verilog and verified functionality using testbenches in Synopsys VCS
- Developed a 32-bit WISHBONE bus controller to interface SSP with memory and ARM-2 microprocessor modules
- Implemented a clock management unit to sync data flow for all modules and handle interrupts on SSP FIFO overflow
- Imported synthesized Verilog design into Synopsys Design Vision for area and timing optimizations
- Performed automatic place-and-route (APR) in Cadence Innovus using a 45nm PDK to generate the physical SoC layout

16-bit RISC ALU Custom IC Design
- Designed gate-level schematic and layout of a 16-bit RISC ALU with arithmetic, logic, compare, and shift functions
- Implemented a 16-bit radix-2 Kogge–Stone adder and barrel shifter for fast arithmetic and shift functions
- Performed APR in Cadence Innovus and conducted post-layout static timing analysis (STA) using Synopsys PrimeTime
- Verified functionality with NC Verilog and optimized the critical path via fanout reduction and bubble pushing

SKILLS

Software Python, C/C++, Java, Verilog, ARM Assembly, Bash, Gradle, MATLAB
Hardware Signal Generators, Oscilloscopes, Microcontrollers, PCB Design
Tools Git, Linux, VSCode, KiCAD, LTSpice, Fusion 360, AutoCAD
Cadence: Virtuoso, Innovus, Spectre, NC Verilog | *Synopsys:* VCS, DV, PrimeTime, HSPICE