ISABELLA NICOLE ZAENS

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EDUCATION

The University of Texas at Austin — Austin, TX
B.S. Electrical and Computer Engineering — *Aug 2022 - May 2026*

COURSEWORK

Fall 2025: CMOS VLSI (graduate-level), Tactile Sensing for Robotics (graduate-level), Senior Capstone
Relevant: Computer Architecture, Embedded Systems, Digital Logic Design, Circuits, Microelectronics, Signal Processing, Algorithms, Machine Learning and Neural Networks

EXPERIENCE

Texas Instruments | Dallas, TX — *May 2025 - Aug 2025*
Test Engineering Intern - High Voltage Drivers and Bias
• Developed a C++ diagnostic program for the handler interface board of an isolated DC/DC module on ETS-364 ATE
• Characterized restart behavior and body diode of isolated DC/DC modules across temperature for product qualification
• Executed high voltage/temperature tests on half-bridge driver lead frames, analyzing leakage current and arcing behavior
• Automated repetitive tasks with four Python/Linux scripts, improving accuracy and workflow efficiency

Advanced Micro Devices (AMD) | Austin, TX — *May 2024 - Aug 2024*
GPU System-Level Test Intern
• Executed system-level validation of Radeon GPUs on ATE-93K, ensuring reliable production and characterization flows
• Debugged silicon and characterized performance metrics and process variation across various test conditions
• Automated test flows and release notes generation using Bash, Python, Java, and Gradle, reducing manual workload
• Set up devices under test and independently ran system-level tests to support debug and accelerate test timelines

Rehabilitation and Neuromuscular (ReNeu) Robotics Lab | Austin, TX — *Sept 2023 - Aug 2024*
Undergraduate Research Assistant
• Researched and developed embedded software for an EMG-driven hand exoskeleton to assist spinal cord injury patients
• Optimized EMG data acquisition using C++, EtherCAT, ESI, and SOEM, enabling real-time signal processing
• Integrated advanced hardware and software to improve exoskeleton performance based on research findings
• Created wiring diagrams and documentation for integration, delivered to Sony for next-generation exoskeleton

PROJECTS

4-bit SRAM Design and Characterization
• Designed custom 4-bit SRAM cell at transistor level in Cadence Virtuoso: schematic, layout, parasitic extraction
• Characterized propagation delay through post-layout HSPICE simulations across varying input slews and output loads
• Modeled 32x32 SRAM array with RC delay model for worst-case access time analysis using Spectre simulations
• Optimized layout for low power and area efficiency while maintaining stable read/write performance

LC-3b Microarchitecture Simulator
• Built a cycle simulator for the LC-3b microarchitecture using C and LC-3b assembly language
• Implemented arithmetic and logic operations, branching, and exception handling (unaligned access, protection fault, etc.)
• Designed a microsequencer to drive the state machine, supporting little-endian memory and instruction decoding
• Added virtual memory via a one-level page table and modified the datapath and control logic to support pipelining

FPGA-Based Stopwatch and Timer
• Designed a programmable stopwatch/timer on the Basys3 FPGA with four counting modes using Verilog and RTL
• Developed a high-level state machine and datapath to control operations and optimize efficiency
• Implemented in Xilinx Vivado using behavioral modeling, clock division, and a 7-segment display

SKILLS

Software: Java, Python, C/C++, Verilog, Bash, ARM Assembly, MATLAB
Hardware: Signal Generators, Oscilloscopes, Microcontrollers, PCB Design, High Voltage/Temperature Testing
Tools: Linux, Git, VSCode, Cadence Virtuoso, Spectre, HSPICE, KiCAD, LTSpice, Fusion 360, AutoCAD