电子技术
Introduction to Electronics

By Bao Qilian
鲍其莲

Chapter 7 Flip-Flops

- *Objectives*
  - Latches
  - Edge-triggered Flip-Flops
    - S-R FF
    - D FF
    - J-K FF
    - T FF
  - One shot
  - 555 timer
- *Reading assignment*
  p359-p397

- Logic circuits
  - Combinational Circuits
  - Sequential Circuits

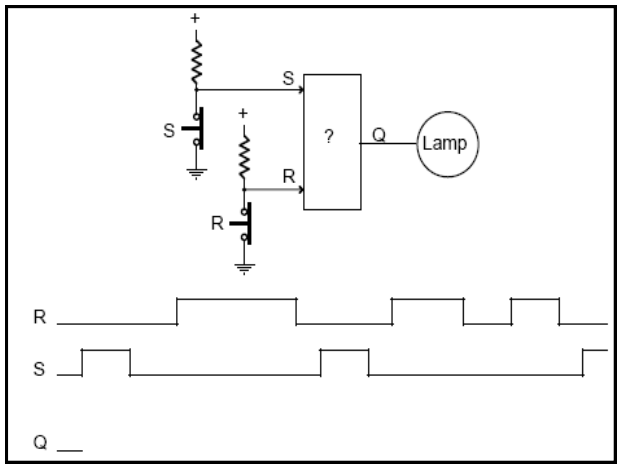
Basic Block ⇒ Flip-Flops

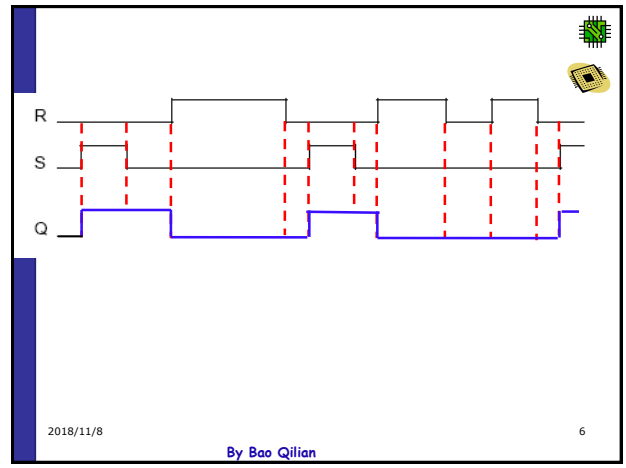
Problem

Design a network to control a lamp from two push button switches labeled S and R.

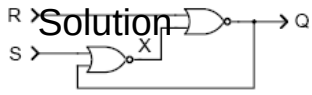
- If we push switch S the light should turn on. If we then release S, the light should stay on.
- If we push switch R, the lamp should turn off and stay off after releasing R.

Assume that both S and R are not pushed at the same time.





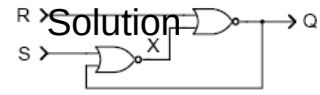
Solution



R	S	X	Q
0	0		
0	1		
1	0		
1	1		

Q=0 ⇒ $X = ?$, $Q = ?$

Solution



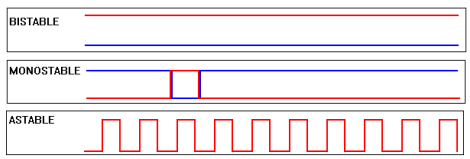
R	S	X	Q
0	0	1	0
0	1	0	1
1	0	1	0
1	1	0	0

Q=0 ⇒ $X = ?$, $Q = ?$

$$X = \overline{S + Q}$$

$$Q = \overline{R + X} = \overline{R + \overline{S + Q}}$$

- Bistable devices have two stable states, called SET and RESET. They are used as storage devices.
- Monostable devices (monostable trigger, one-shot) have one stable state. They are used as timers.
- Astable devices (multivibrator) do not have stable state. They are used as waveform

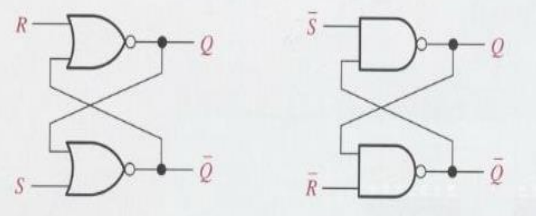


7.1 Latches

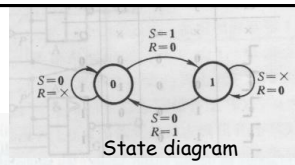
- The *latch* (锁存器)is a type of temporary device that has two stable states (*bistable*) and is normally placed in a category separate from that of *flip-flops*.
- The difference between latches and flip-flops is the *method used* for changing their states.

- *Latches*
  - S-R (Set-Reset) Latch
  - D (Delay) Latch
  - J-K Latch
  - T (Toggle) Latch

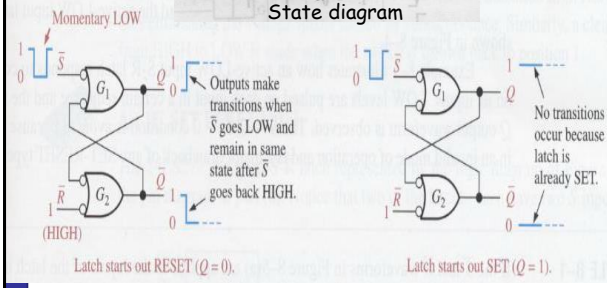
1 S-R (Set-Reset) Latch

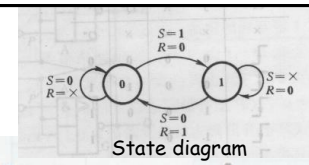


(a) Active-HIGH input S-R latch (b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

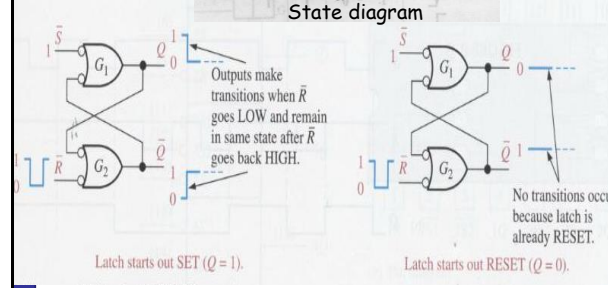


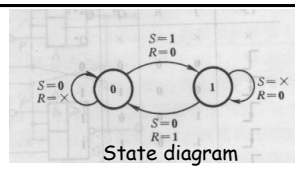
State diagram



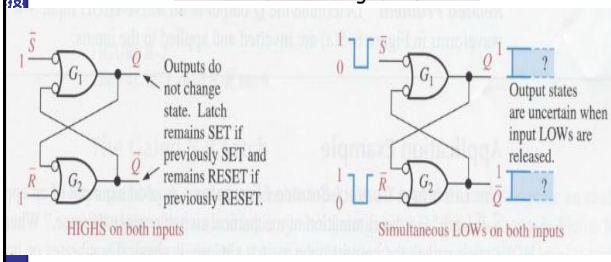


State diagram





State diagram



The Invalid Operation

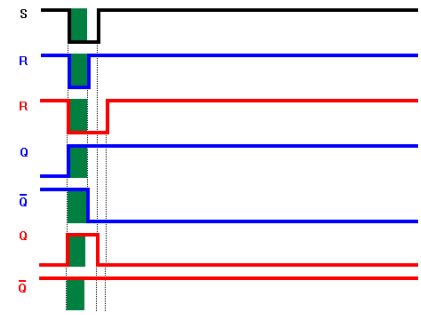
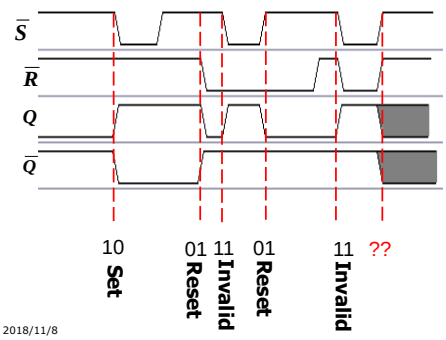


Figure 801 Outputs are uncertain when input LOWs died out

Truth Table

Inputs $\bar{S}$	Inputs $\bar{R}$	Outputs Q	Outputs $\bar{Q}$	Comments
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1*	1*	Invalid condition

Timing diagram



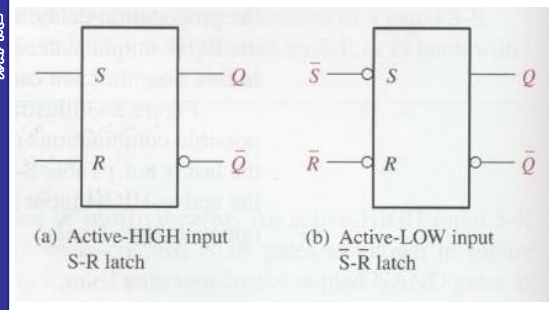
Memory Function

R=1; S=0; $\begin{cases} Q=0 \\ \overline{Q}=1 \end{cases}$ "0", remember "0"

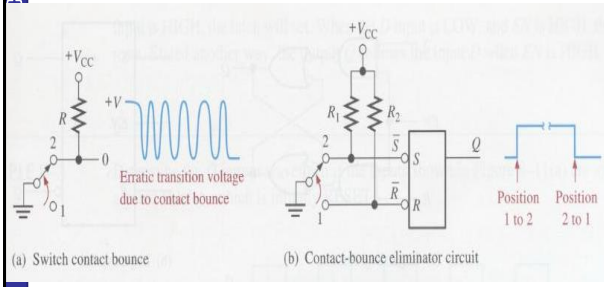
S=1; R=0; $\begin{cases} Q=1 \\ \overline{Q}=0 \end{cases}$ "1", remember "1"

Bi-stable ⇨ **Used to store 1 bit binary number**

Logic Symbol



Application Example



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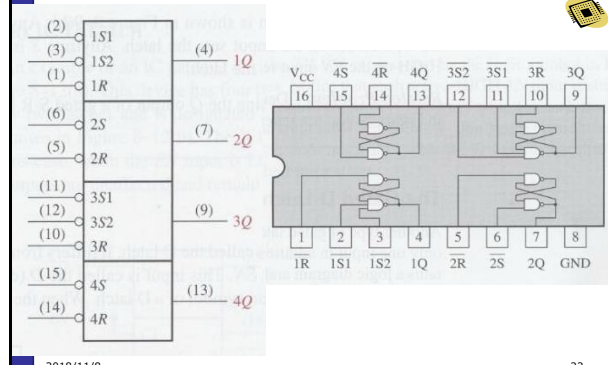
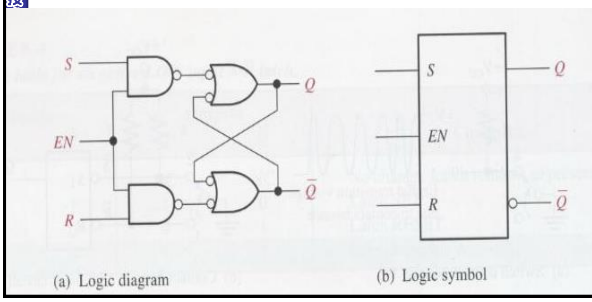
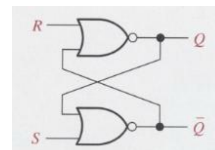


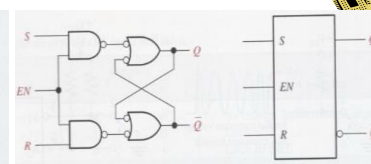
The Gated S-R Latch

EN: control the time when the inputs S and R can control the output. (***Level-triggered***)



Comparison

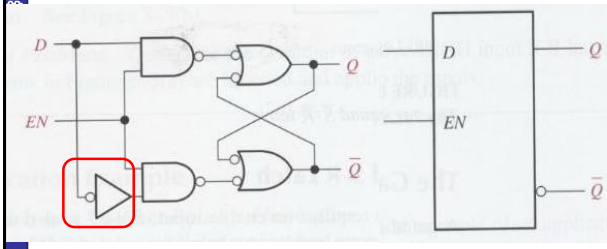




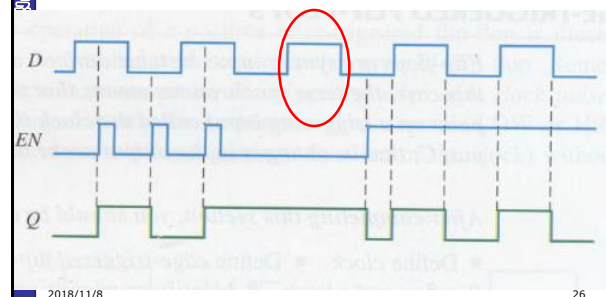
R	S	Q	$\overline{Q}$
1	1	Q_0	$\overline{Q_0}$
0	1	1	0
1	0	0	1
0	0	1*	1*

E	R	S	Q	$\overline{Q}$
0	X	X	Q_0	$\overline{Q_0}$
1	0	0	Q_0	$\overline{Q_0}$
1	0	1	1	0
1	1	0	0	1
1	1	1	1*	1*

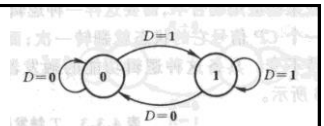
2 The Gated D Latch

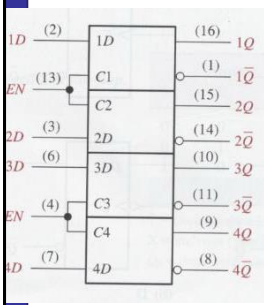


Example



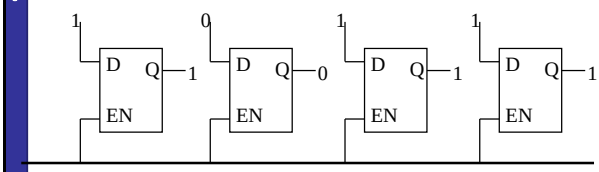
74LS75





Inputs		Outputs		Comments
D	EN	Q	$\overline{Q}$	
0	1	0	1	RESET
1	1	1	0	SET
X	0	Q_0	$\overline{Q}_0$	No change

Application example: Latches for temporary data storage



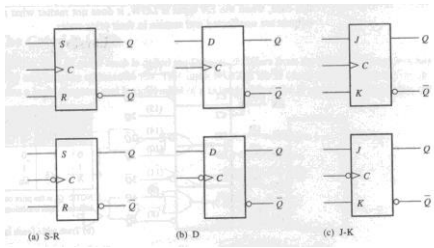
chapter6

- 32,34，，46，48

7.2 Edge-triggered Flip-Flops

- Flip-flops(触发器) are *synchronous bi-stable* devices. The term *synchronous （同步）* means that the output changes state only at a specified point on a triggering input called the clock (CLK) is designated as a control input C. i.e., changes in the output occur in synchronous with the clock.
- An edge-triggered flip-flop changes state either at the *positive edge* (rising edge) or at the *negative edge* (falling edge) of the clock pulse and is sensitive to its input only at this transition of the clock.

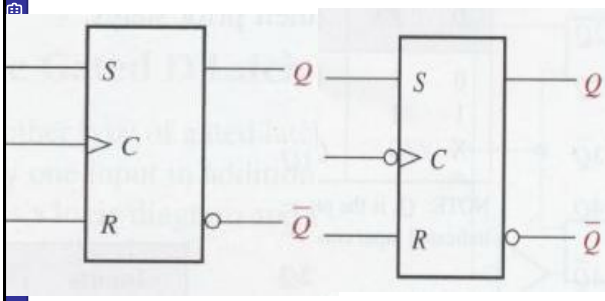
- *Edge-triggered flip-flops* (FF)
  - S-R flip-flop
  - J-K flip-flop
  - D flip-flop
  - T flip-flop



1 The edge-triggered S-R FF

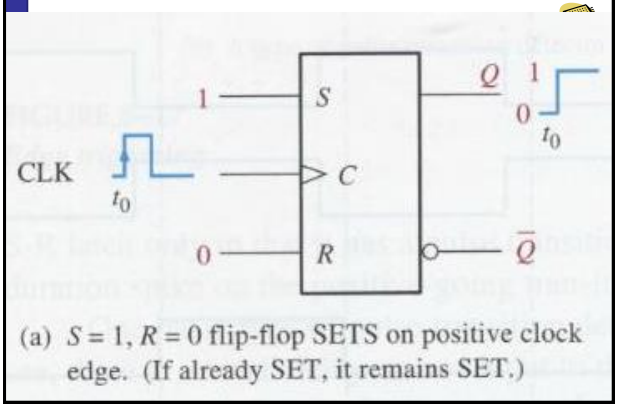
- The S and R inputs of the S-R flip-flop are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the *triggering edge of the clock pulse*.
- When S is HIGH and R is LOW on the triggering edge of the clock pulse, Q is HIGH and the flip-flop is *SET*. When S is LOW, R is HIGH, Q is LOW and flip-flop is *RESET*. When S and R are both LOW, the output does not change from its prior state. When S and R are both HIGH, it is an invalid condition.

The edge-triggered S-R FF

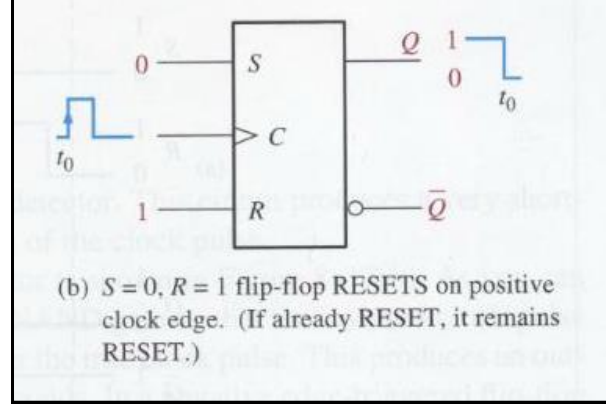


Truth Table of S-R FF

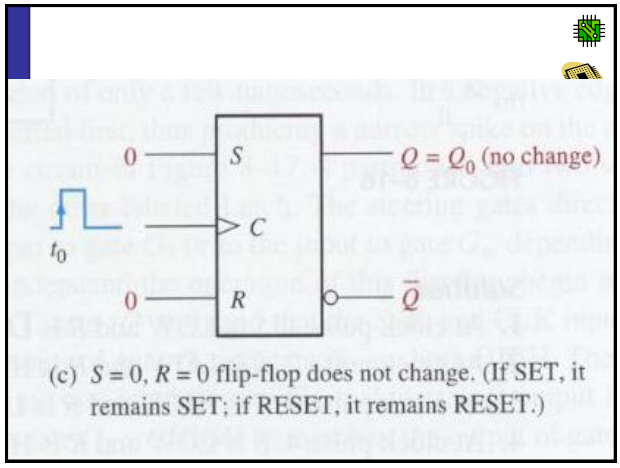
Inputs			Outputs		
S	R	CLK	Q	$\overline{Q}$	Comments
0	0	X	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid



(a) $S = 1, R = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $S = 0, R = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $S = 0$, $R = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

Example

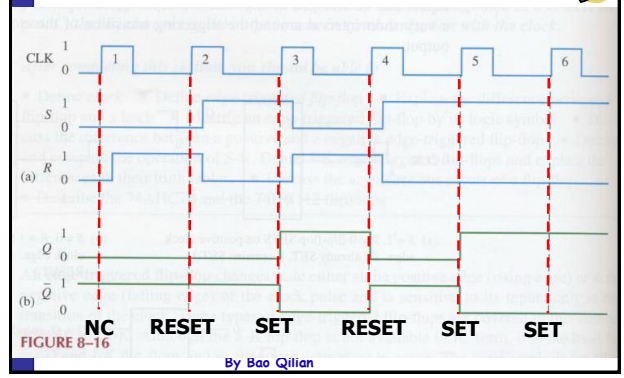
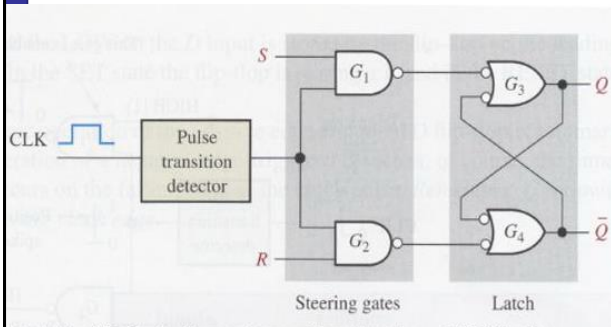


FIGURE 8–16

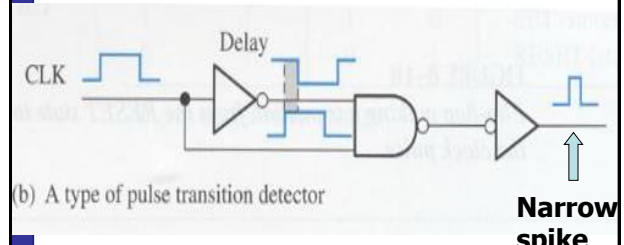
By Bao Qilian

A method of Edge-triggering



(a) A simplified logic diagram for a positive edge-triggered S-R flip-flop

Pulse transition detector

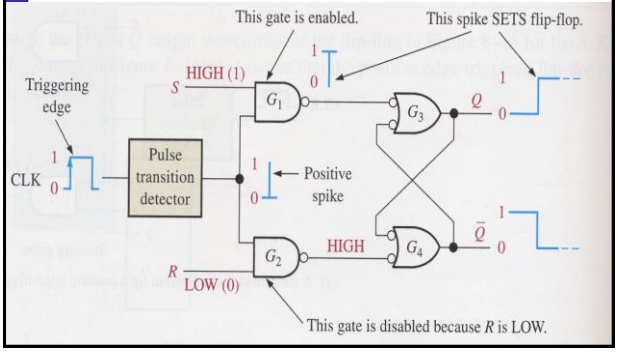


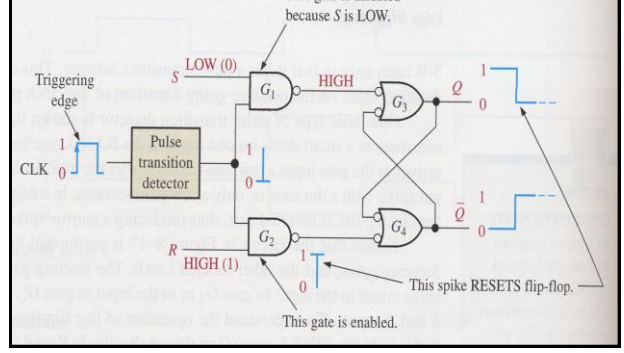
(b) A type of pulse transition detector

Narrow spike

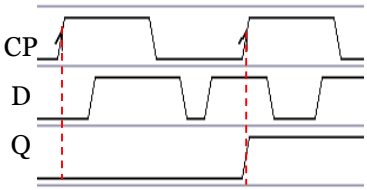
By Bao Qilian

2 The Edge-Triggered SR FF





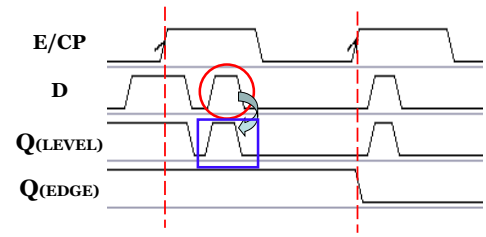
Timing diagram



Truth Table

CP	D	Q	$\overline{Q}$
↑	D	D	$\overline{D}$

Comparison of edge-triggered and level-triggered

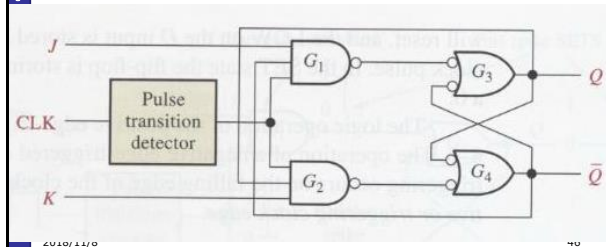


Examples of MSI Chips

Number	Flip-Flop Type	Output	Features
'74	Dual D	$\overline{Q}$ Q	Pre-set,Clear
'174	Hex D	Q	Clear
'171/'175	Quad D	$\overline{Q}$ Q	Clear
'273	Octal D	Q	Clear
'374/'377	Octal D	Q	Output enable
'378	Hex D	Q	Output enable
'379	Quad D	$\overline{Q}$ Q	Output enable

3 The Edge-Triggered J-K FF

***No invalid states.**

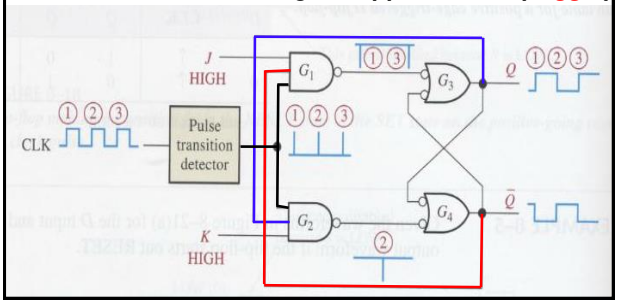


①IF J=1,K=0,Q_0=0;THEN G_1 enabled, Q=1 (SET)

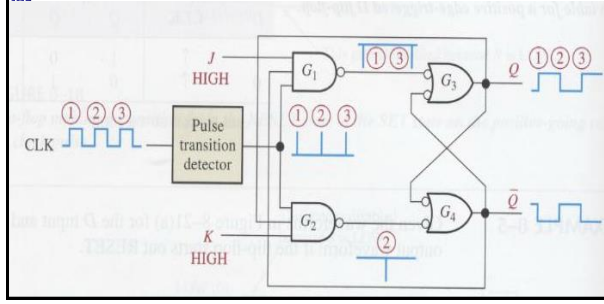
②IF J=0,K=1,Q_0=1;THEN G_2 enabled, Q=0 (RESET)

③IF J=0,K=0; THEN no change

④IF J=1,K=1; THEN change to opposite state(*Toggle*)

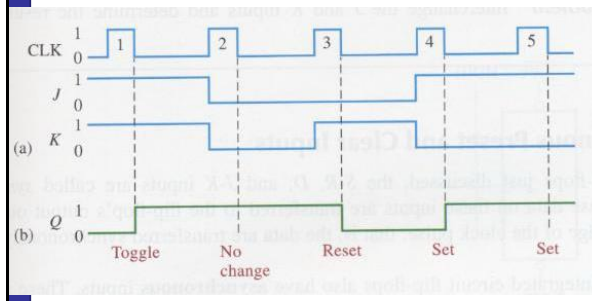


Toggle operation when J=K=1



- When J=K=1
- If Q=0, then Q=$\overline{Q}_0$ (from G_3, when CP↑)
- If Q=1,then $\overline{Q}$=Q_0 (from G_4, when CP↑)

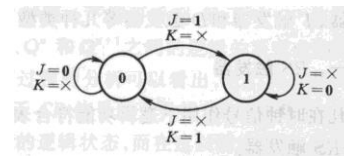
Timing diagram

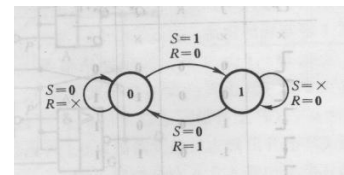


Truth Table

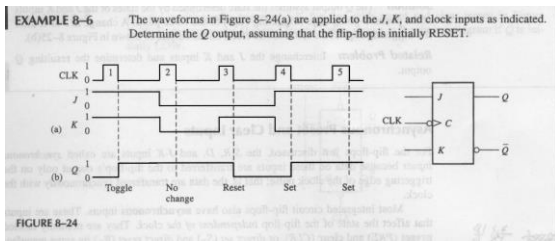
Inputs J	K	CLK	Outputs Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

The Edge-Triggered J-K Flip-Flop

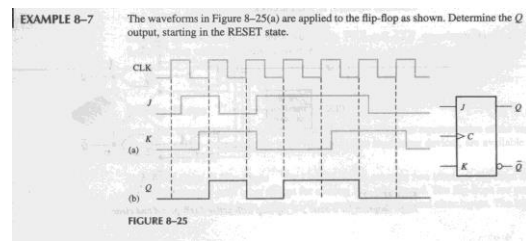




Example 8-6

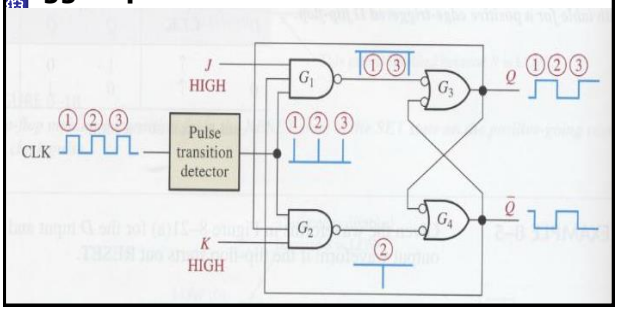


Example 8-7



4 The Edge-Triggered Toggle FF

Toggle operation when J=K=1



Transition equations of FFs

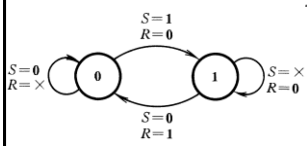
- SR Flip-flop
- JK Flip-flop
- Toggle Flip-flop
- D Flip-flop

By Bao Qilian

SR Flip-flop

$$Q^{n+1} = \bar{S}\bar{R}Q^n + S\bar{R}\bar{Q}^n + S\bar{R}Q^n$$
$$= S\bar{R} + \bar{S}\bar{R}Q^n$$

S	R	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	*
1	1	1	*

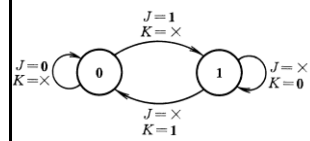


By Bao Qilian

JK Flip-flop

$$Q^{n+1} = J\bar{Q}^n + \bar{K}Q^n$$

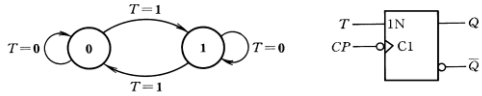
J	K	Q^n	Q^{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



By Bao Qilian

Toggle Flip-flop

T	Q^n	Q^{n+1}
0	0	0
0	1	1
1	0	1
1	1	0



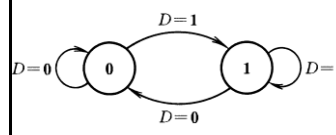
$$Q^{n+1} = T\bar{Q}^n + \bar{T}Q^n \overset{T=1}{=} \bar{Q}^n$$

By Bao Qilian

D Flip-flop

$$Q^{n+1} = D$$

D	Q^n	Q^{n+1}
0	0	0
0	1	0
1	0	1
1	1	1



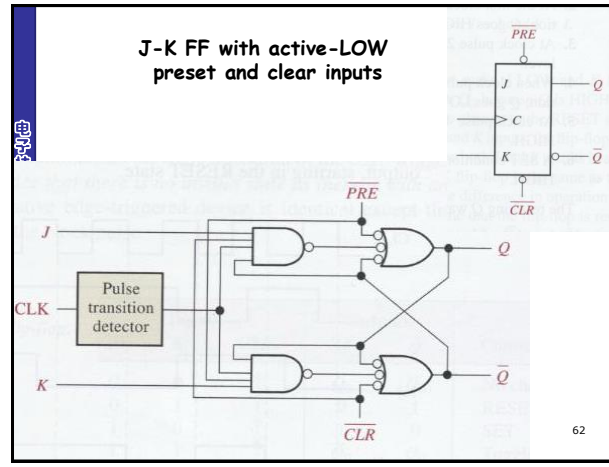
By Bao Qilian

Asynchronous Preset and Clear Inputs

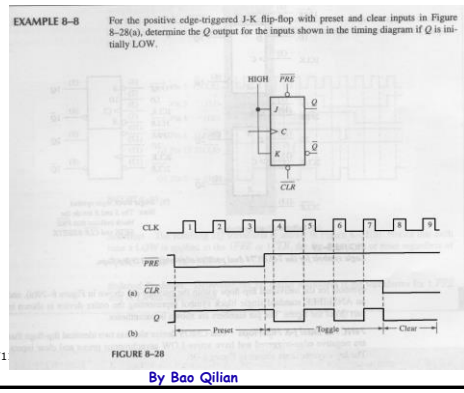
- Asynchronous（异步） inputs are independent of the clock. Usually labeled *preset* (*PRE：预置*) and *clear* (*CLR：清零*), or *direct set* (*SD*) and *direct reset* (*RD*).

By Bao Qilian

J-K FF with active-LOW preset and clear inputs



Example 8-8



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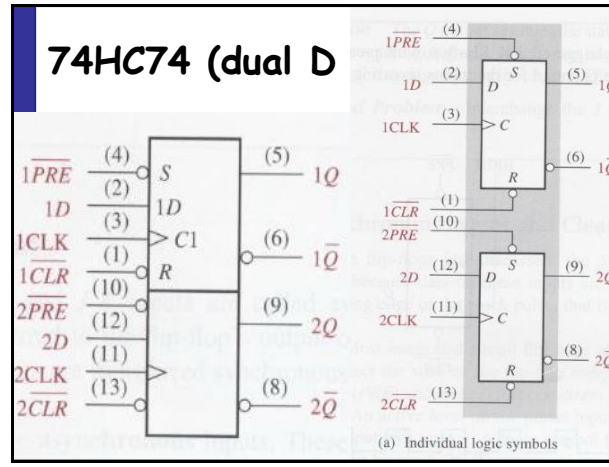
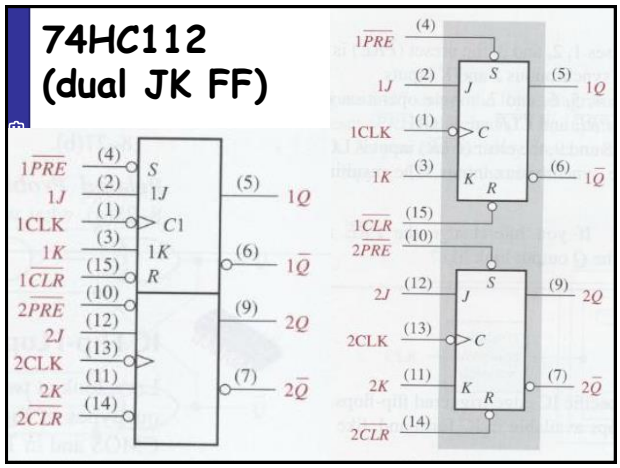
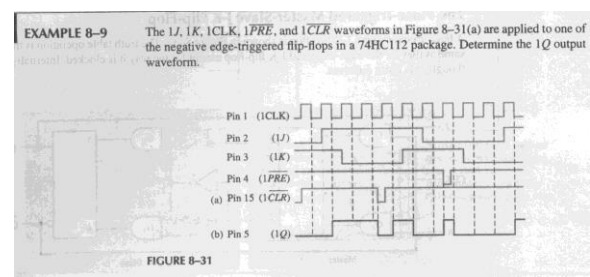
74HC74 (dual D



74HC112 (dual JK FF)

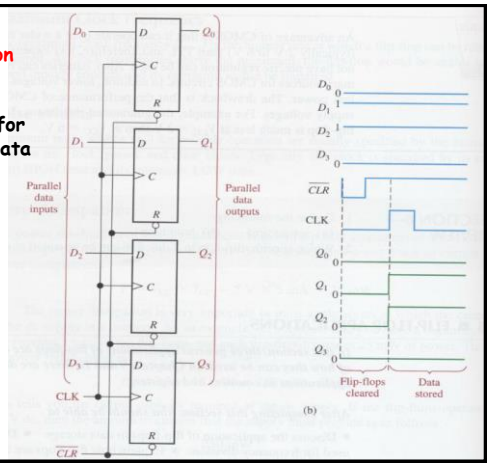


Example 8-9

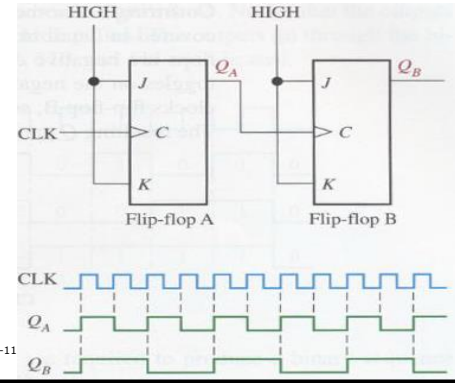


By Bao Qilian

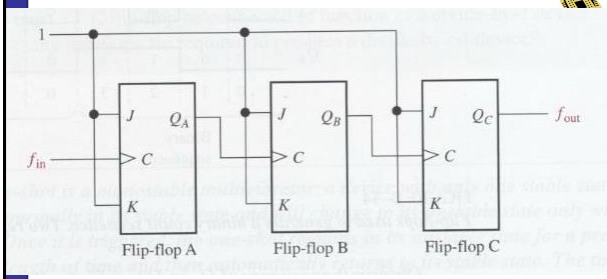
Application example: Basic register for parallel data storage



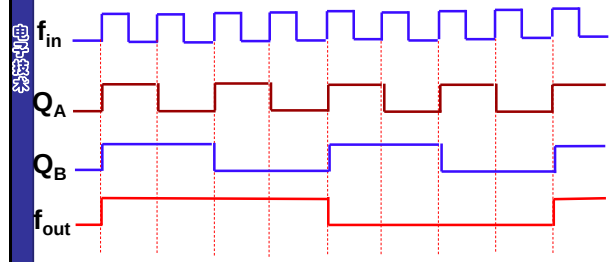
J-k FF as a devide-by-2 device



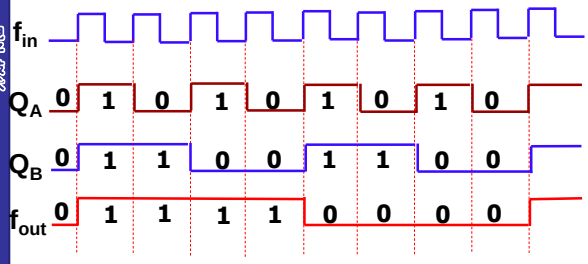
Exercise:



By Bao Qilian



By Bao Qilian



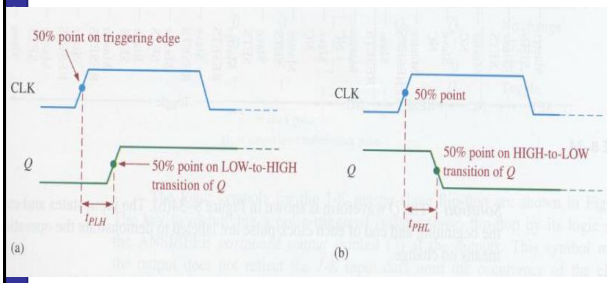
By Bao Qilian

7.3 Flip-Flops Operation Characteristics

- Propagation delay times
- Set-up time
- Hold Time
- Maxim Clock Frequency
- Pulse Widths
- Power Dissipation

By Bao Qilian

Propagation delay times



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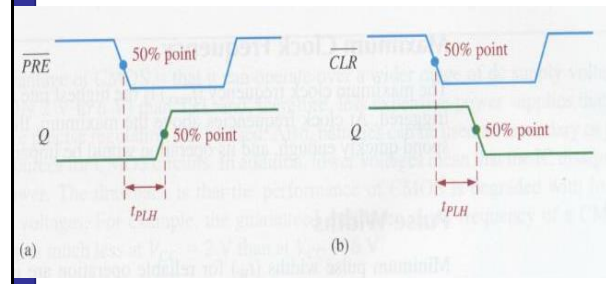

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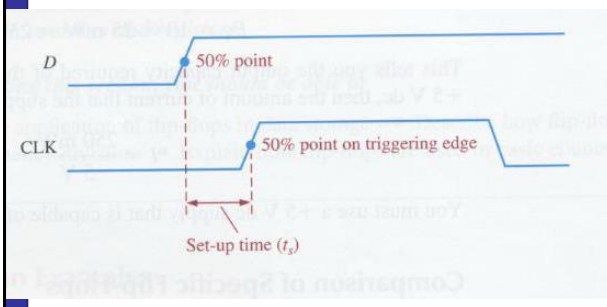
Set-up time



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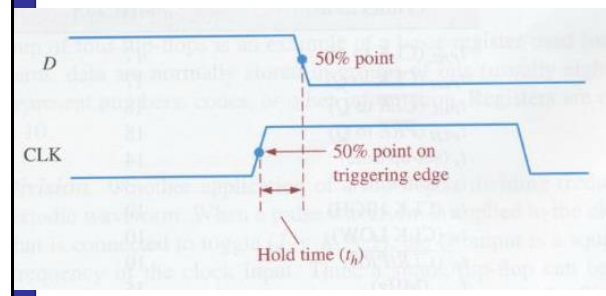
Hold Time



By Bao Qilian

Other parameters

- Maxim Clock Frequency
- Pulse Widths
- Power Dissipation

By Bao Qilian

Comparison of typical FFs

Parameter (Times in ns)	CMOS 74HC74A	CMOS 74AHC74	TTL 74LS74A	TTL 74F74
t_{PHL} (CLK to Q)	17	4.6	40	6.8
t_{PLH} (CLK to Q)	17	4.6	25	8.0
t_{PHL} ($\overline{CLR}$ to Q)	18	4.8	40	9.0
t_{PLH} ($\overline{PRE}$ to Q)	18	4.8	25	6.1
t_s (set-up time)	14	5.0	20	2.0
t_h (hold time)	3.0	0.5	5	1.0
t_W (CLK HIGH)	10	5.0	25	4.0
t_W (CLK LOW)	10	5.0	25	5.0
t_W ($\overline{CLR}$/$\overline{PRE}$)	10	5.0	25	4.0
f_{max} (MHz)	35	170	25	100
Power (mW), quiescent	0.012	1.1		
Power (mW), 50% duty cycle			44	88

Summary of FF

- Latches
- Flip-Flops
  - S-R FF
  - D FF
  - J-K FF
  - T FF
- Comparison
- Characteristics

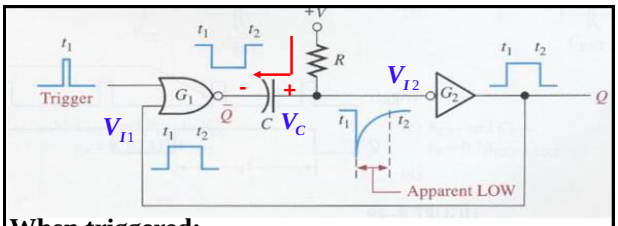
7.4 555 Timer

Objectives

- one-shots
- Multi-vibrators
- 555 timer
- *Reading reference:*
  - Digital fundamentals
    P421-434
  - Fundamentals of digital electronics
    p308-352

1 One-Shots

- *One shot* (mono-stable multi-vibrator单稳态触发器) only has one stable state and one unstable state.
- When triggered the device changes from its stable state and remains there for a fixed period of time, known as the *pulse width*, before returning to its stable state.
- The duration time of the unstable state determined by the circuit parameters, no related with the triggered pulse.
- The duration time of the unstable state determines the pulse width of the output pulse.



When triggered:

$\bar{Q}=0 \rightarrow V_C \approx \bar{Q} \rightarrow V_{I2} \approx 0 \rightarrow Q=1 \rightarrow V_{I1}=1$

$\bar{Q}=0 \rightarrow V_C \uparrow \rightarrow V_{I2} \uparrow \rightarrow Q \downarrow \rightarrow Q=0 \rightarrow V_{I1} \downarrow \rightarrow V_{I1}=0$

$\bar{Q}=1$

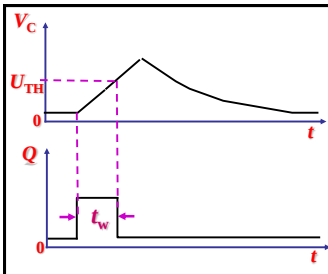
$V_c = V_{\bar{Q}} + u_c = V_{I2}$

$1) stable: u_c = 0, V_{\bar{Q}} = 1 \Rightarrow V_C = V_{I2} = 1 \Rightarrow Q = 0$

$2) unstable: u_c = 0, V_{\bar{Q}} = 0 \Rightarrow V_C = V_{I2} = 0 \Rightarrow Q = 1$

$\text{charging}: u_c \uparrow \Rightarrow V_C \uparrow \Rightarrow V_{I2} \uparrow \Rightarrow V_{I2} = V_{TH}$

$\Rightarrow Q \downarrow \Rightarrow Q = 0 (stable\ state)$



$$v_c(t) = v_c(\infty) + [v_c(0_+) - v_c(\infty)]e^{-\frac{t}{\tau}}$$

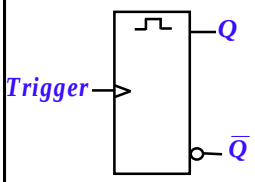
$$v_c(\infty) = V_{DD} \qquad v_c(0_+) = 0 \qquad \tau = RC$$

$$v_c(t_w) = V_{TH} \Rightarrow t_W = RC \ln \frac{V_{DD}}{V_{DD} - V_{TH}}$$

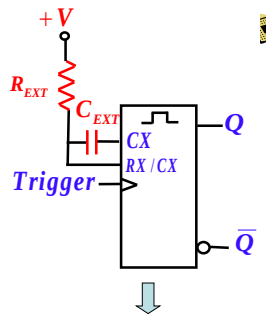
- Stable state: Q=0
- Unstable state: Q=1
- The time duration determined by the charge time of C and R , i.e. the RC time constant.

$$t_W = RC \ln \frac{V_{DD}}{V_{DD} - V_{TH}} = RC \ln 2 \approx 0.69RC$$

$$\approx 0.7RC$$



Logic Symbol



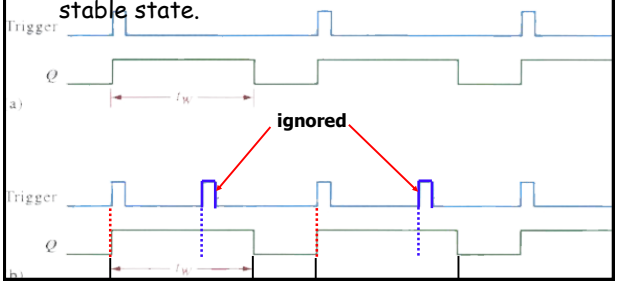
$$t_W = 0.7R_{ext}C_{ext}$$

Two basic types of IC one-shot

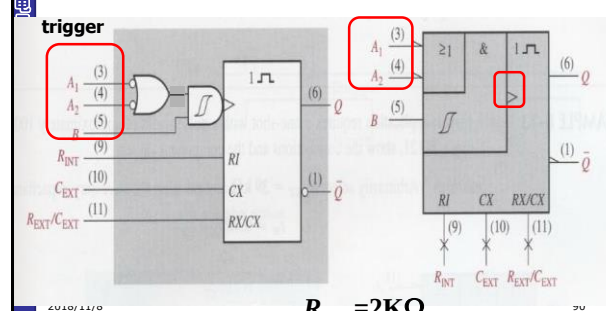
- ***Nonretriggerable* one-shot：74LS121**
- ***Retriggerable* one-shot：74LS122**

Non-retriggerable one-shot

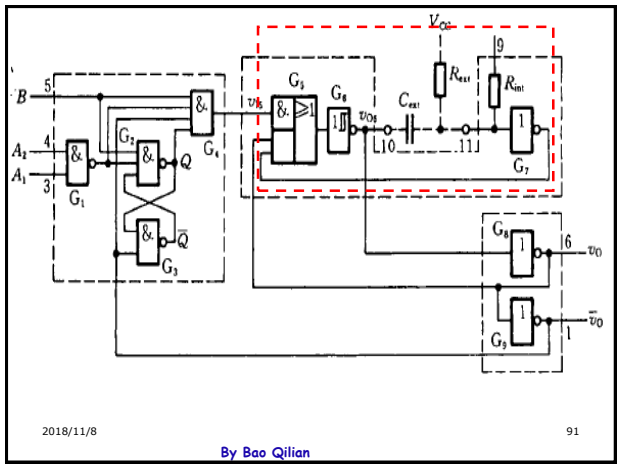
Not respond to any additional trigger pulse from the time it is triggered until it returns to stable state.



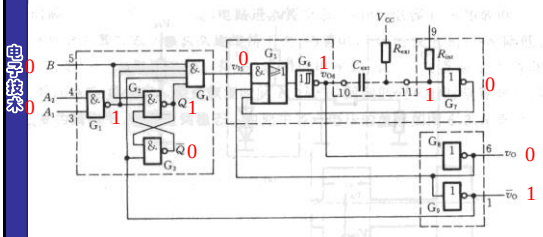
74LS121：non-retriggered one-shot



R_{INT}=2KΩ

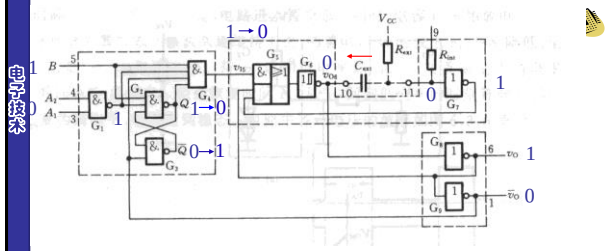


74121: Stable State



$$Assume: A_1 = 0, A_2 = \times \rightarrow v_{O1} = 1 \rightarrow Q = 1$$
$$\left.\begin{array}{l} B = 0 \rightarrow v_{I5} = 0 \\ v_{I7} = 1 \rightarrow v_{O7} = 0 \end{array}\right\} \rightarrow v_{O6} = 1 \rightarrow v_O = 0 \rightarrow \bar{v}_O = 1 \left\{\begin{array}{l} \\ \end{array}\right. \overline{Q} = 0$$

74121: Unstable State



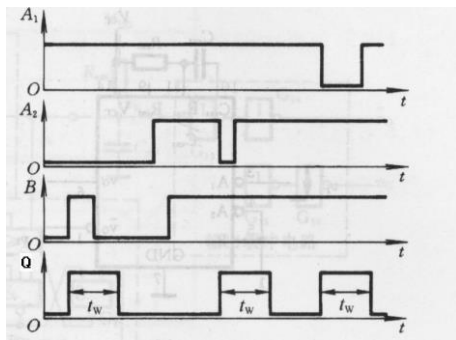
74121: Function Table

Inputs			Outputs	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

H = HIGH Logic Level
L = LOW Logic Level
X = Can Be Either LOW or HIGH
⎍ = A Positive Pulse
⎎ = A Negative Pulse

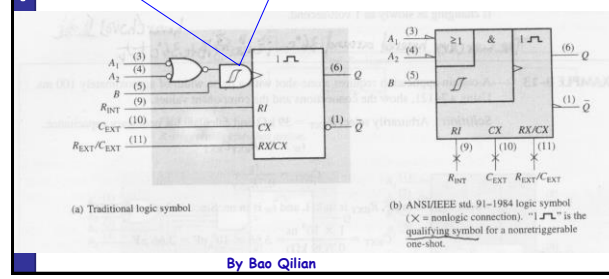
↑ = Positive Going Transition
↓ = Negative Going Transition

74121: Timing Diagram



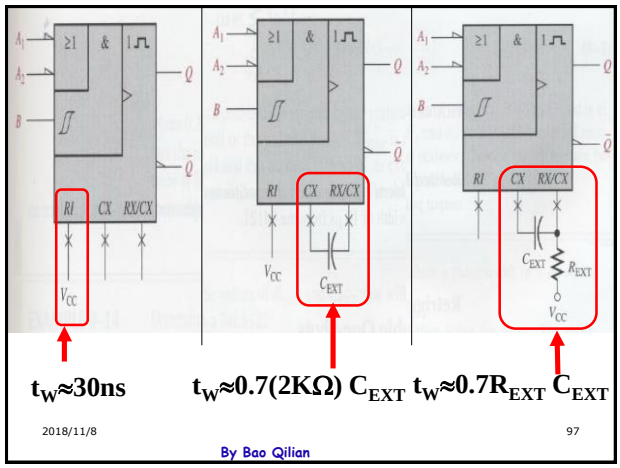
74121: Schmitt-Trigger Inputs

- This symbol indicates a Schmitt-trigger input. This type of input uses a special threshold circuit that produces hysteresis, a characteristic that prevents erratic switching between states when a slow-changing trigger voltage hovers around the critical input level.



(a) Traditional logic symbol

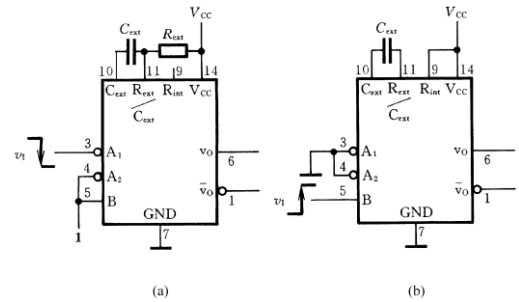
(b) ANSI/IEEE std. 91–1984 logic symbol (× = nonlogic connection). "1 ⎍" is the qualifying symbol for a nonretriggerable one-shot.



集成单稳态触发器74121的外部连接方法

（a）使用外接电阻R_{ext} （下降沿触发）

（b）使用内部电阻R_{int} （上升沿触发）



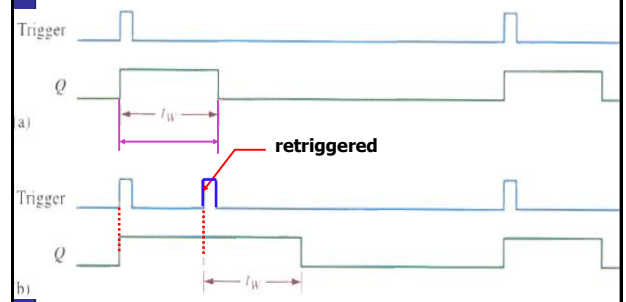
Exercise

To achieve a one-shot with a pulse width of approximately 10ms, using a 74121.

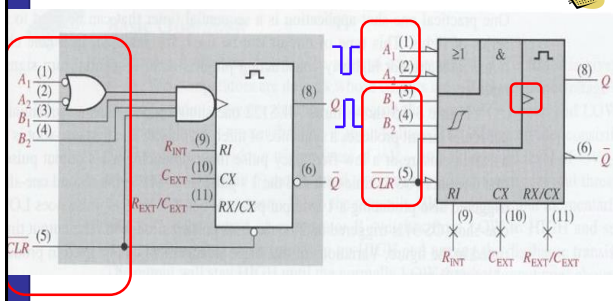
If select R_{EXT}=20KΩ, calculate the capacitance:

C_{EXT}=?

Retriggerable One-shots



74LS122



Width of pulse

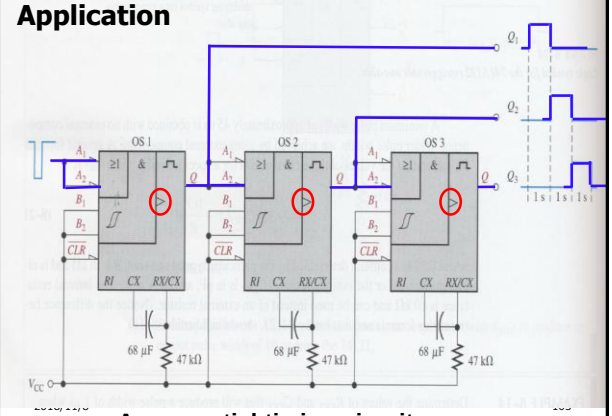
With no external resistor and capacitor:

t_W≈45ns

With external resistor and capacitor:

$$t_W = 0.32RC_{EXT}(1+\frac{0.7}{R})$$

Application



A sequential timing circuit

Exercise:

$$t_W = 0.32RC_{EXT}(1+\frac{0.7}{R})$$

$$= 0.32 \times 47K\Omega \times 68\mu F \times (1+\frac{0.7}{47K\Omega})$$

$$= 1.0227(s)$$

$$\approx 1(s)$$

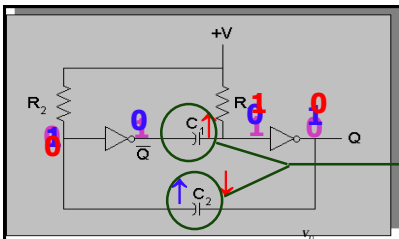
Applications:

- Timing
- Time delay
- Pulse conditioning

- 定时（产生一定宽度的矩形波）
- 整形（把不规则的波形变为规则的脉冲波形）
- 延时（将输入信号延迟一定时间后输出）

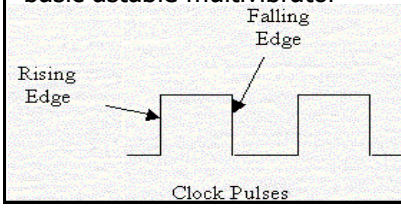
2 Astable Multivibrators

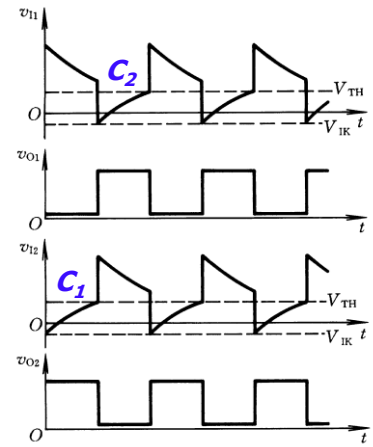
Astable multivibrator devices have no stable states, instead they *continually switch* between two unstable states. Consequently, they are used as *oscillators* to provide clock signals for timing purposes.



basic astable multivibrator

The two capacitive coupling networks prevents either inverter from having a stable state





calculation

For 74LS series:

If $R_1=R_2=R, C_1=C_2=C$, $R_1, R_2 << R_L$

$$T \approx 2RC \ln \frac{V_{OH} - V_{IK}}{V_{OH} - V_{TH}} \approx 1.3RC$$