

# 电子技术

# Introduction to

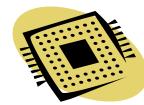
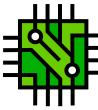
# Electronics

By Bao Qilian

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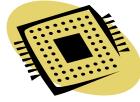
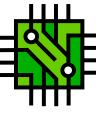
# Chapter 12 Digital and Analog Interfacing

## Objectives

- DAC
  - Binary-weighted-input DAC
  - R/2R ladder DAC
- ADC
  - Sampling and quantization
  - Flash ADC
  - Stairstep-ramp ADC

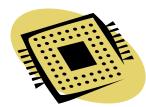
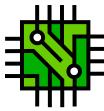
Reading Assignments:

P682-698

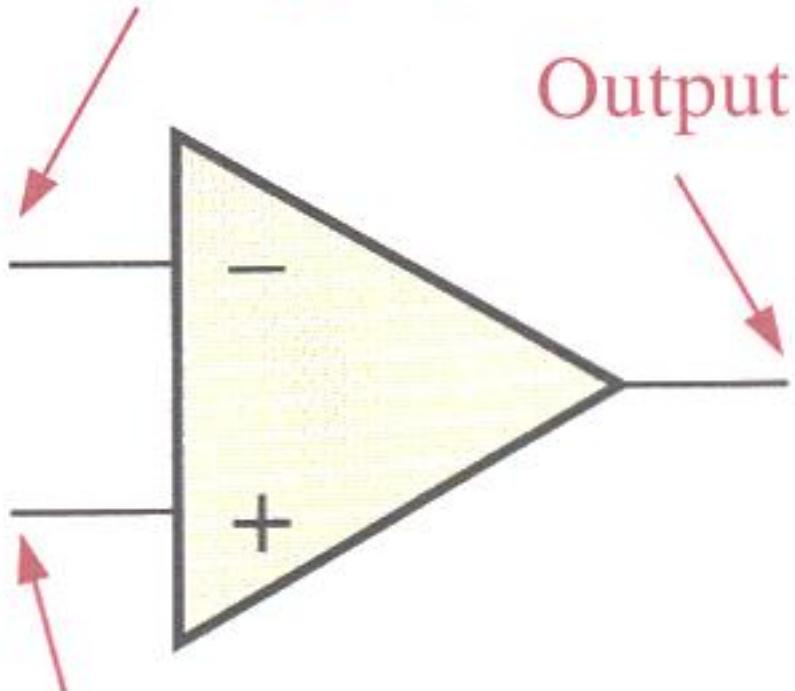


- DAC: digital-to-analogue converter
- ADC: analogue-to-digital converter

# Operational Amplifier (op-amp)



Inverting input

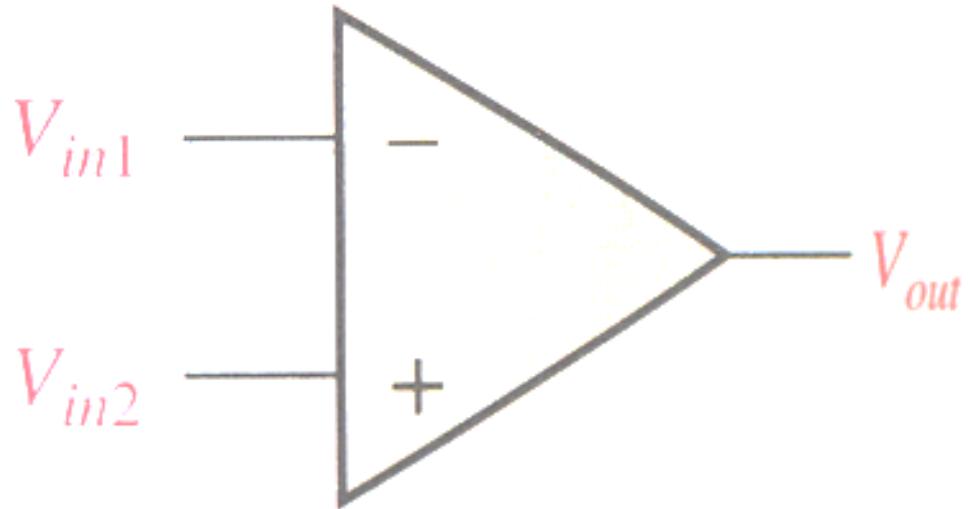
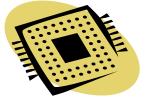
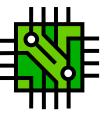


Noninverting input

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An op-amp is a linear amplifier that has two inputs and one output. It has a very high voltage gain, a very high input impedance, and a very low output impedance.<sup>4</sup>

# Voltage Comparator



$$V_{out} = -K(V_{in1} - V_{in2})$$

$\therefore K \rightarrow \infty$

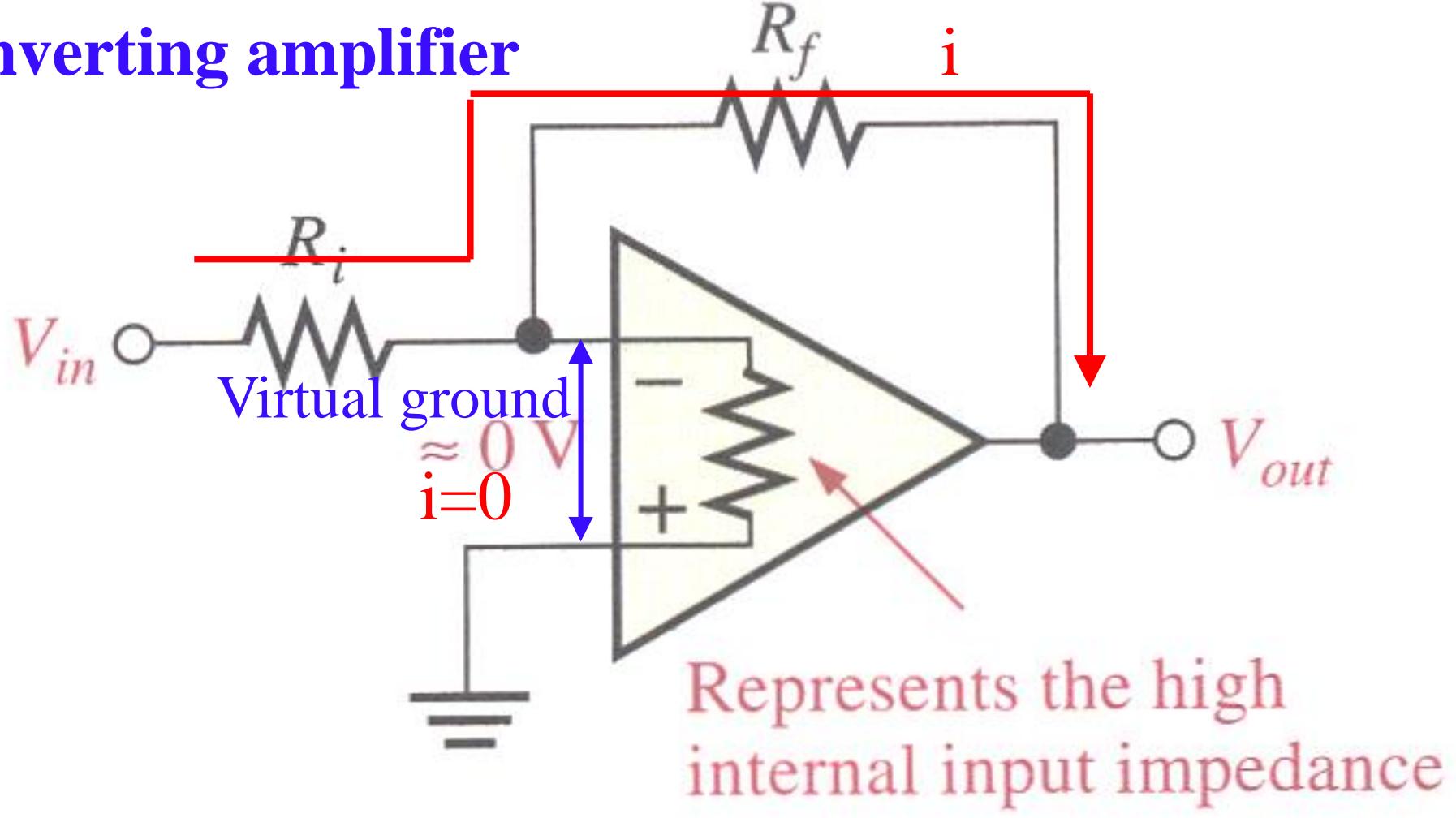
$\therefore \text{if } (V_{in1} - V_{in2}) > 0, V_{out} = LOW$

$\text{if } (V_{in1} - V_{in2}) < 0, V_{out} = HIGH$



Two saturated outputs

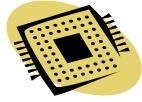
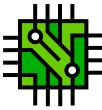
# Inverting amplifier



$$i = \frac{V_{in} - 0}{R_i} = \frac{0 - V_{out}}{R_f} \rightarrow \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i}$$

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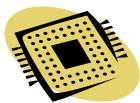
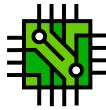
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# 1 Digital-to-analog Conversion

- Binary-weighted-input D/A Converter
- R/2R Ladder digital-to-analog converter

# Binary-weighted-input D/A Converter



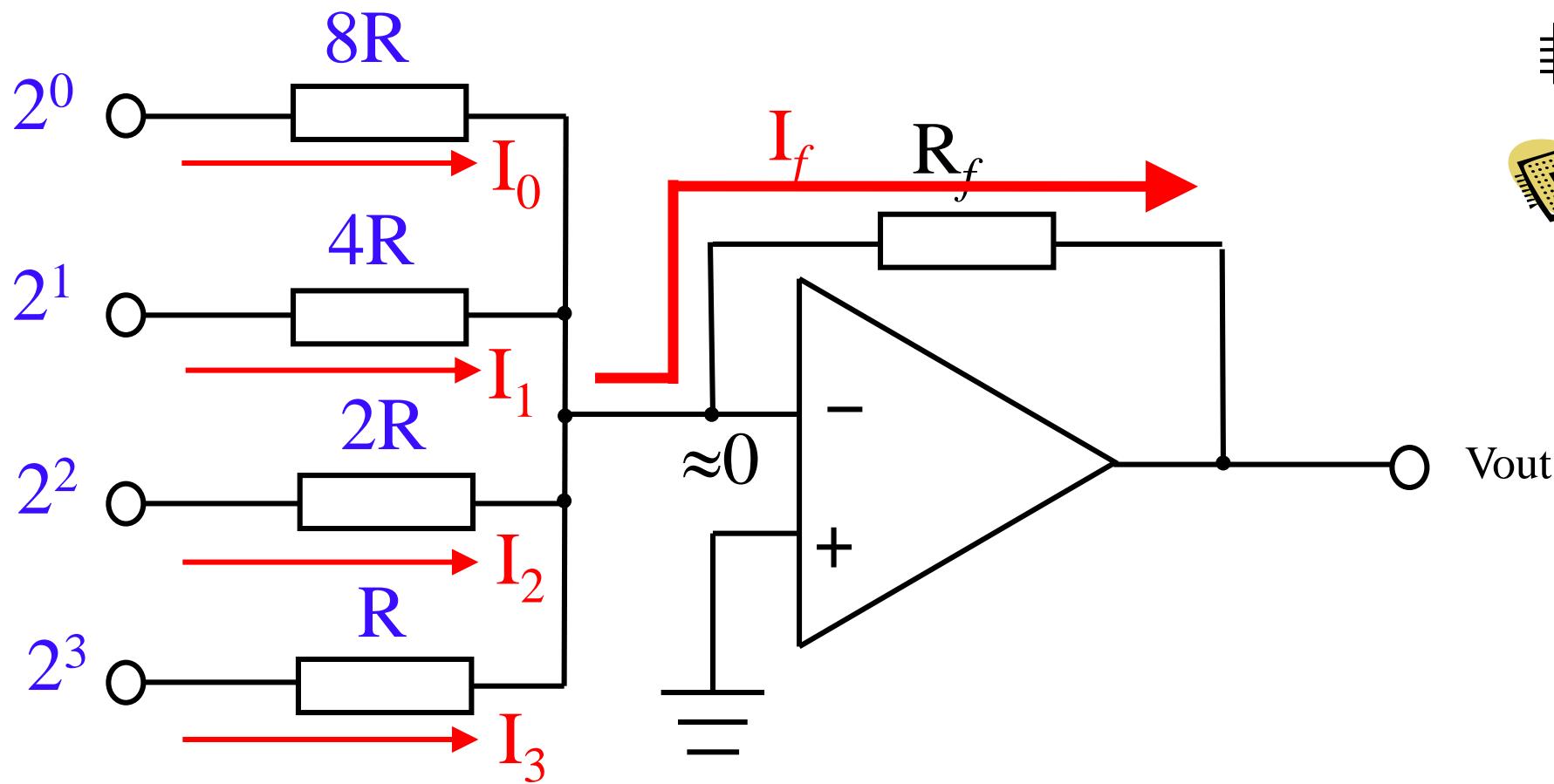
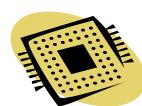
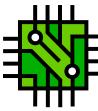
Sum-of-Weight expression:

$$(N)_r = C_{n-1}r^{n-1} + C_{n-2}r^{n-2} + \dots + C_1r^1 + C_0r^0 + C_{-1}r^{-1} + \dots + C_{-m}r^{-m}$$

For integer binary number:

$$(N)_2 = C_{n-1}2^{n-1} + C_{n-2}2^{n-2} + \dots + C_12^1 + C_02^0$$

$$\begin{aligned} R(N)_2 &= RC_{n-1}2^{n-1} + RC_{n-2}2^{n-2} + \dots + RC_12^1 + RC_02^0 \\ &= 2^{n-1}RC_{n-1} + 2^{n-2}RC_{n-2} + \dots + 2RC_1 + RC_0 \end{aligned}$$



$$I_f = I_0 + I_1 + I_2 + I_3$$

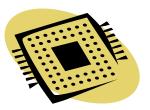
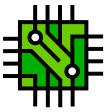
$$V_{out} = -I_f R_f = -\left(\frac{V}{8R} + \frac{V}{4R} + \frac{V}{2R} + \frac{V}{R}\right)$$

If binary number = 1111

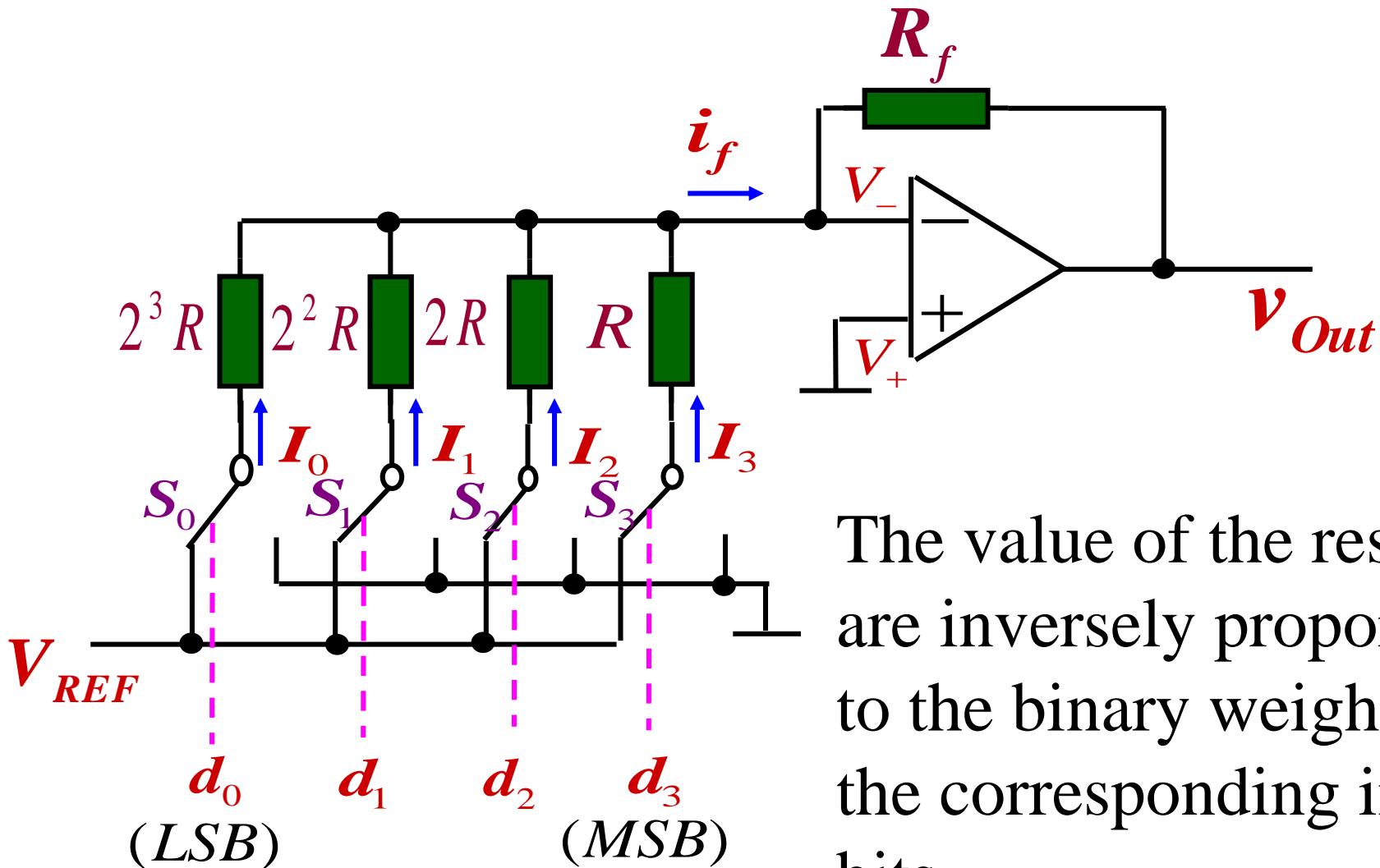
$$I_f = \frac{VR_f}{8R} (1 + 2 + 4 + 8)$$

$$= -\frac{VR_f}{8R} (1 \times 1 + 1 \times 2 + 1 \times 4 + 1 \times 8)$$

gain Weighted sum

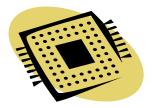
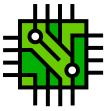


# Binary-weighted-input D/A Converter



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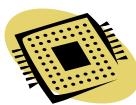
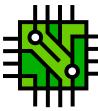
$$V_{out} = -I_f R_f$$

$$= -\frac{V_{REF} R_f}{8R} (d_3 2^3 + d_2 2^2 + d_1 2^1 + d_0 2^0)$$

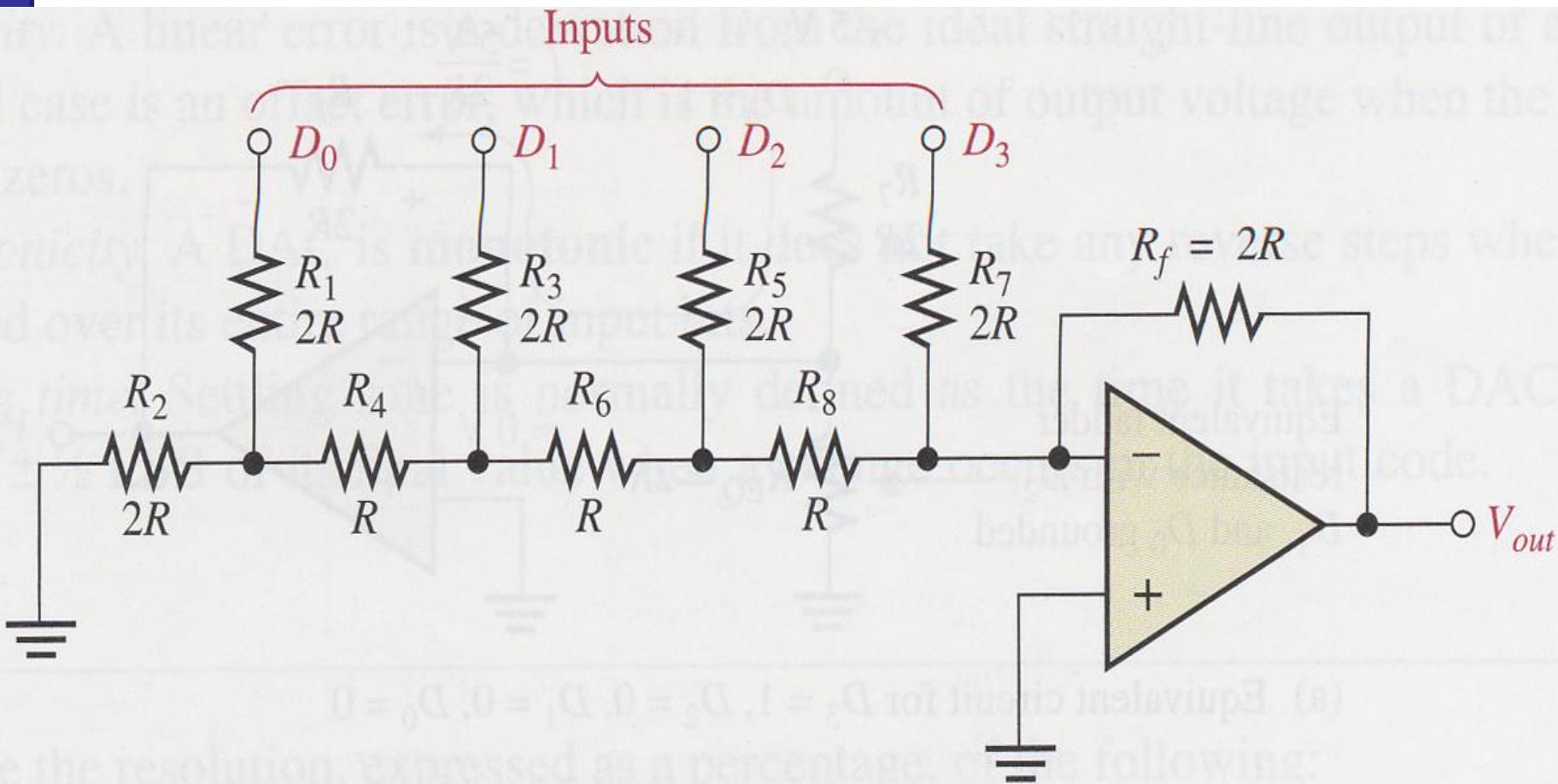
$$R_f = R/2 \quad = -\frac{V_{REF}}{2^4} (d_3 2^3 + d_2 2^2 + d_1 2^1 + d_0 2^0)$$

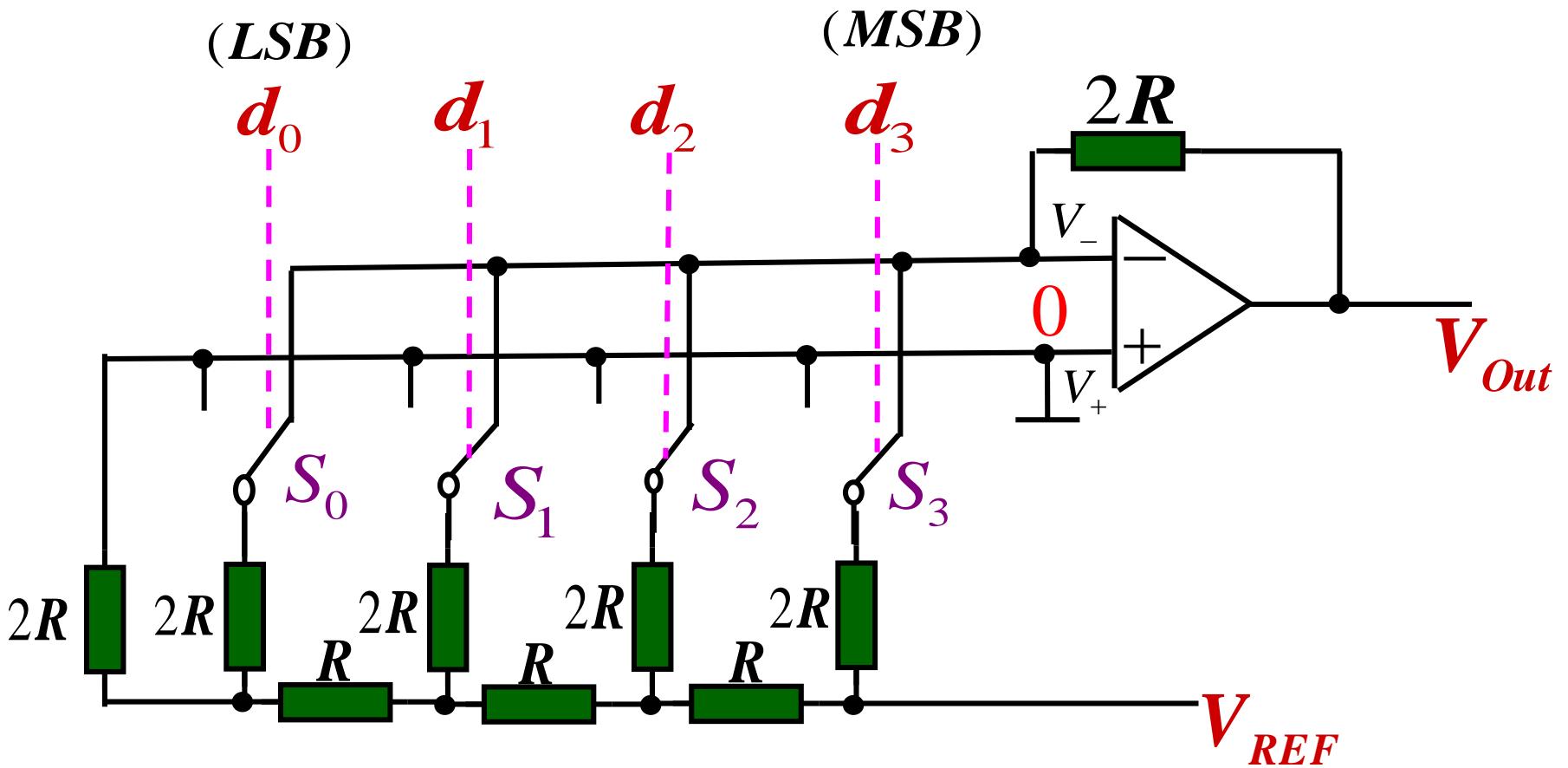
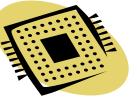
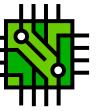
**Advantage:** simple

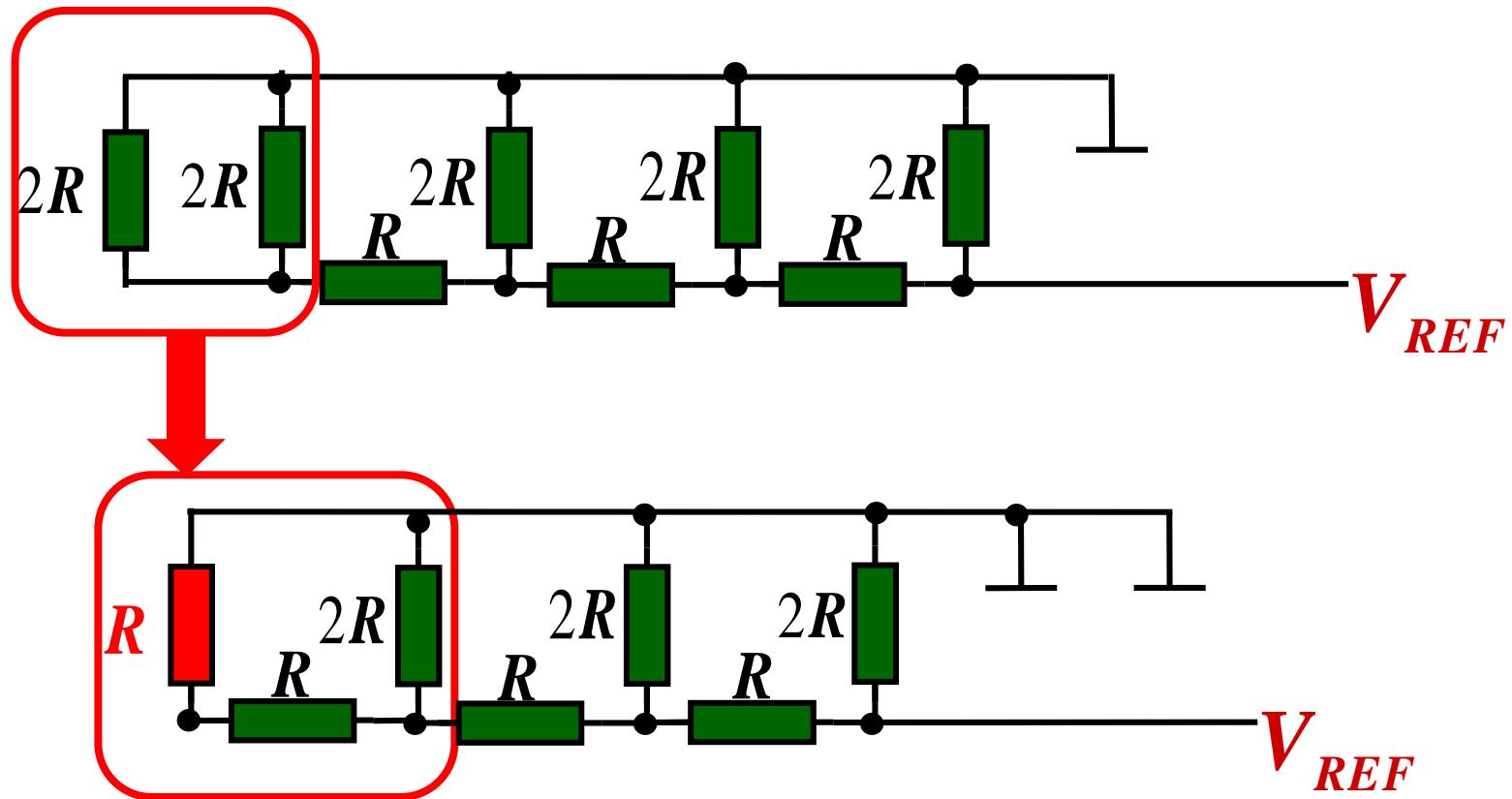
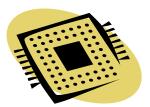
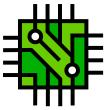
**Disadvantage:** because of different resistor values, the range of resistors is too big to be mass-produced.

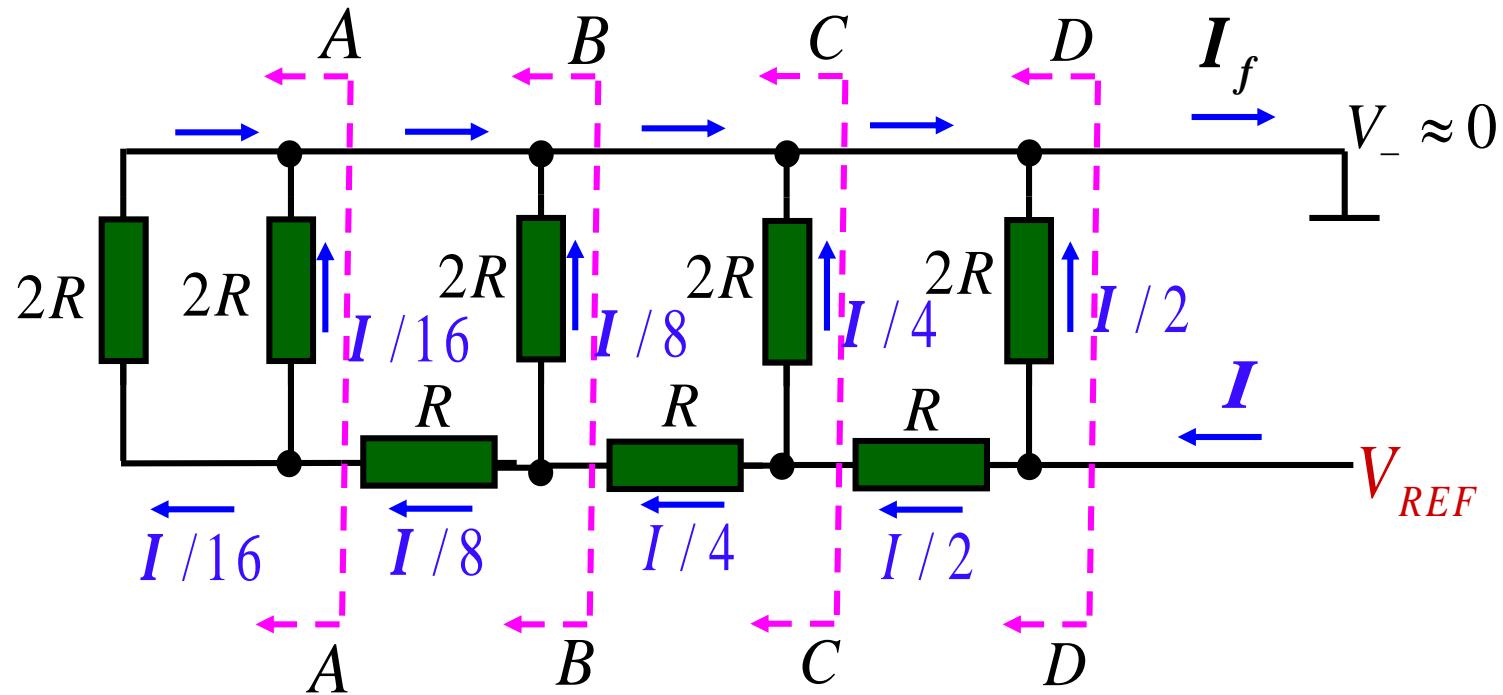
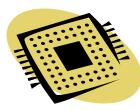


# R/2R Ladder Digital-to-analog Converter



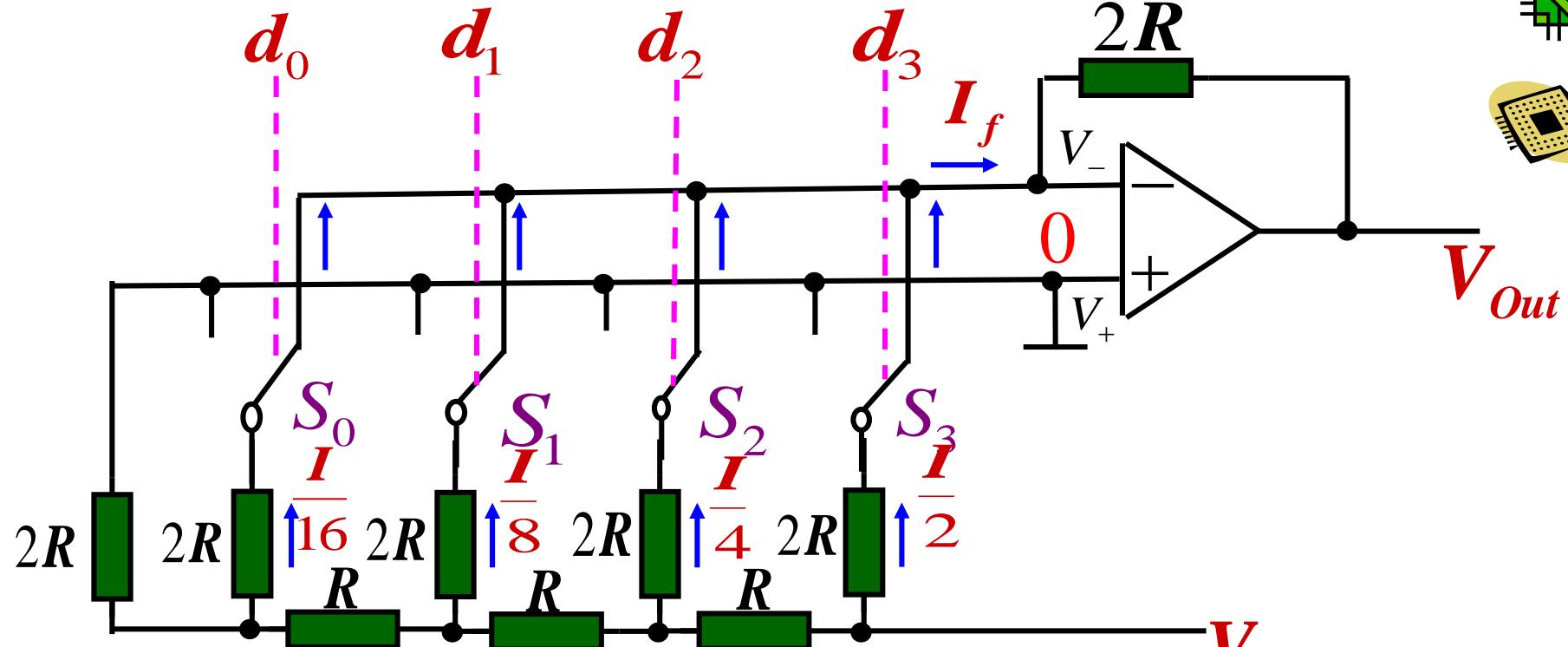
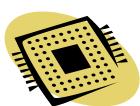
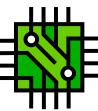






(LSB)

(MSB)



$$I_f = d_0 \frac{I}{16} + d_1 \frac{I}{8} + d_2 \frac{I}{4} + d_3 \frac{I}{2}$$

$$I = \frac{V_{REF}}{R}$$



$$V_{out} = -I_f R_f = -IR_f \left( d_0 \frac{1}{16} + d_1 \frac{1}{8} + d_2 \frac{1}{4} + d_3 \frac{1}{2} \right)$$

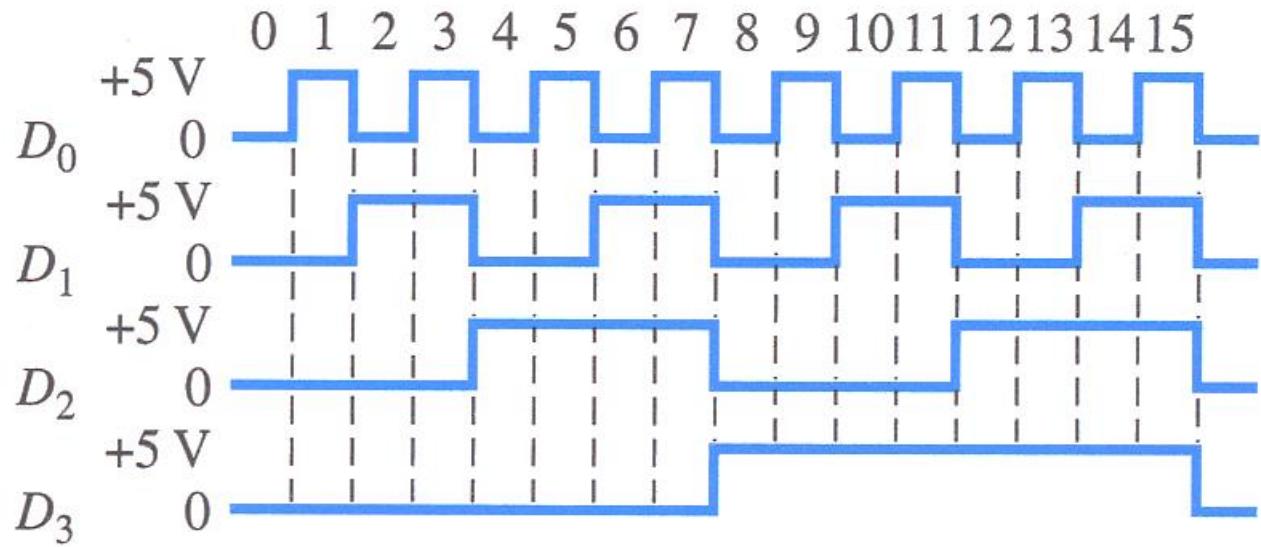
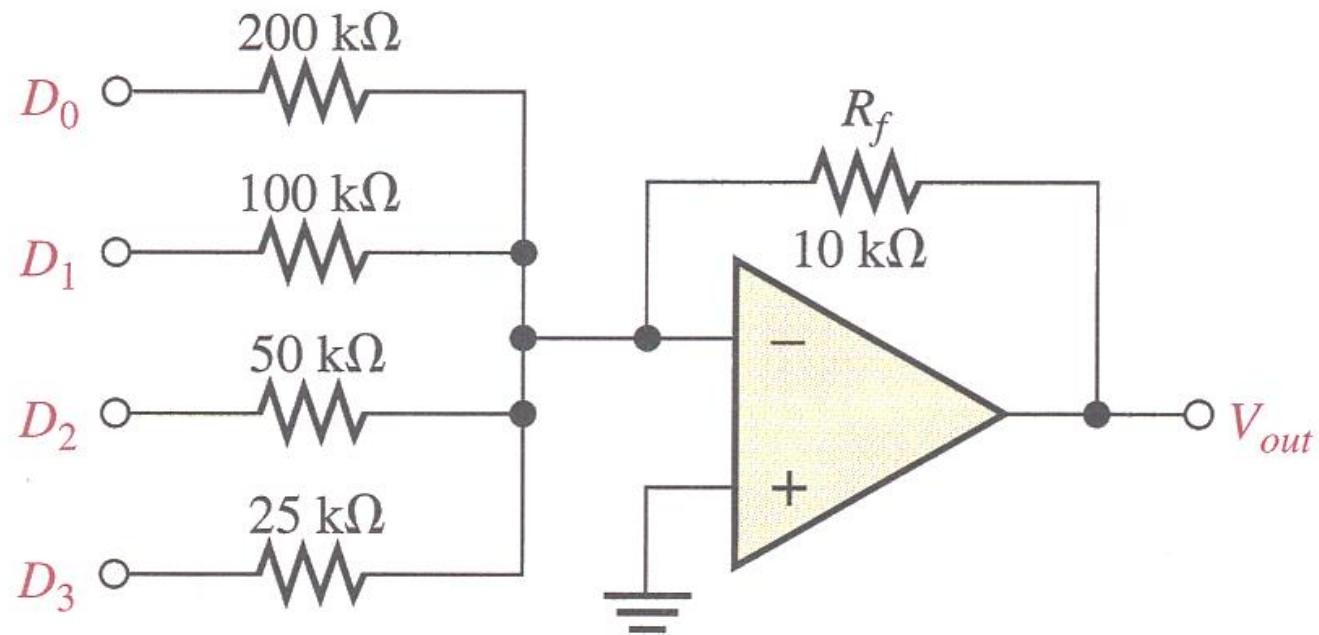
$$= -\frac{V_{REF}}{R} 2R \left( d_0 \frac{1}{16} + d_1 \frac{1}{8} + d_2 \frac{1}{4} + d_3 \frac{1}{2} \right)$$

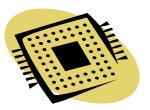
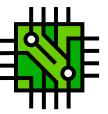
$$= -\frac{V_{REF}}{2^3} (d_0 2^0 + d_1 2^1 + d_2 2^2 + d_3 2^3)$$

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# Solution:

$$I_0 = \frac{5V}{200k\Omega} = 0.025mA$$

$$I_1 = \frac{5V}{100k\Omega} = 0.05mA$$

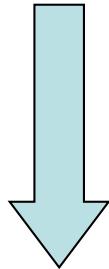
$$I_2 = \frac{5V}{50k\Omega} = 0.1mA$$

$$I_3 = \frac{5V}{25k\Omega} = 0.2mA$$

}



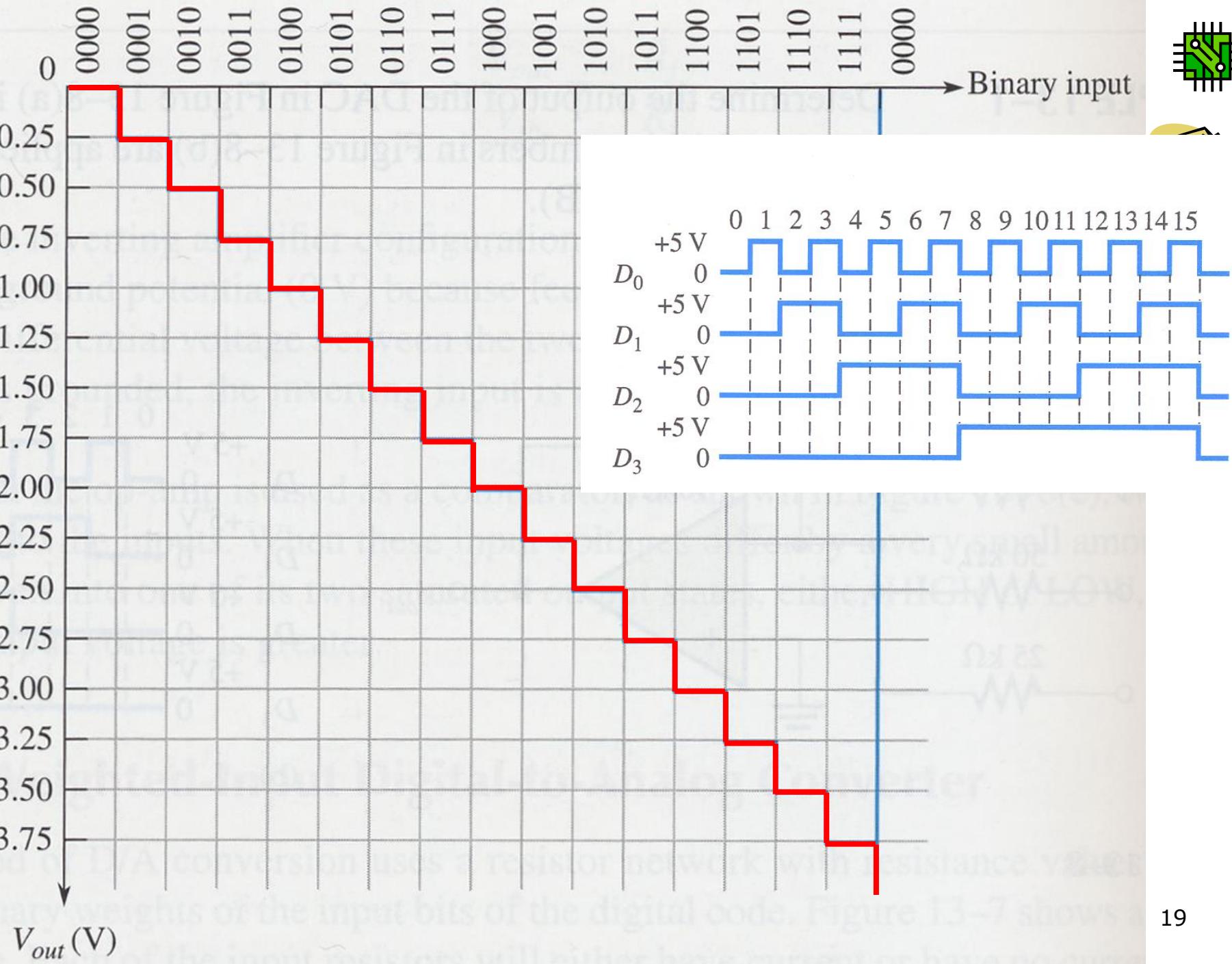
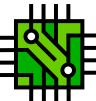
$$I_f = D_0 I_0 + D_1 I_1 + D_2 I_2 + D_3 I_3$$



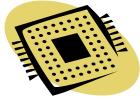
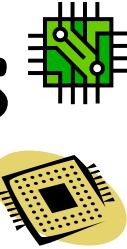
$$V_{out} = -I_f R_f$$

$$= -(D_0 I_0 + D_1 I_1 + D_2 I_2 + D_3 I_3) R_f$$

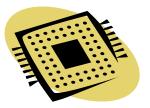
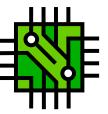
$$= D_0(-0.25V) + D_1(-0.5V) + D_2(-1V) + D_3(-2V)$$



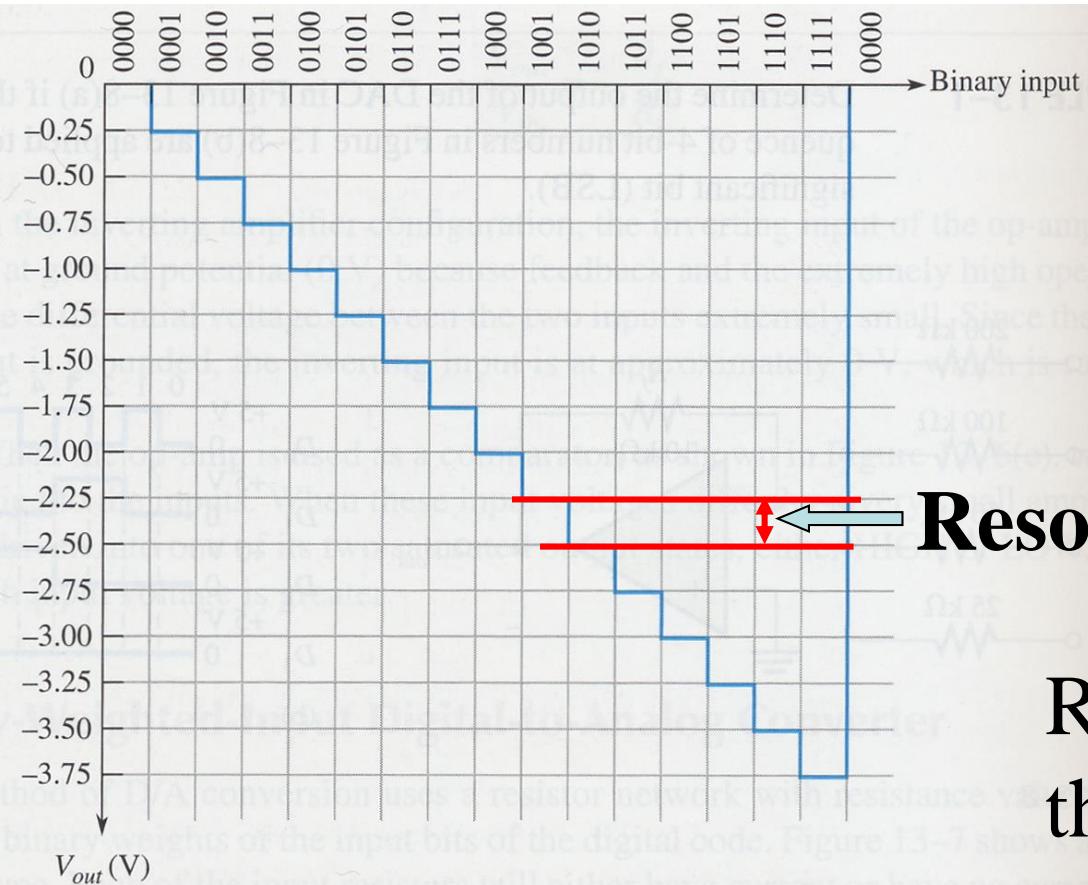
# Performance Characteristics of DAC



- Resolution ✓
- Accuracy ✓
- Linearity
- Settling time ✓
- Monotonicity

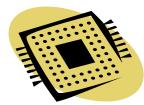
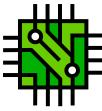


# Resolution: the reciprocal of the number of discrete steps in the D/A output.



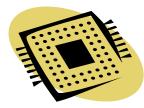
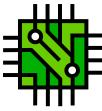
**Resolution**

Resolution dependent on the number of input bits



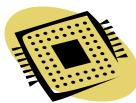
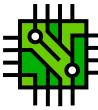
## • Expression of resolution:

- $\text{resolution} = \frac{1}{2^n - 1} \times 100\%$
- The number of input bits :  $n$



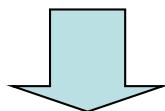
# Example

- For a 12-bit DAC and a 16-bit DAC, calculate the resolution in percentage form.

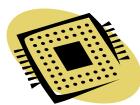
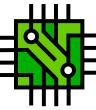


# Accuracy

- Comparison of the actual output of DAC with the expected output.
- Expressed as a percentage of a full-scale, or maximum of output voltage.  
e.g. accuracy =  $\pm 0.1\%$   
full-scale output = 10V



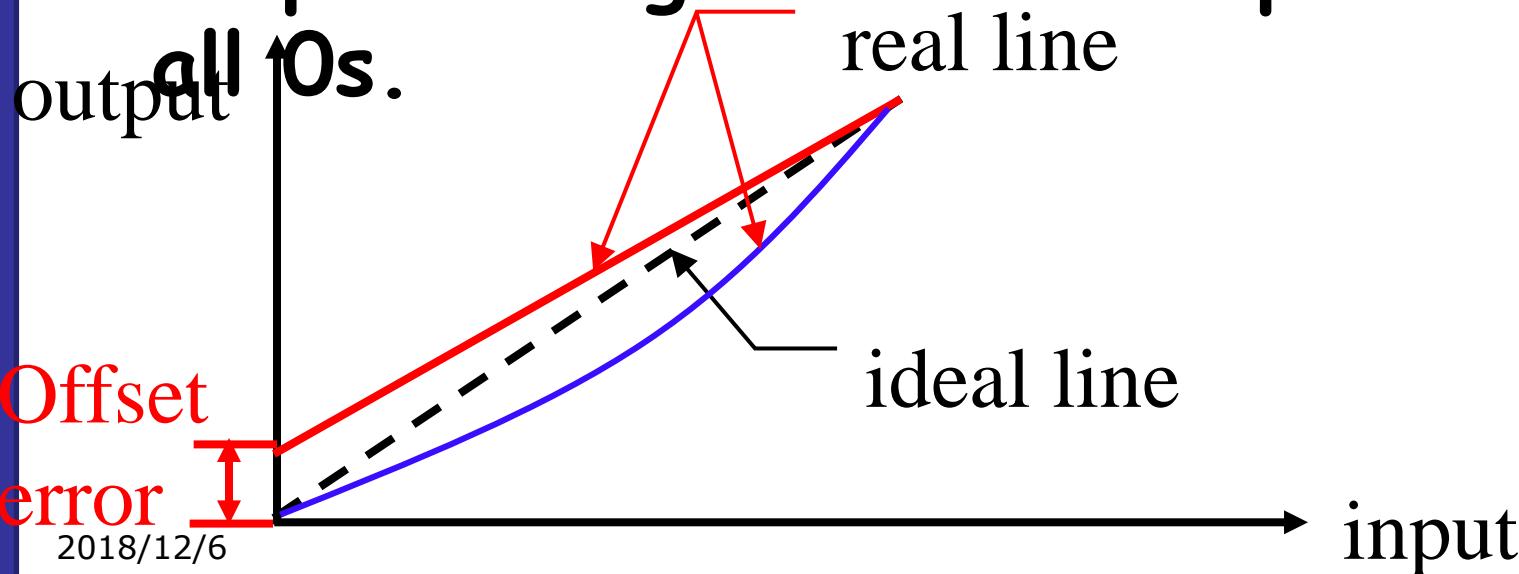
$$\text{maximum error} = (10\text{V}) \times 0.1\% = 10\text{mV}$$



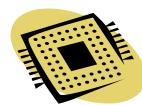
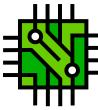
# Linearity

A linear error is a derivation from the ideal straight-line output of a DAC.

e.g. offset error : the amount of output voltage when the input bits are all 0s.

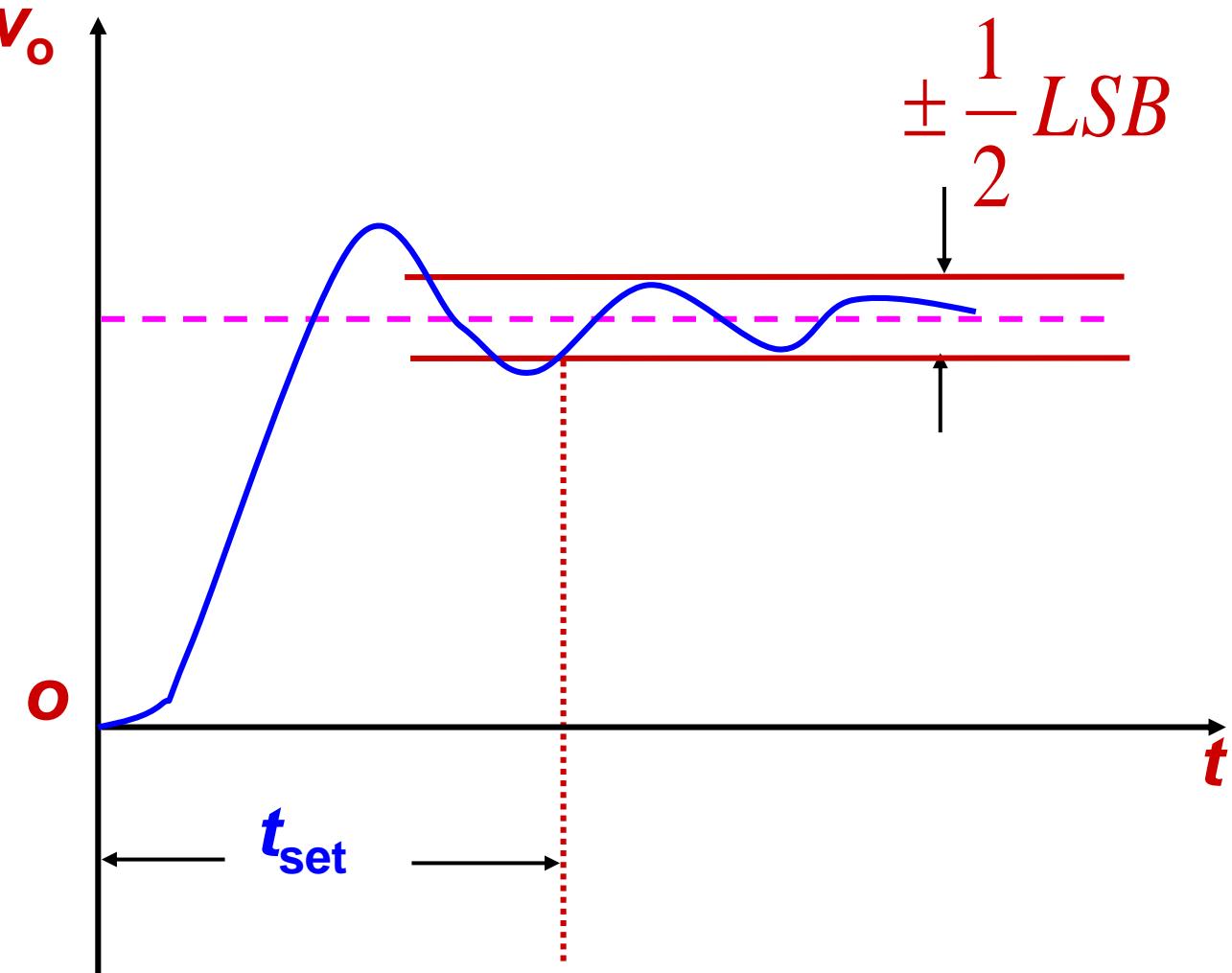
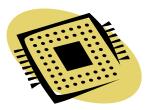
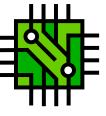


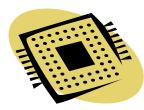
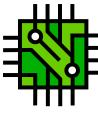
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# Settling time

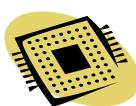
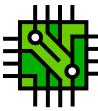
- The time that it takes a DAC to settle within  $\pm \frac{1}{2}$  LSB of its final value when a change occurs in the input code.
- The time for the analog output to stabilize after the digital input is applied



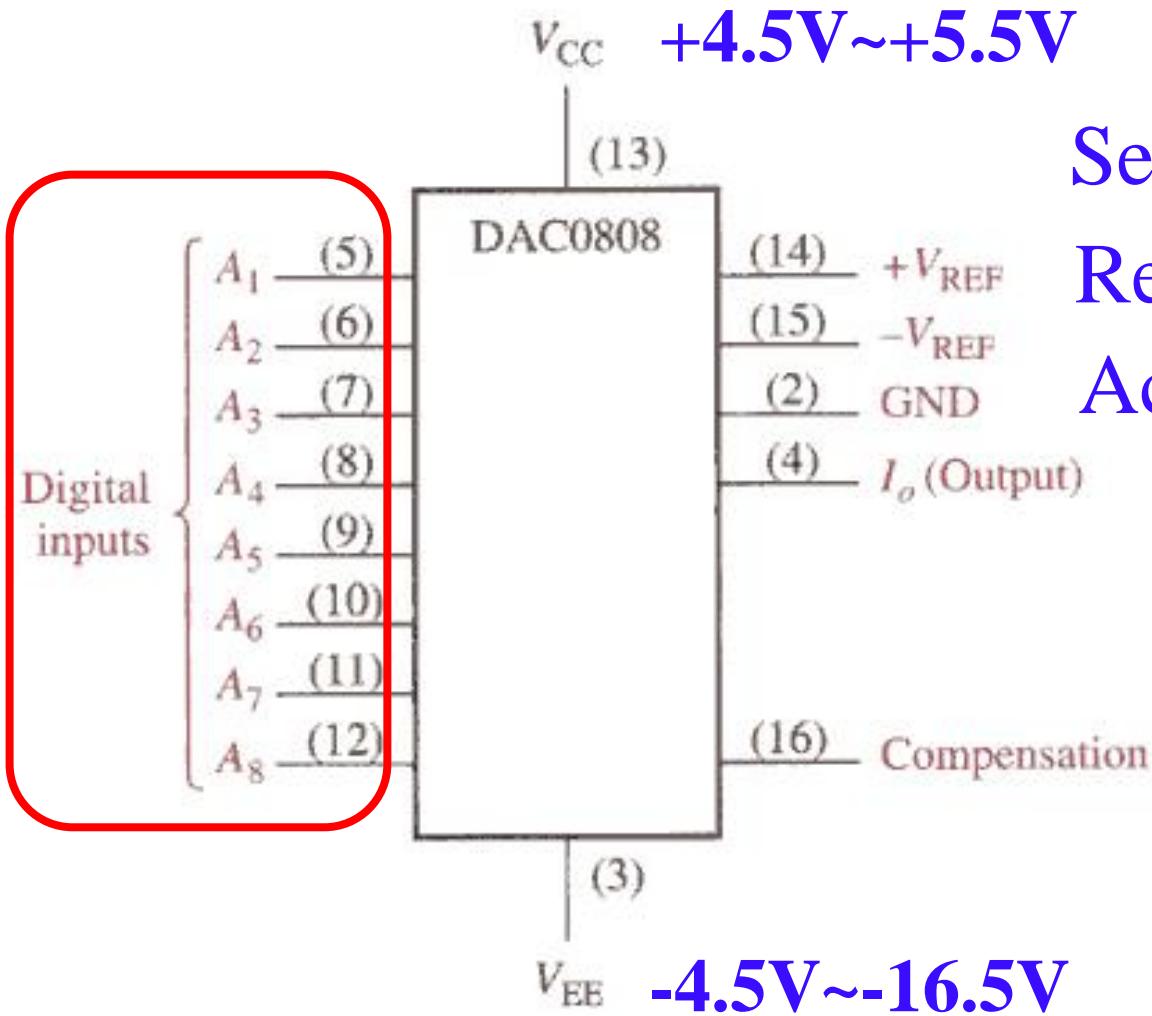


# Monotonicity

A DAC is monotonic if it does not take any reverse steps when it is sequenced over its entire range of input bits.



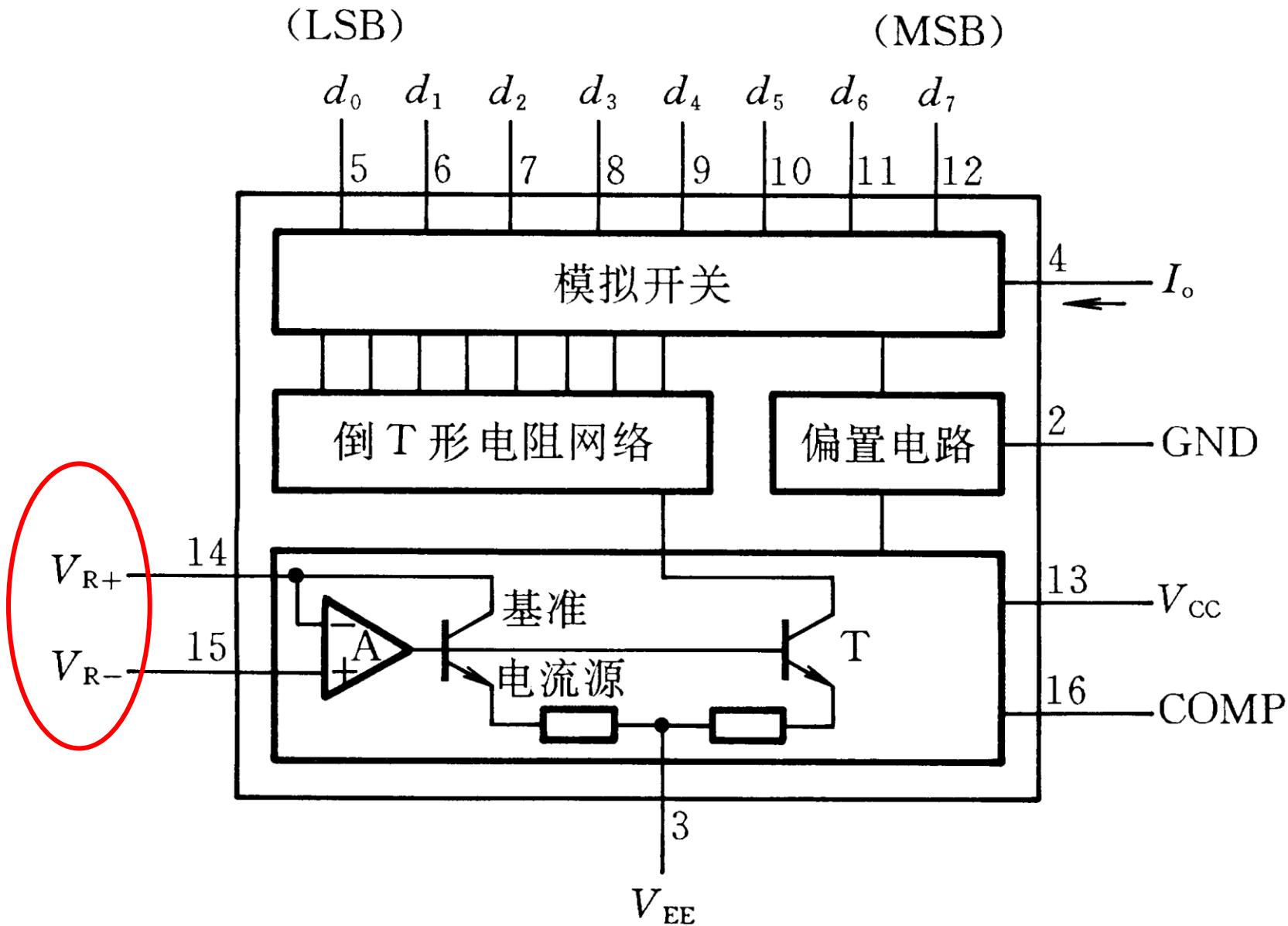
# MSI Chips: DAC8088

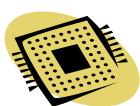
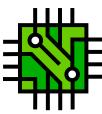


Settling time : 150ns

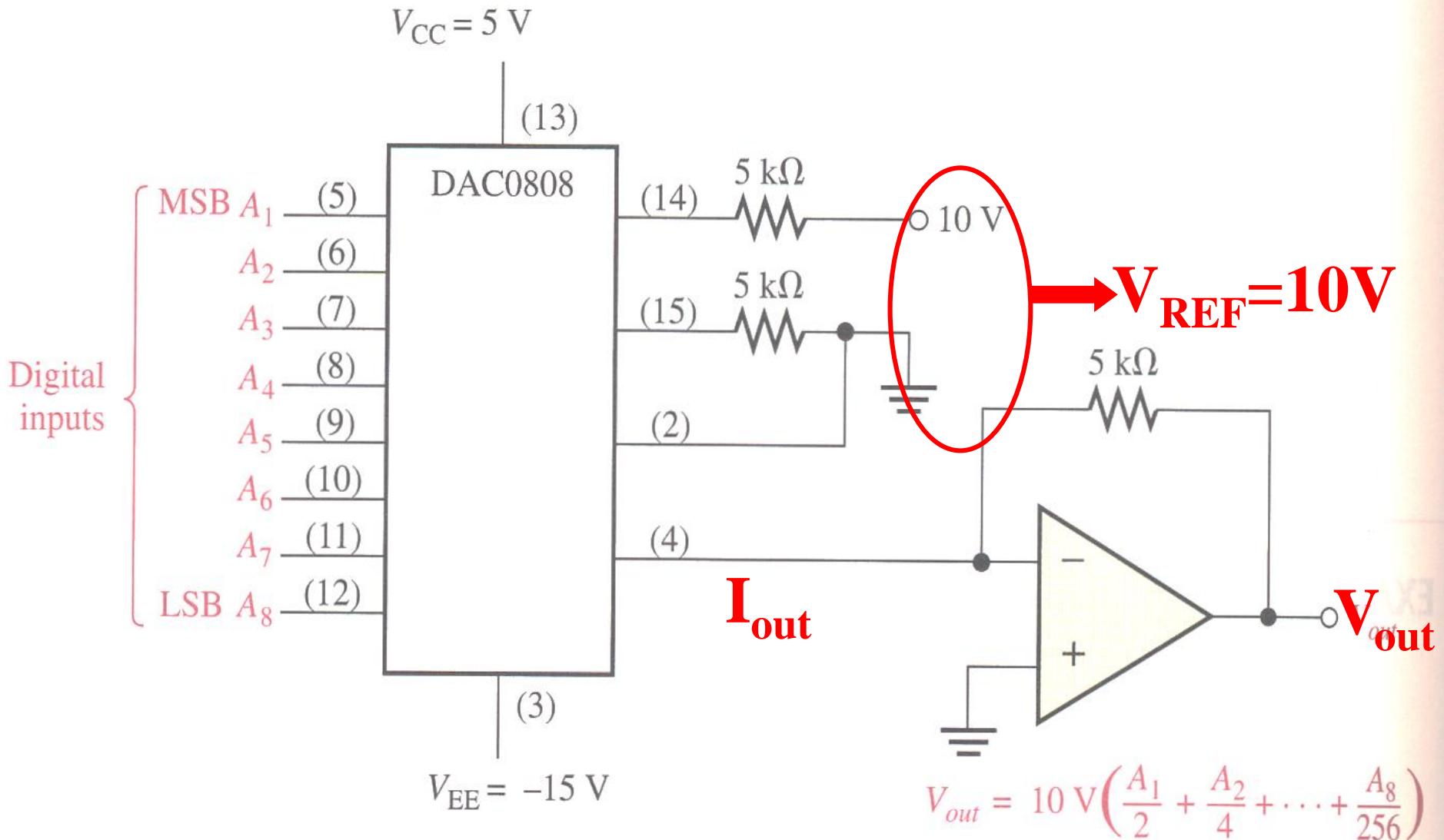
Resolution: 8 bits

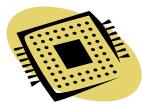
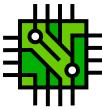
Accuracy :  $\pm 0.19\%$





# Example of Application



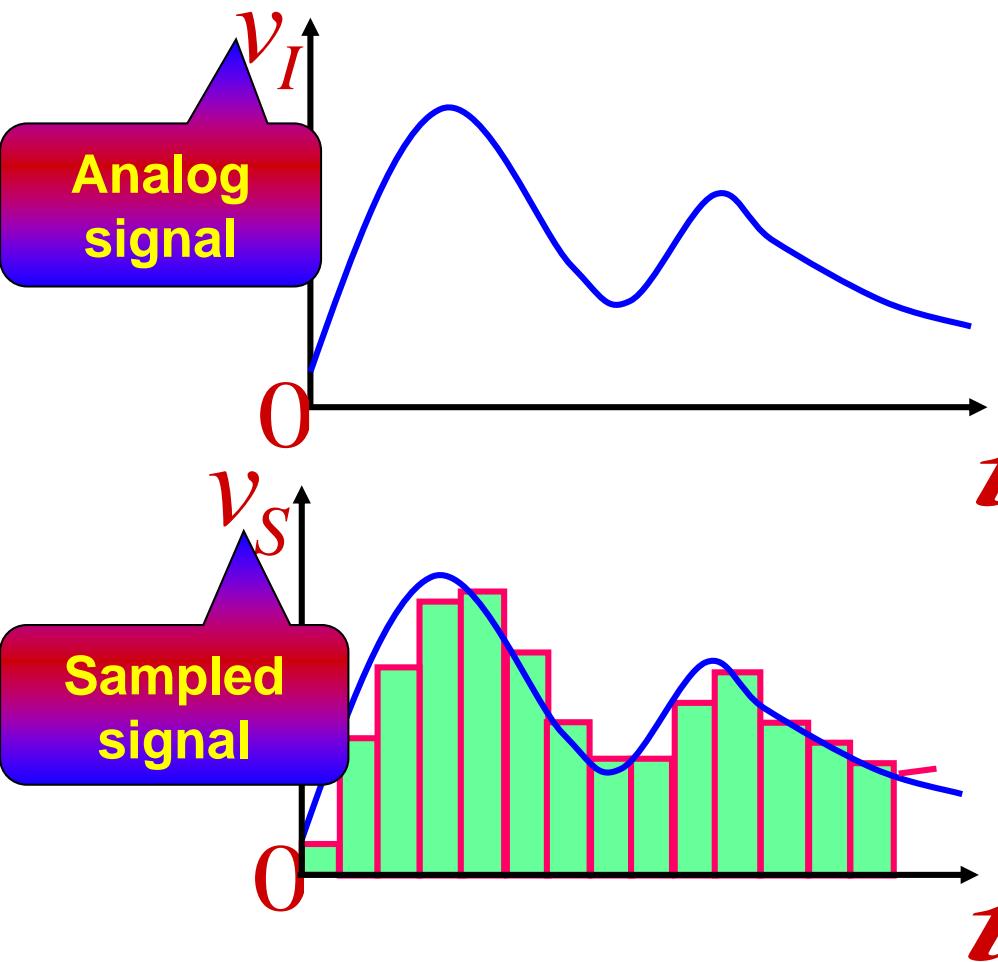


## 2 Analog-to-digital Conversion

There are a number of approaches that can be taken for the construction of an analog-to-digital converter.

# Sampling

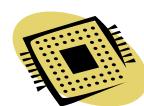
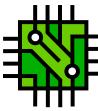
## The frequency of sampled signal must be high enough



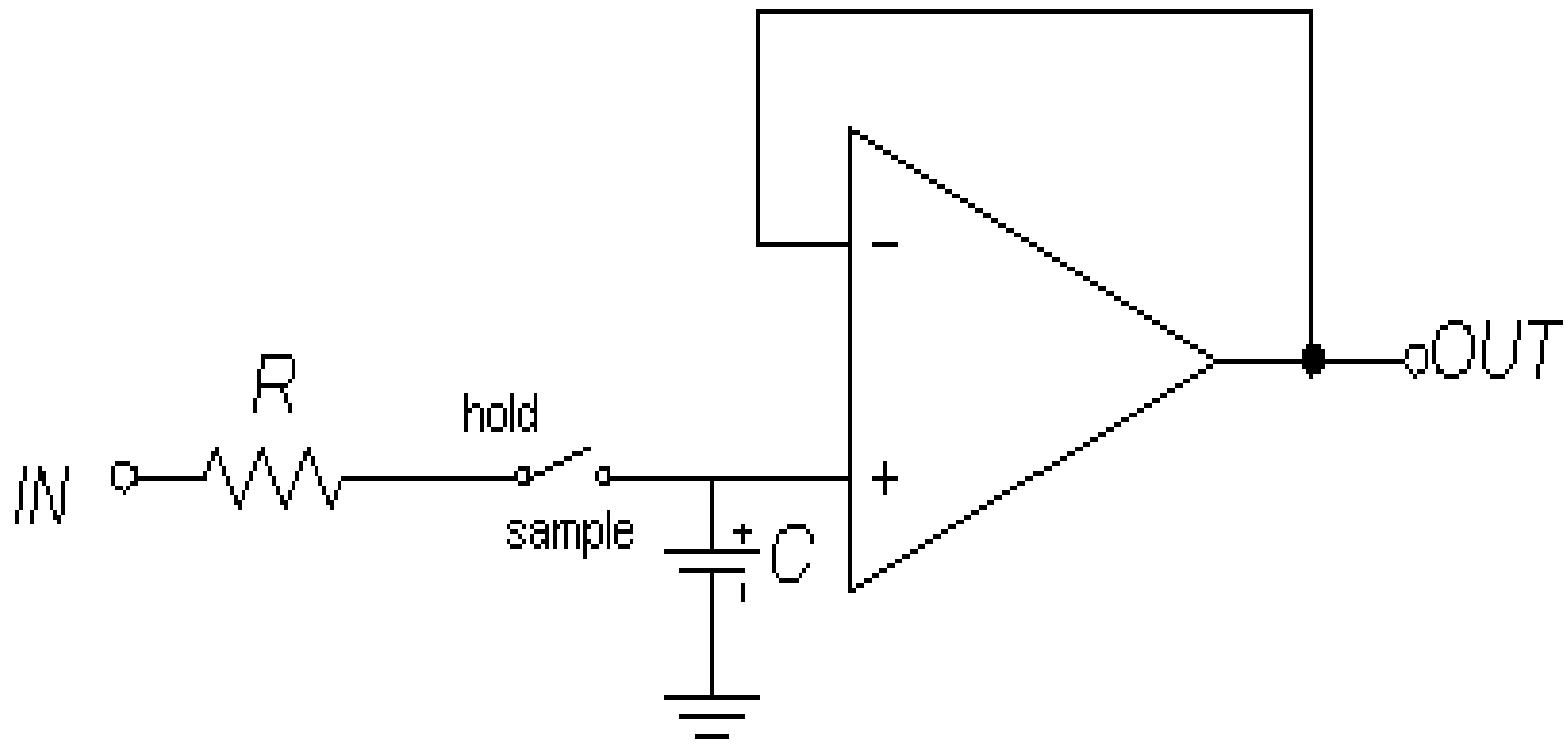
$$f_s \geq 2 f_{i(\max)}$$

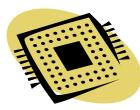
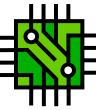
$f_s$  Sampling frequency

$f_{i(\max)}$  maximum frequency of  $v_I$

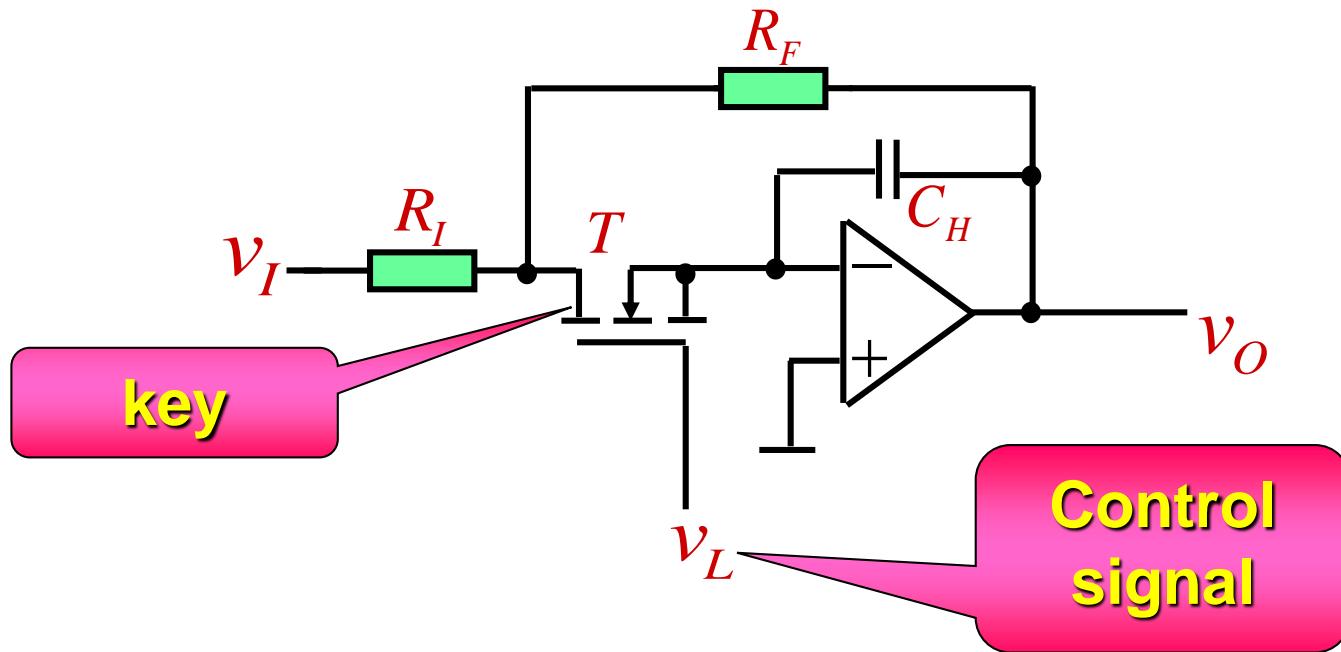


# sample-and-hold circuit



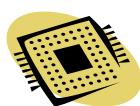
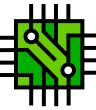


# Sample-and-hold circuit

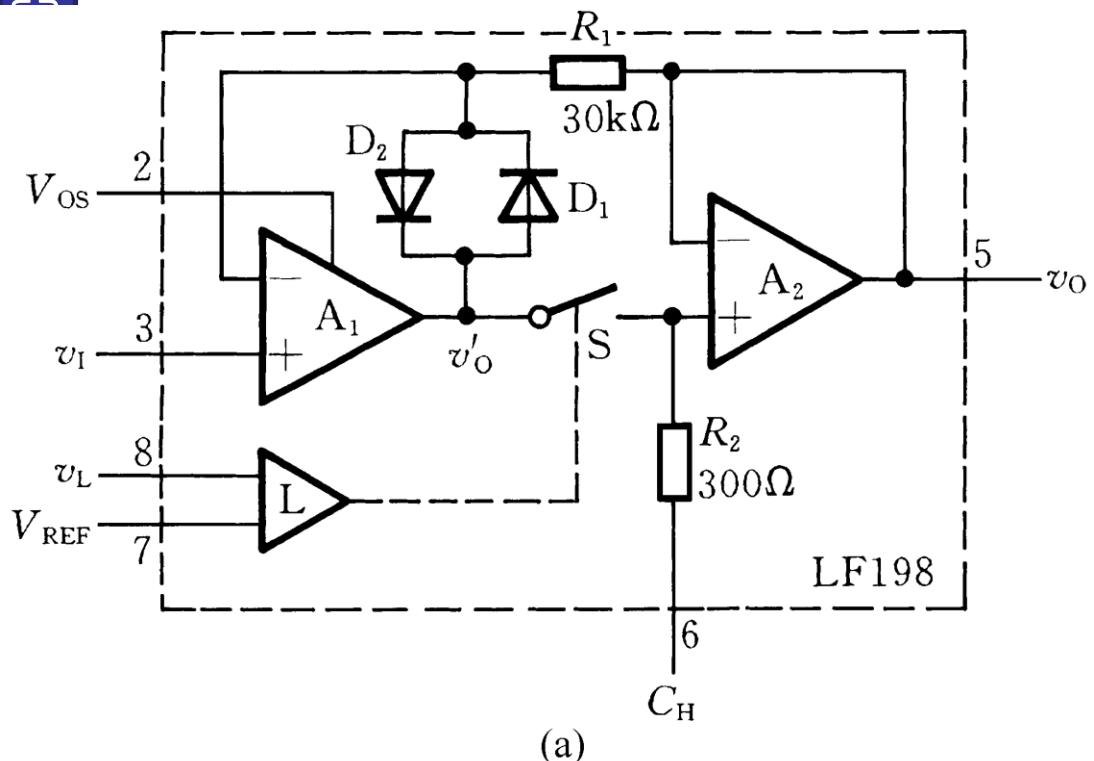


$v_L$  is HIGH T switch on, sampling

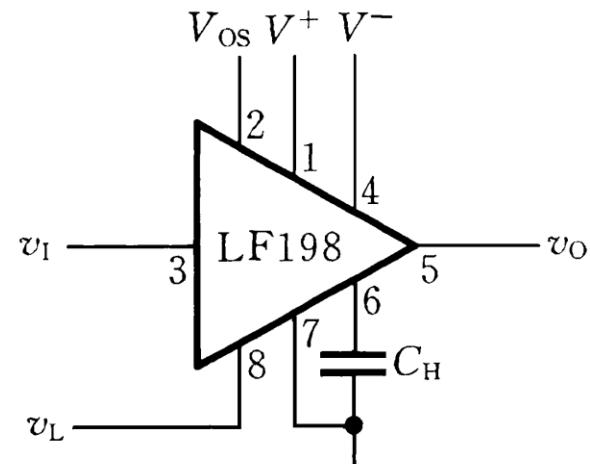
$v_L$  is LOW T switch off, holding



# MSI: LF198



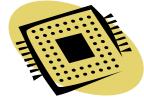
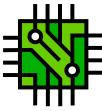
(a)



(b)

structure

Typical application



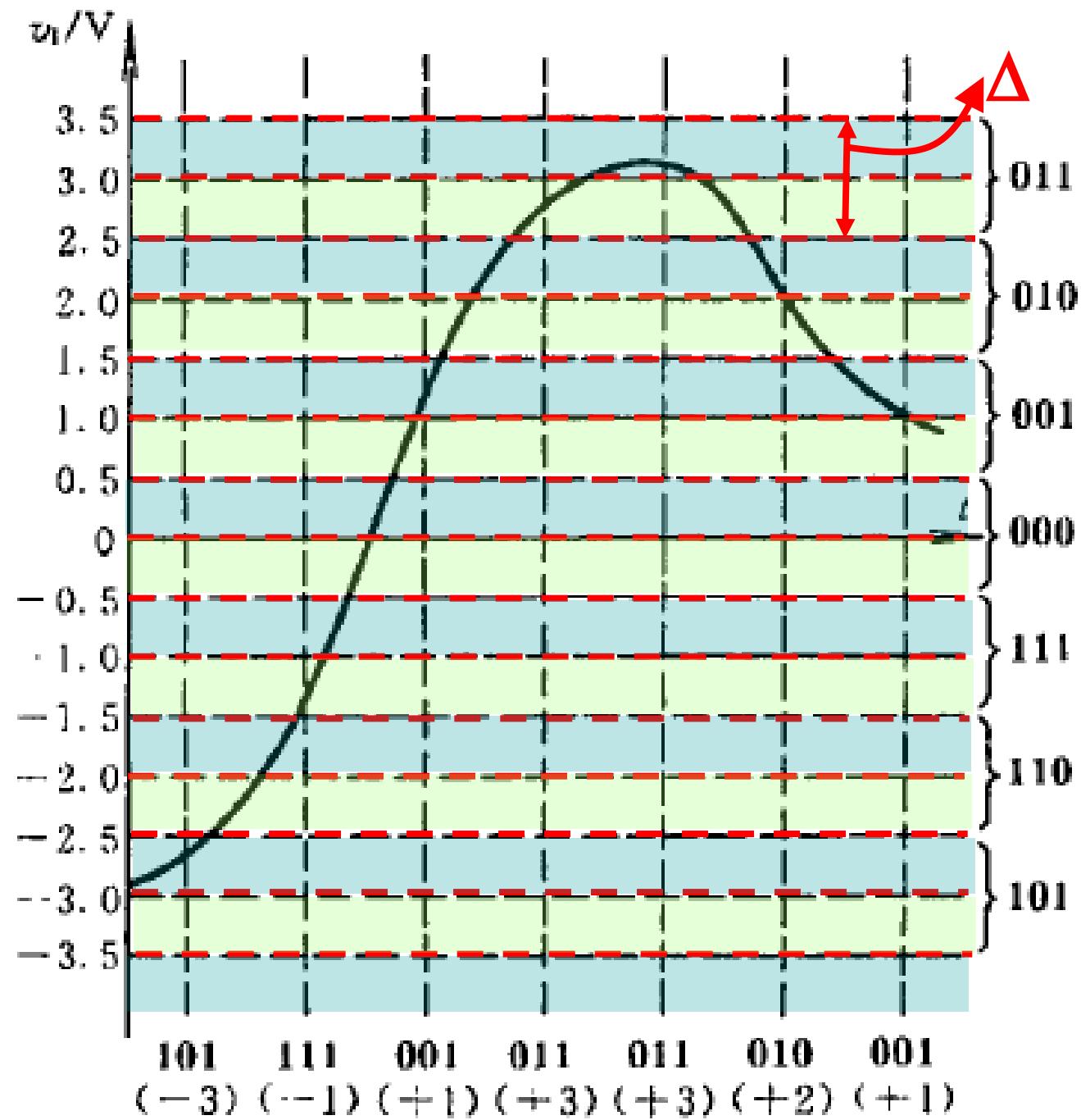
# Quantization: A/D conversion

**Quantization unit:**  $\Delta$  (voltage that represents LSB)

**Coding:** encode the result of quantization (A/D Conversion)

**Quantization error:** the error due to quantization

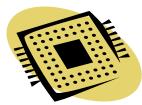
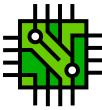
# Example for quantization





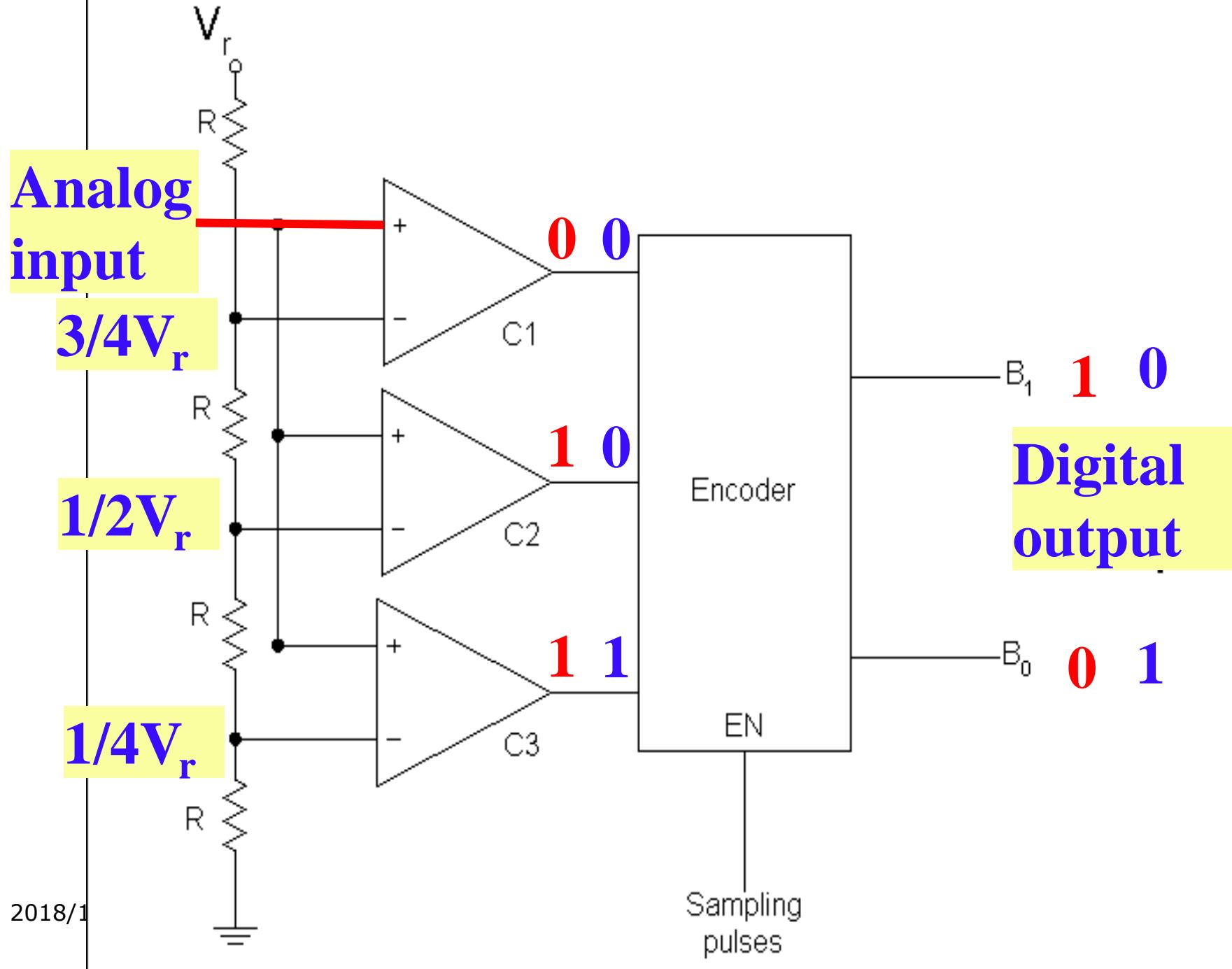
# Analog-to-digital converterS

- Flash ADC
- Stairstep-Ramp ADC
- Tracking ADC

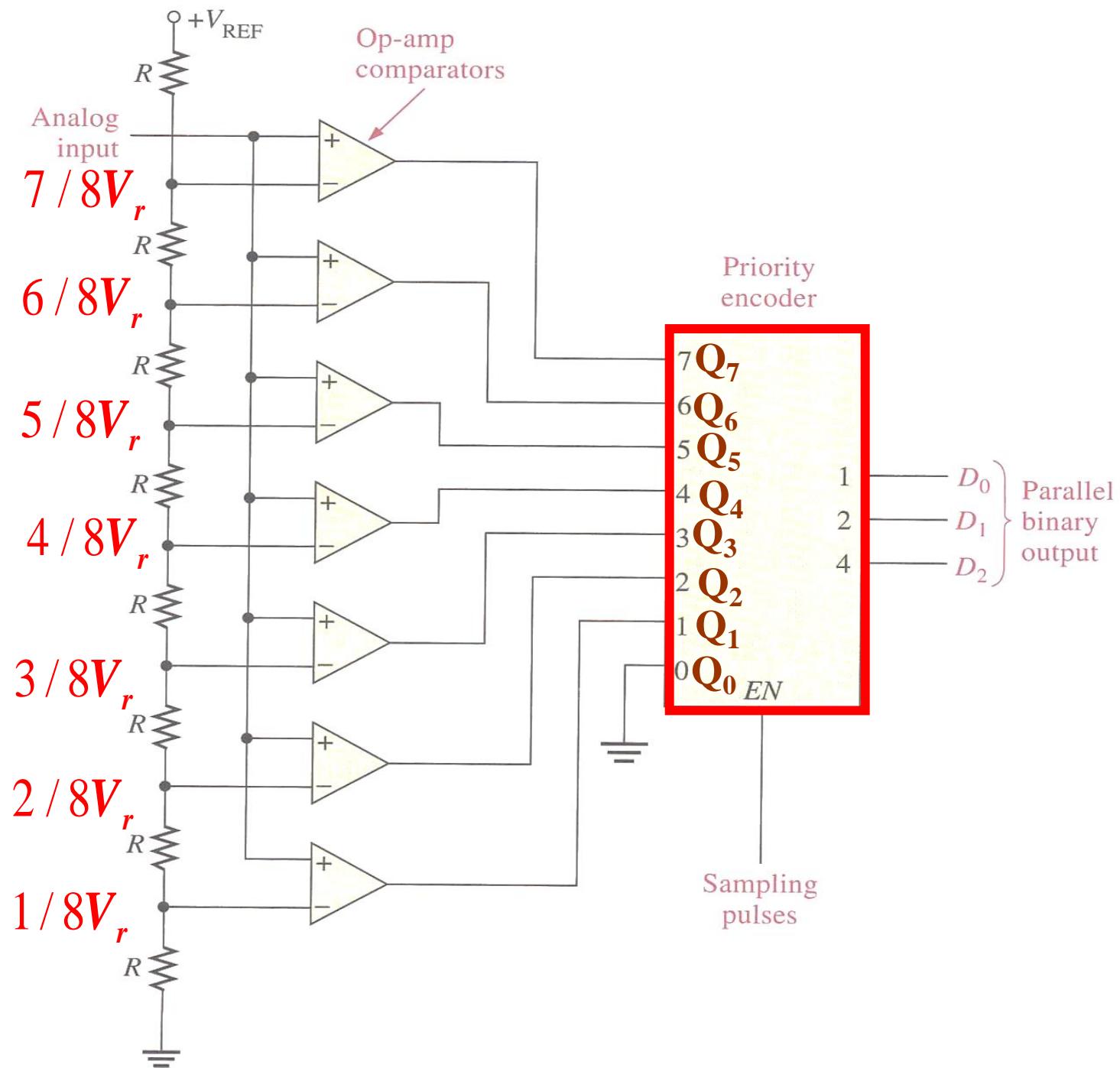


# Flash Analog-to-digital converter

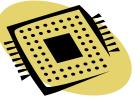
- Using comparators to compare reference voltages with the analog input voltage.



# 3-bit flash ADC



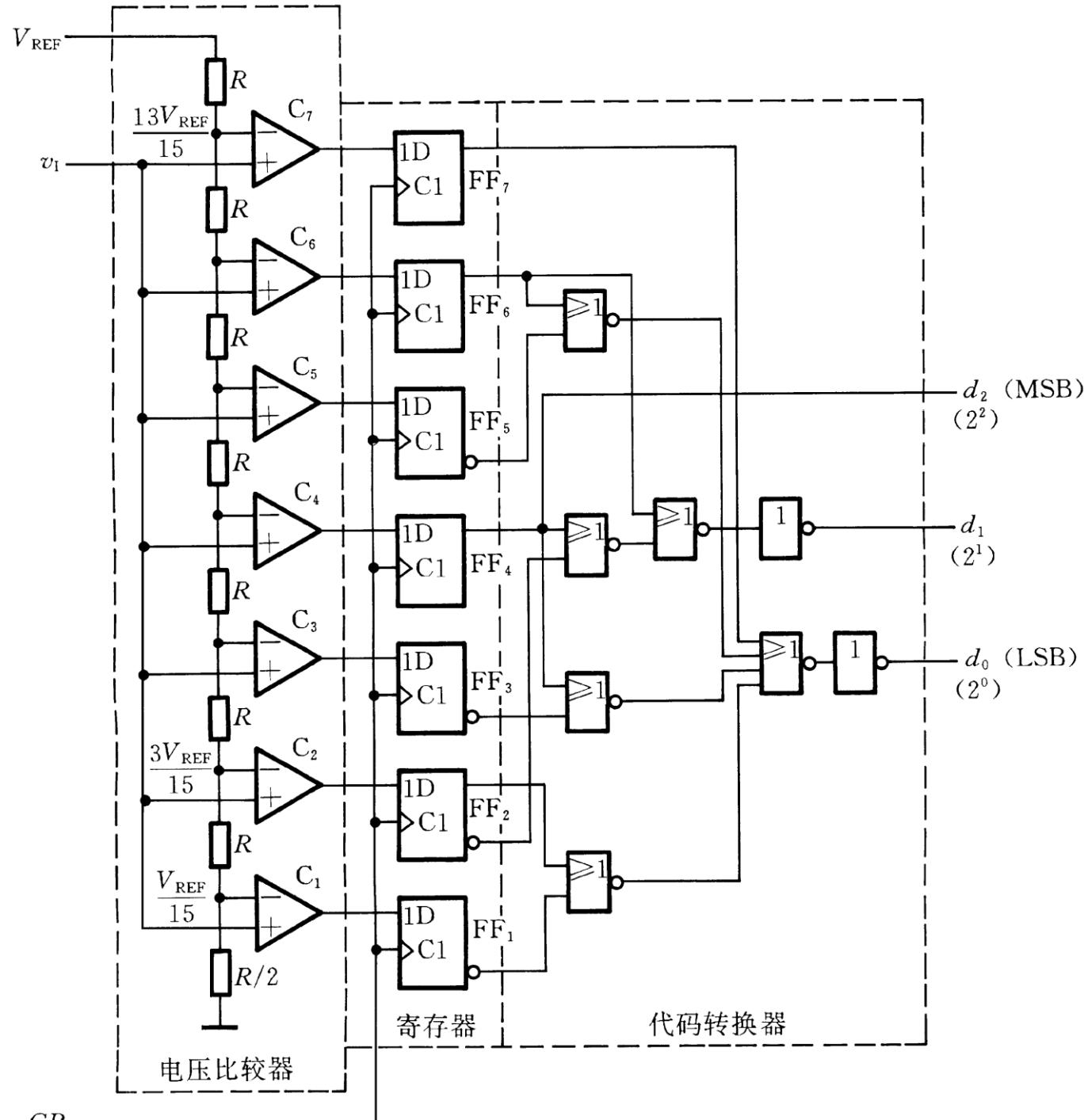
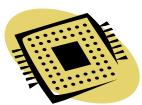


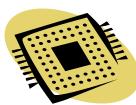
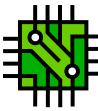


$$d_2 = Q_4$$

$$d_1 = Q_6 + \bar{Q}_4 Q_2$$

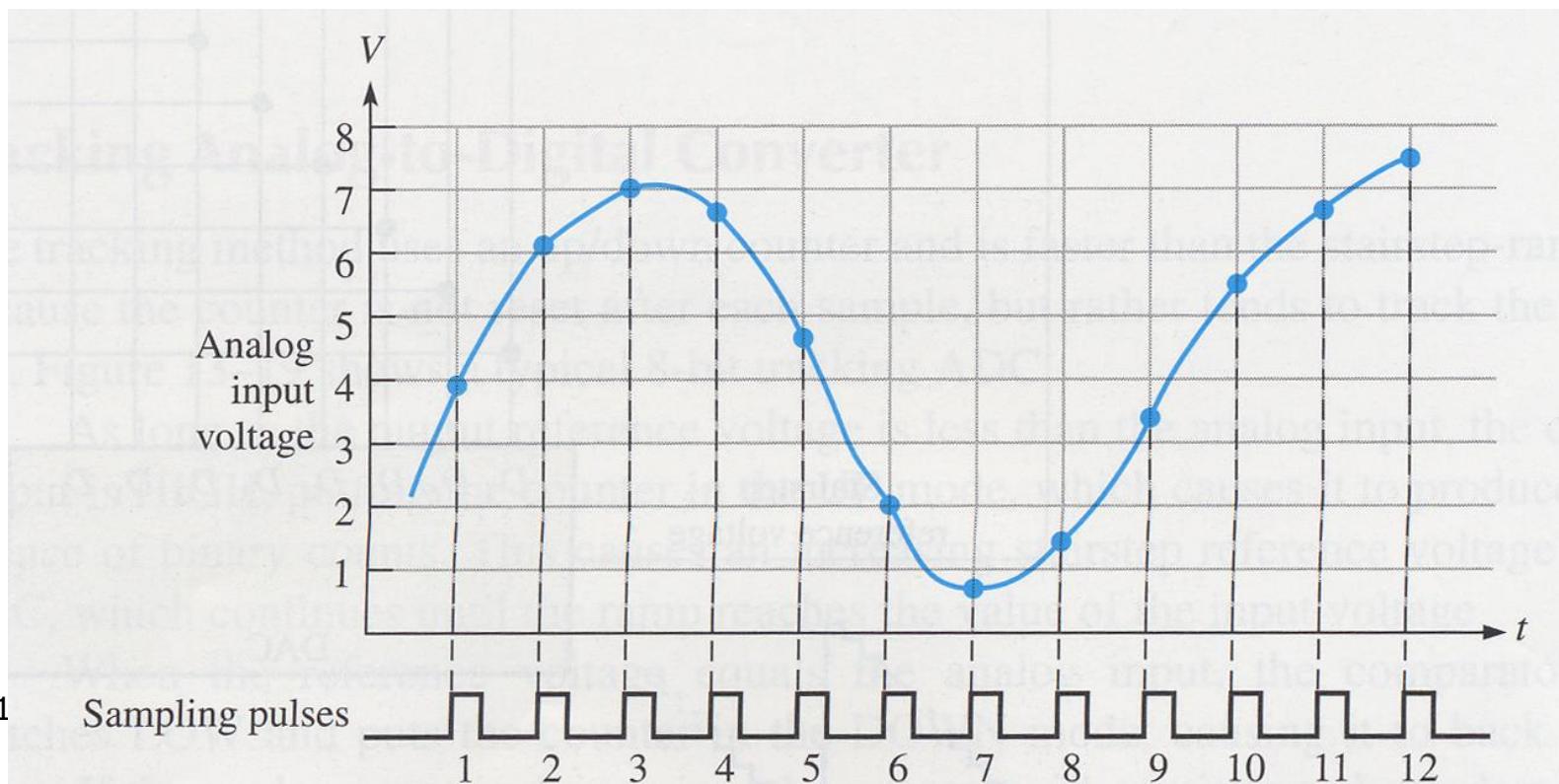
$$d_0 = Q_7 + \bar{Q}_6 Q_5 + \bar{Q}_4 Q_3 + \bar{Q}_2 Q_1$$

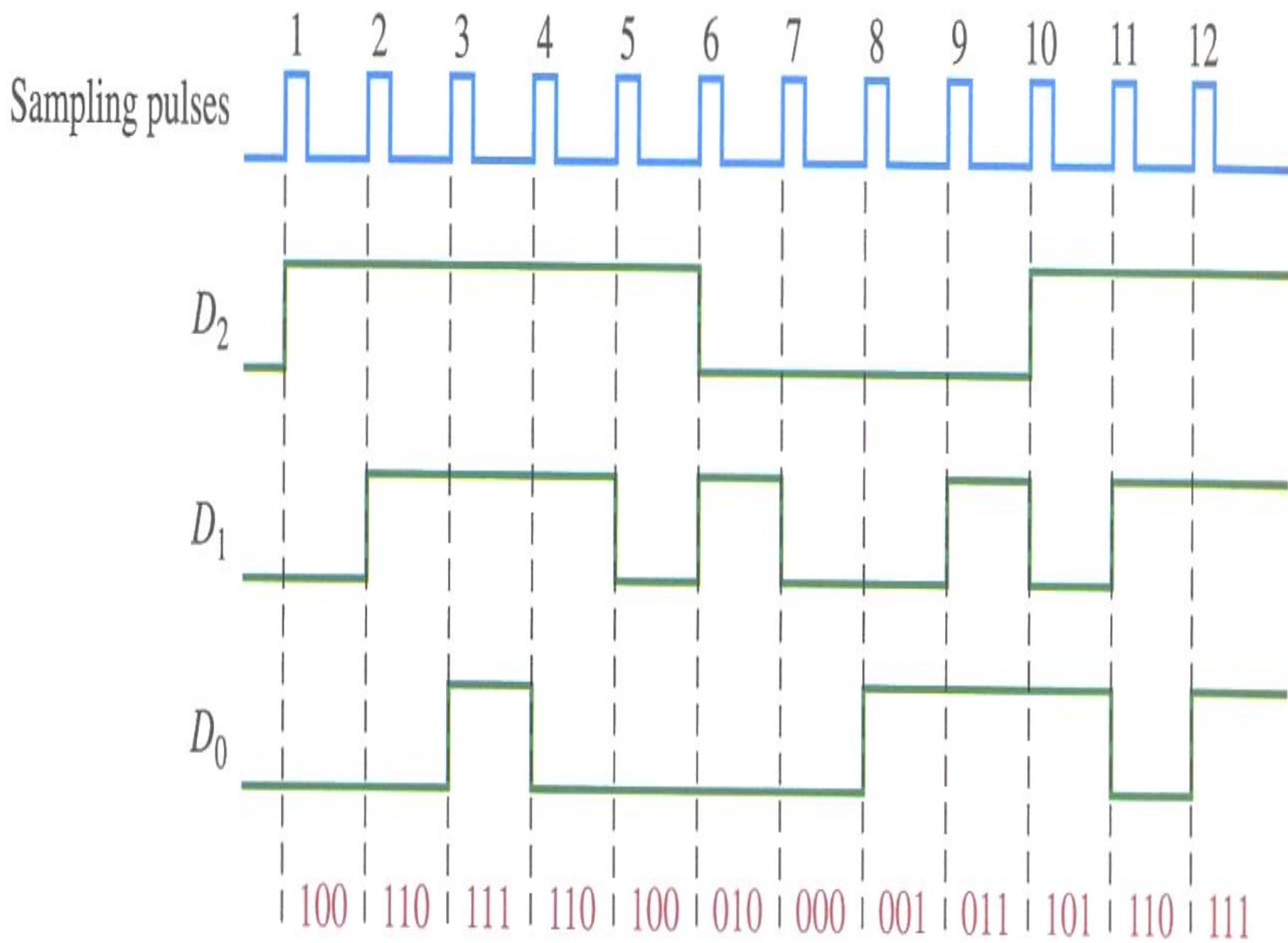


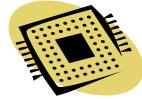
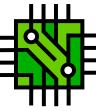


# Exercise

- Determine the binary code output of 3-bit flash ADC for the analog input signal in figure and the sampling pulses. Assume  $V_{REF}=8V$ .

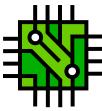




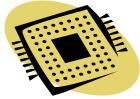


## Flash ADC

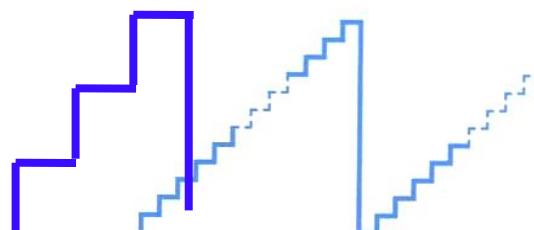
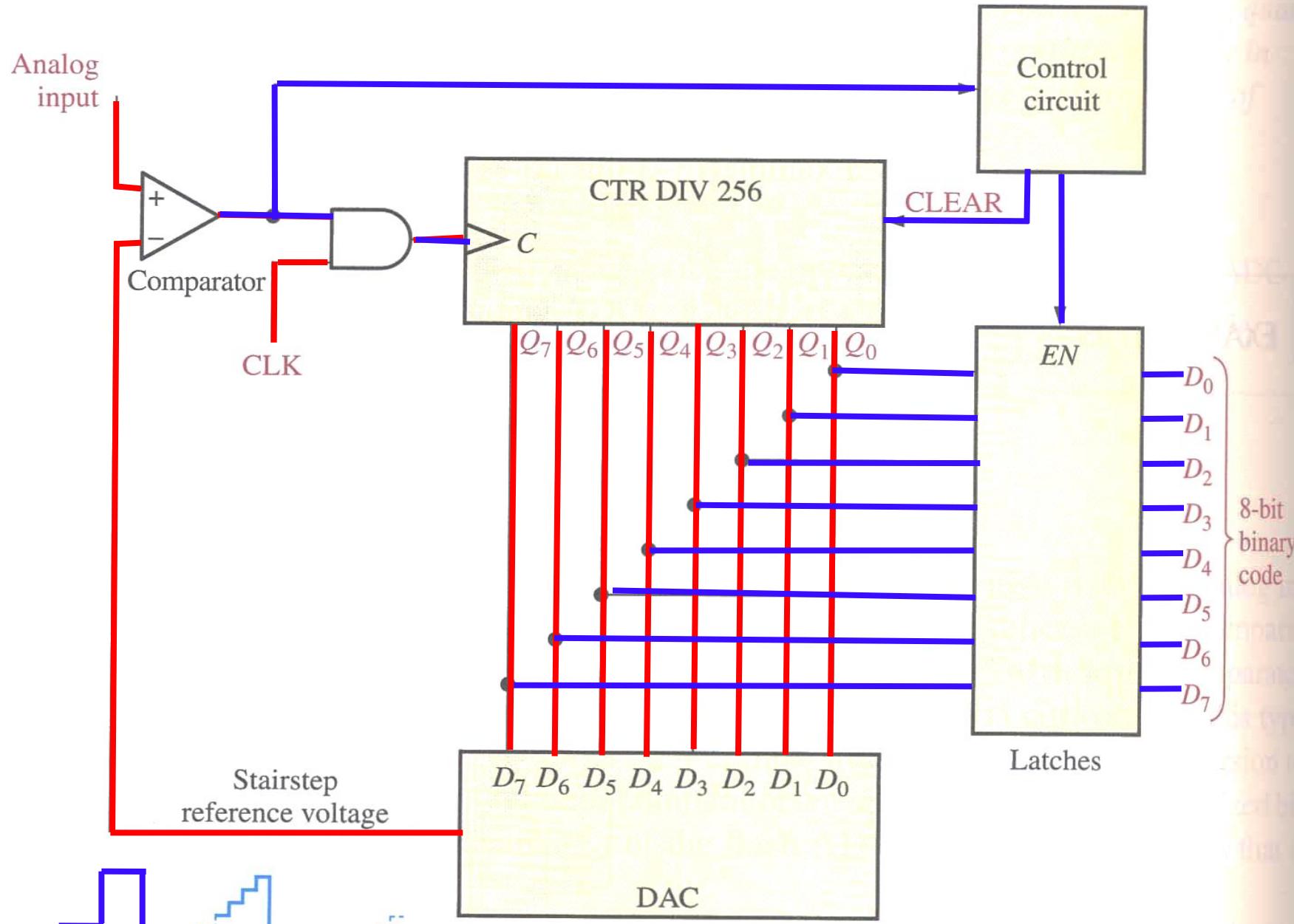
- High speed e.g. 8-bit ADC < 50ns
- Number of comparator and flip-flops increasing dramatically with the number of output bits increasing
  - e.g. for  $n$  bit output:  $2^n - 1$  comparators
  - $2^n - 1$  flip-flops



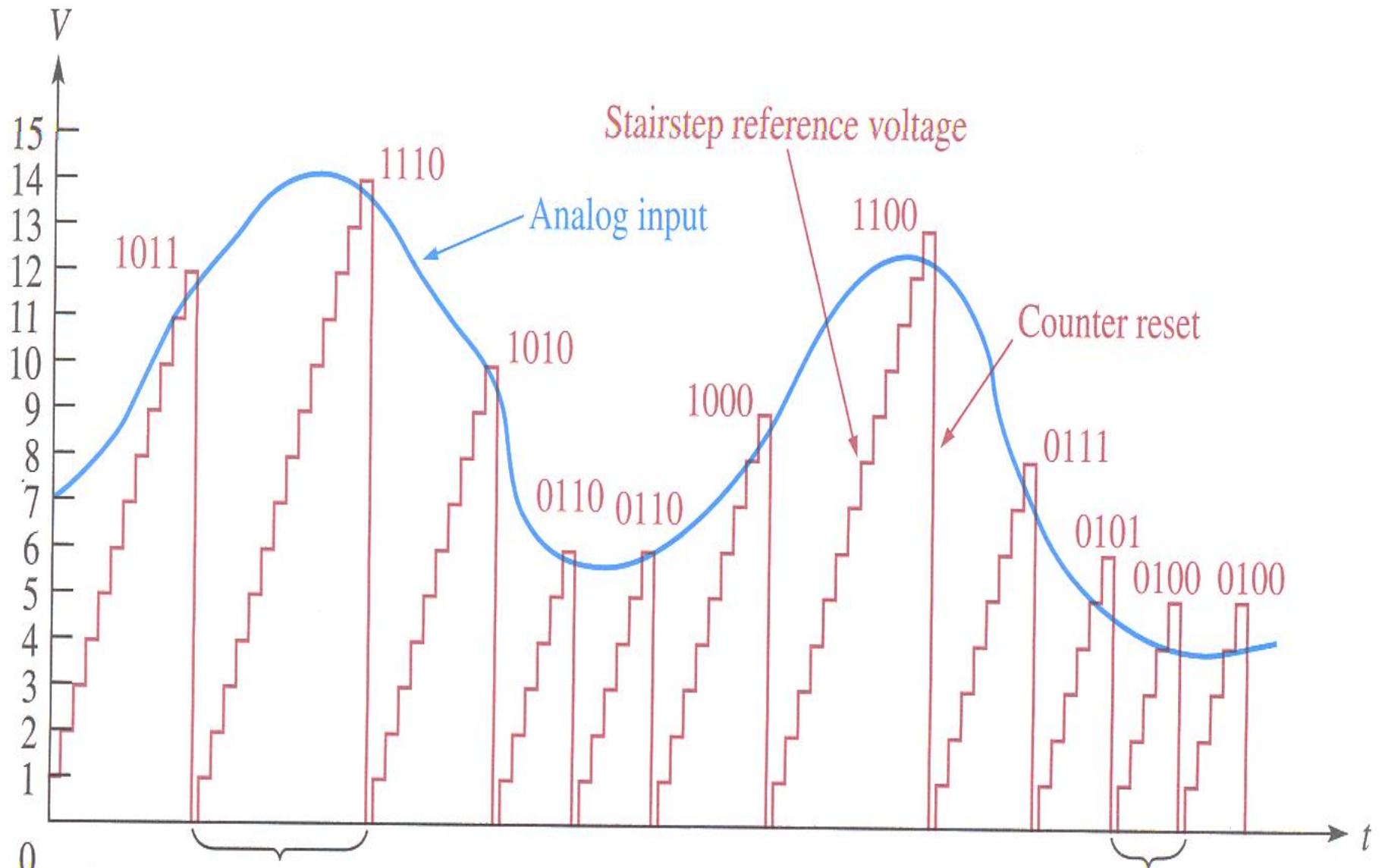
# Stairstep-Ramp Analog-to-digital Converter



- Stairstep-Ramp ADC: digital-ramp or counter method



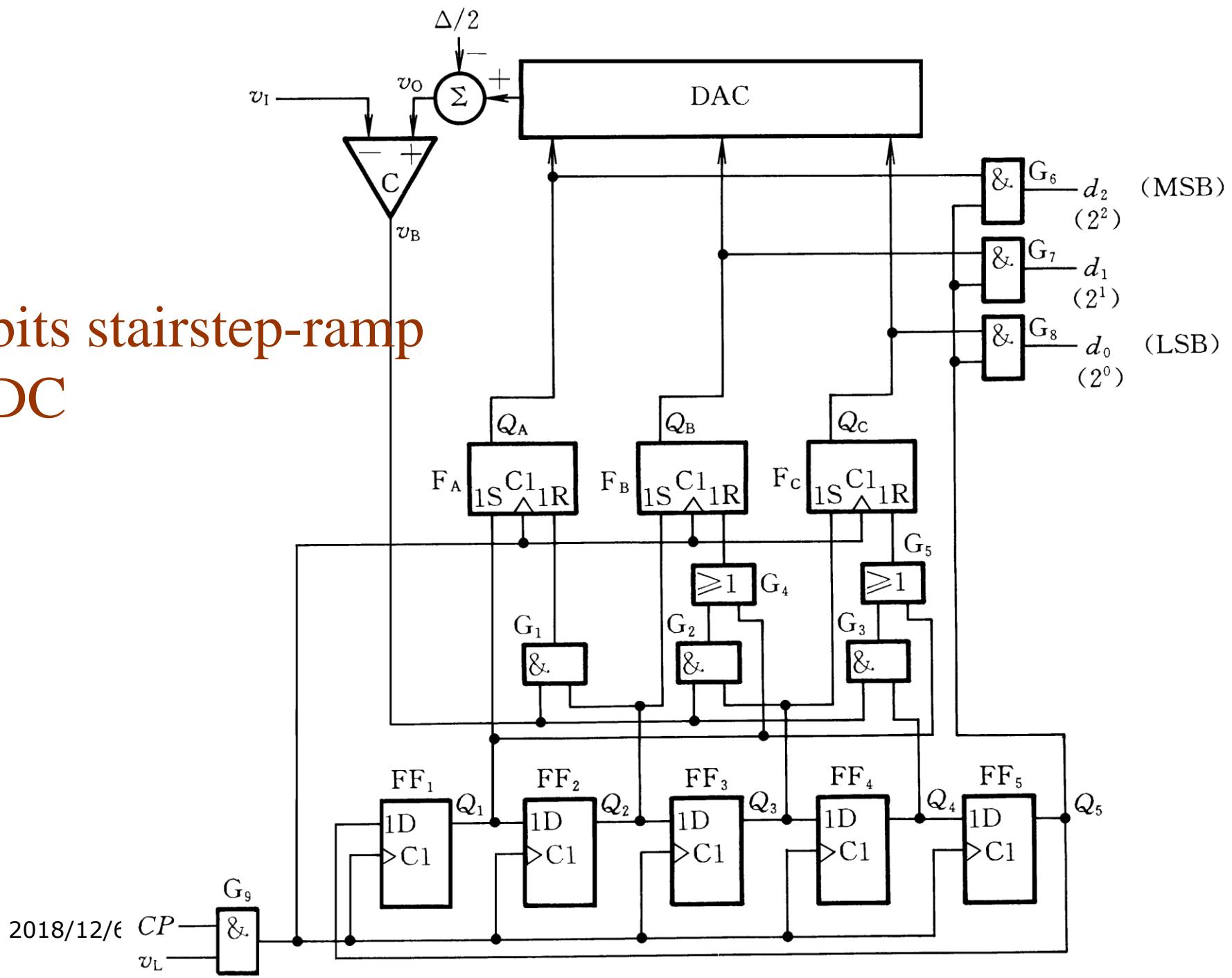
8-bit  
binary  
code

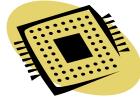


Maximum conversion time  
for these particular values

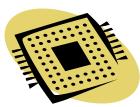
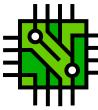
Minimum conversion time  
for these particular values

# 3 bits stairstep-ramp ADC





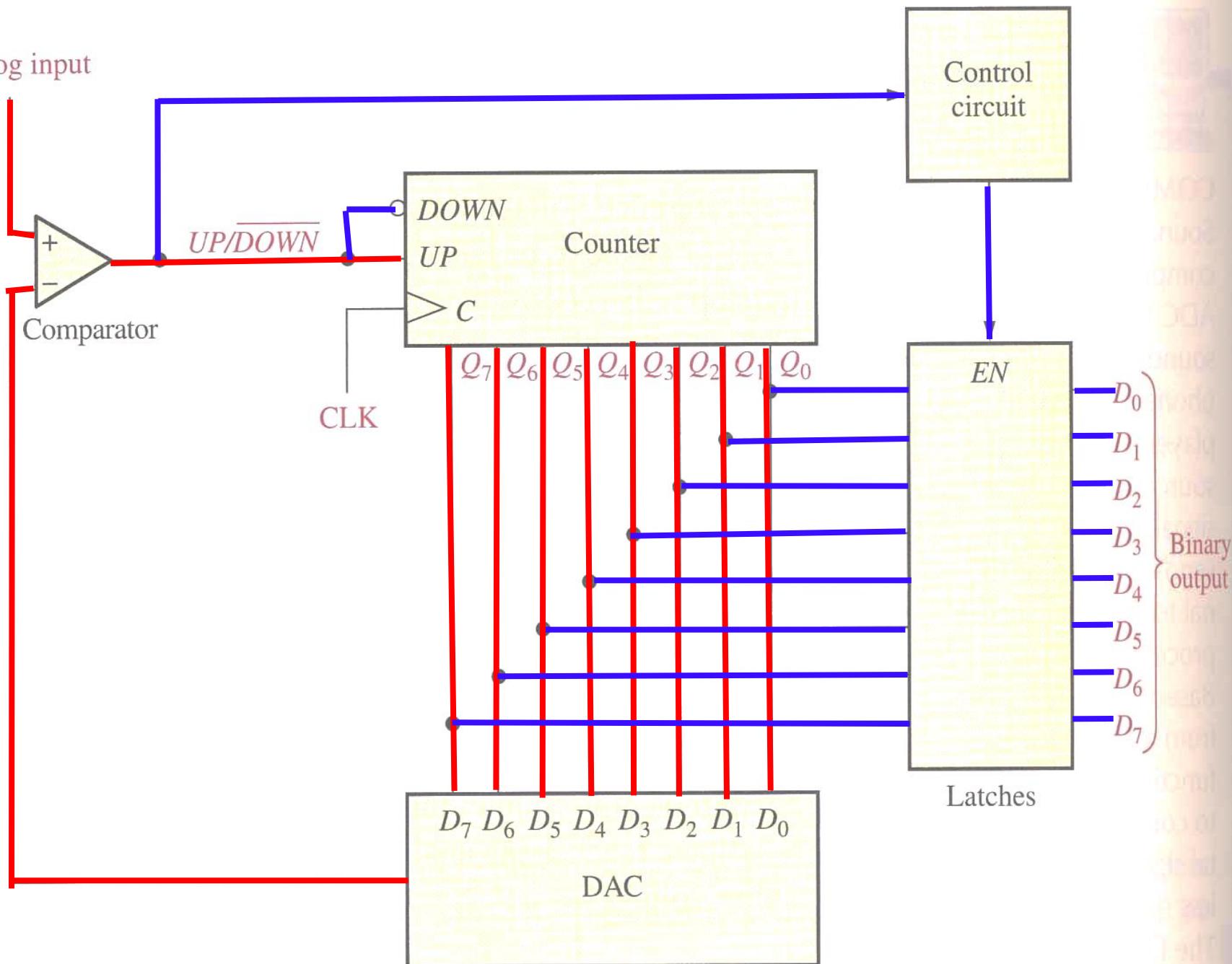
- Stairstep-ramp ADC
  - Slower than flash method ( $10\sim100\mu s$ )
  - The conversion time depending on the analog voltage

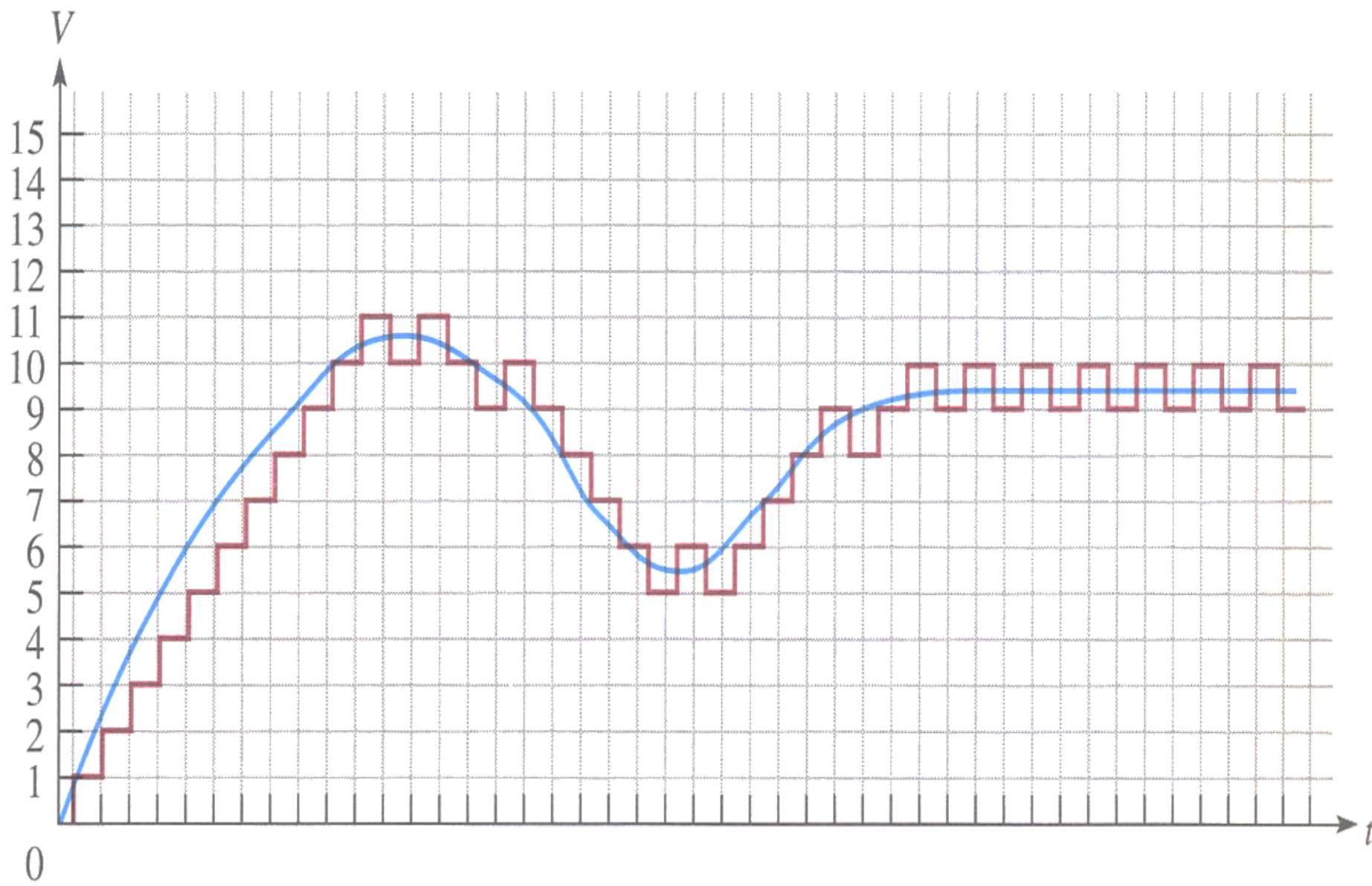


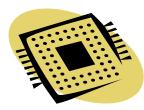
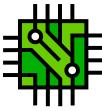
# Tracking ADC

- Using up/down counter, so it is faster than the stairstep-ramp method.

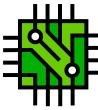
Analog input





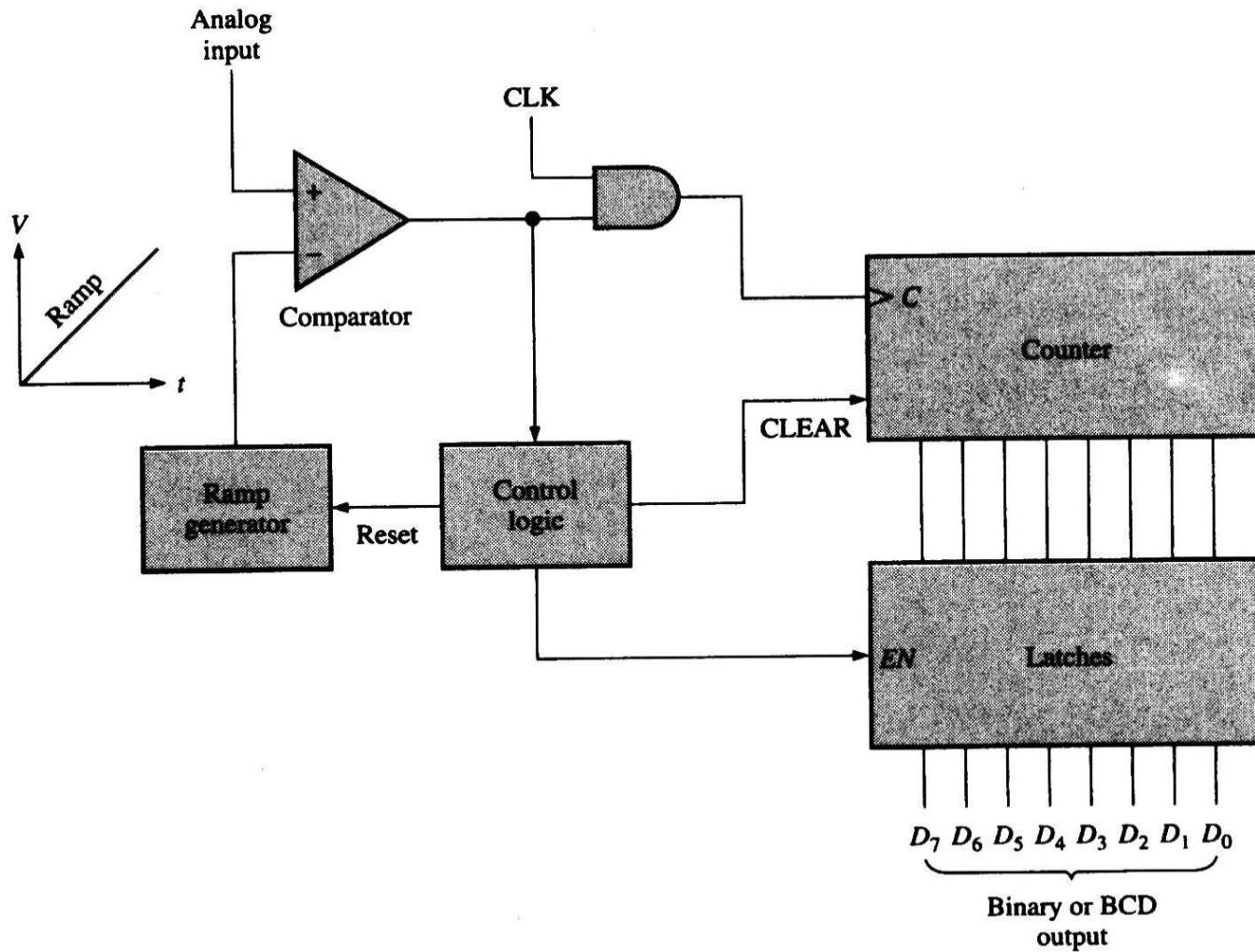


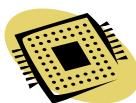
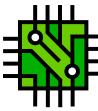
- Back-and-forth action causing an oscillation between two binary states



# Single-Slope ADC

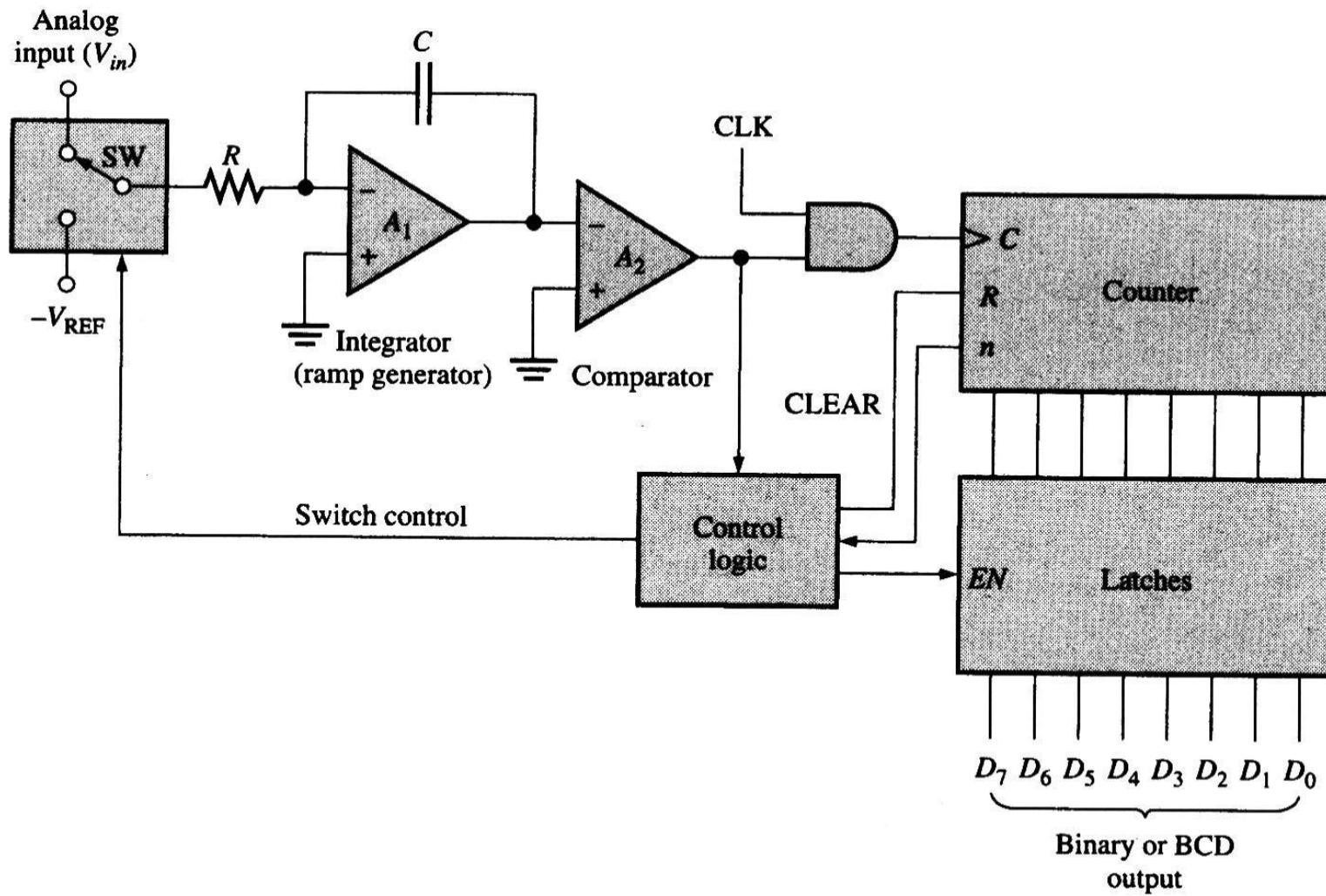
- The single-slop method uses a linear ramp generator to produce a constant-slope reference voltage.

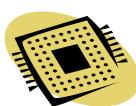
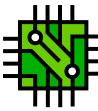




# Dual-Slope ADC

- The dual-slop method(双积分型) uses a linear ramp generator to produce a dual-slope characteristic.

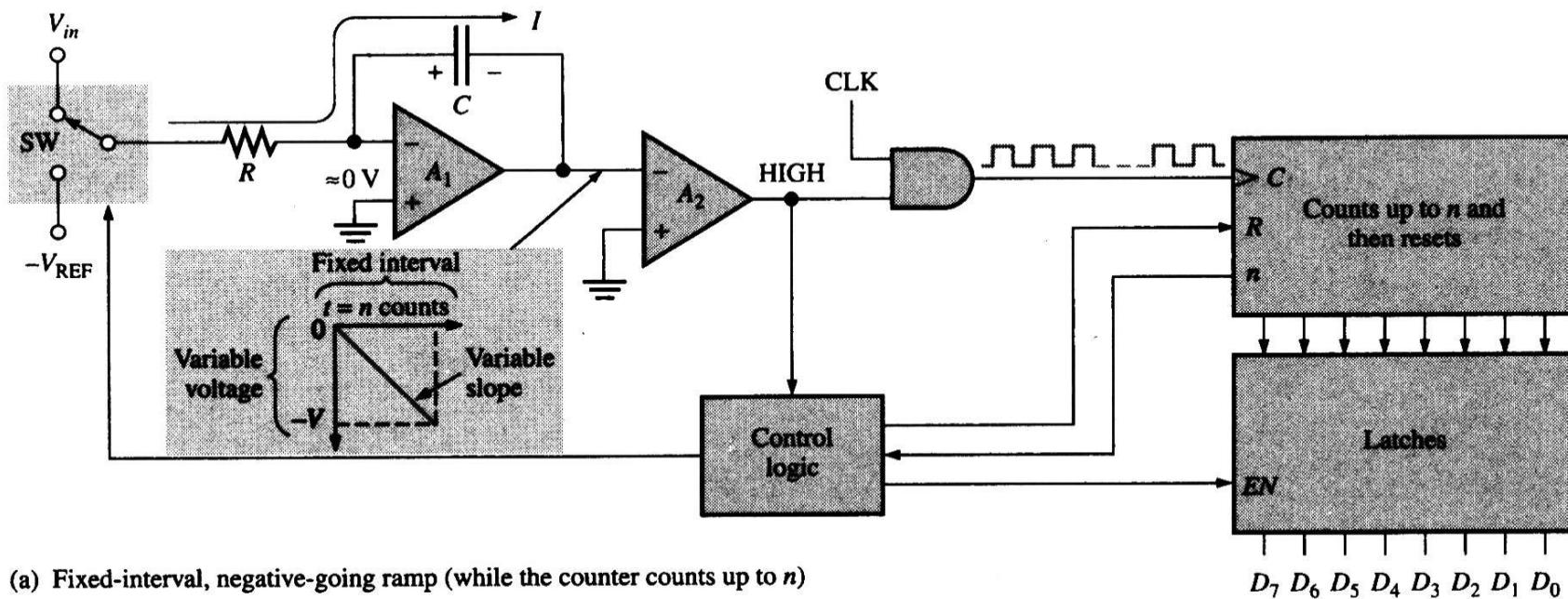


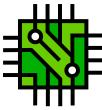


## Dual-Slope ADC

- Start by assuming that the counter is reset and the output of the integrator is zero. Now assume a positive input voltage is applied to the input through the switch as selected by the control logic.

$$v_O = \frac{1}{C} \int_0^{T_1} -\frac{v_1}{R} dt = -\frac{T_1}{RC} v_1$$

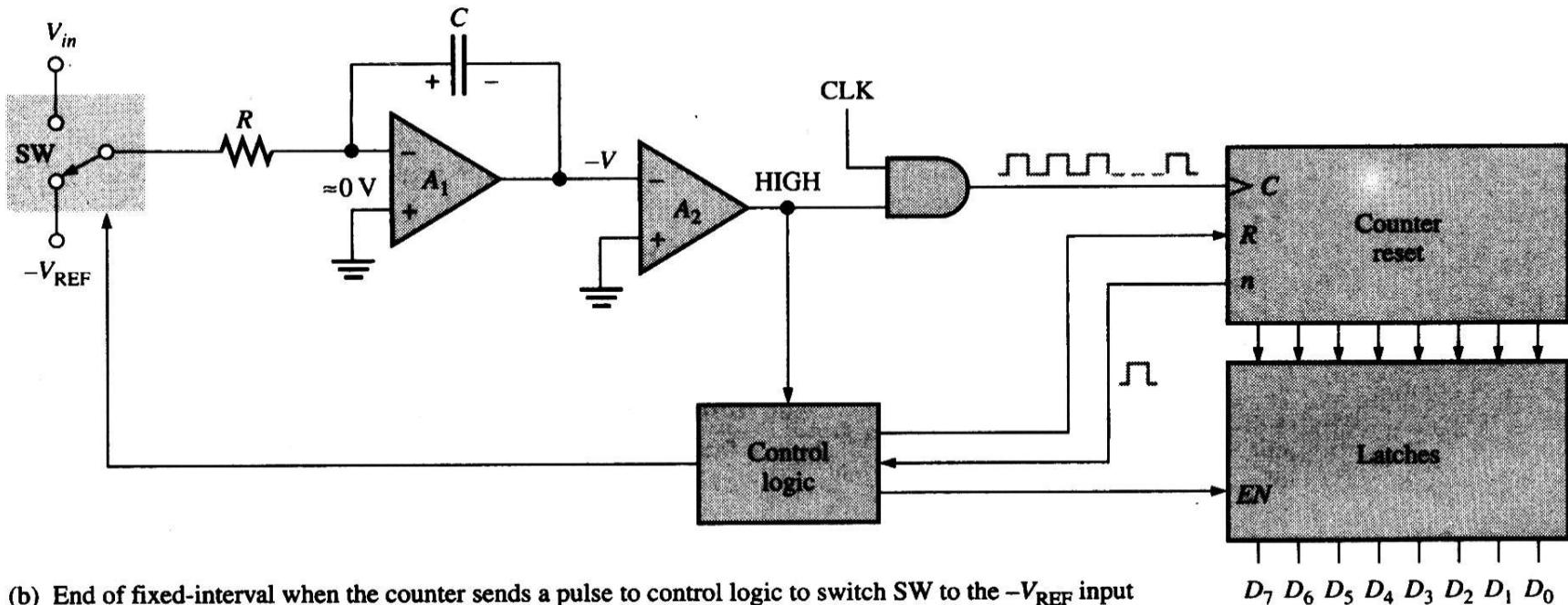


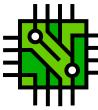


# Dual-Slope ADC

- When the counter reaches a specified count, it will be reset, and the control logic will switch the negative reference voltage to the input of the integrator.
- At this point the capacitor is charged to a negative voltage proportional to the input analog voltage.

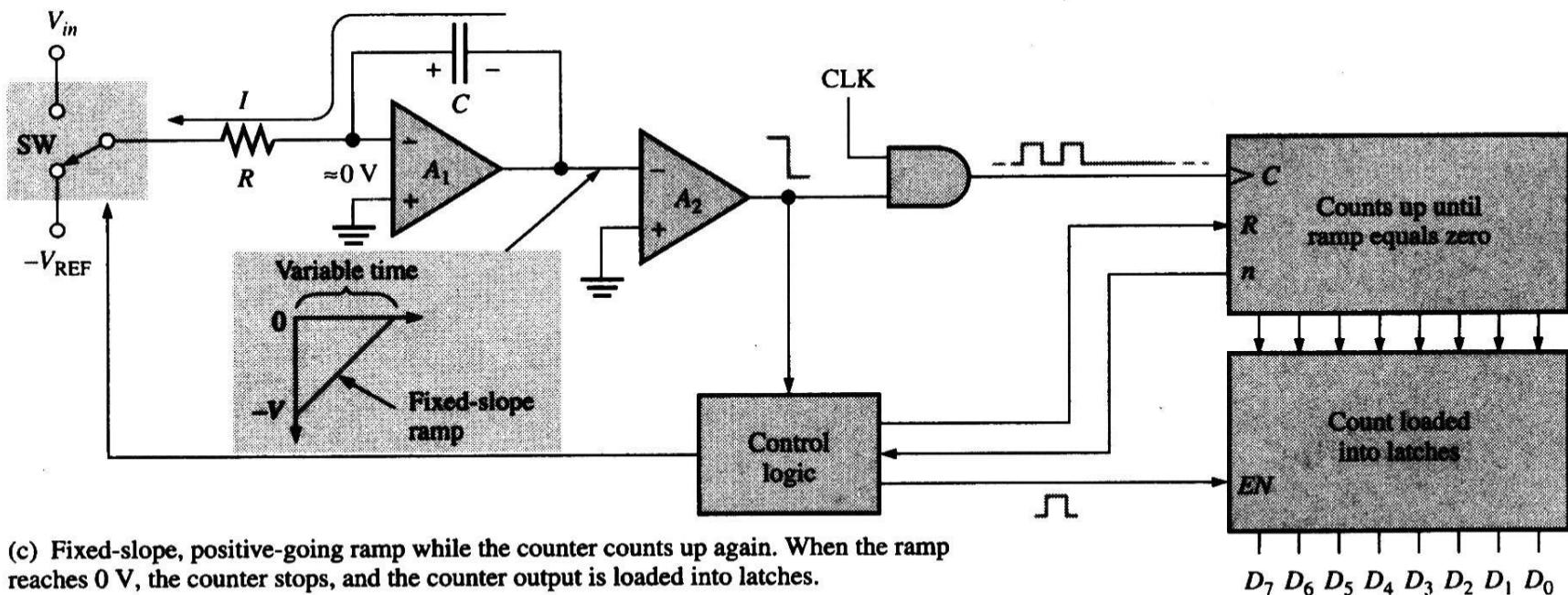
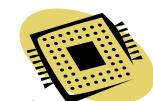
QUESTION





## Dual-Slope ADC

- Now the capacitor discharges with a constant rate. When the integrator output voltage reaches zero, the comparator switches to the LOW state and disables the clock of the counter. The binary count is latched.



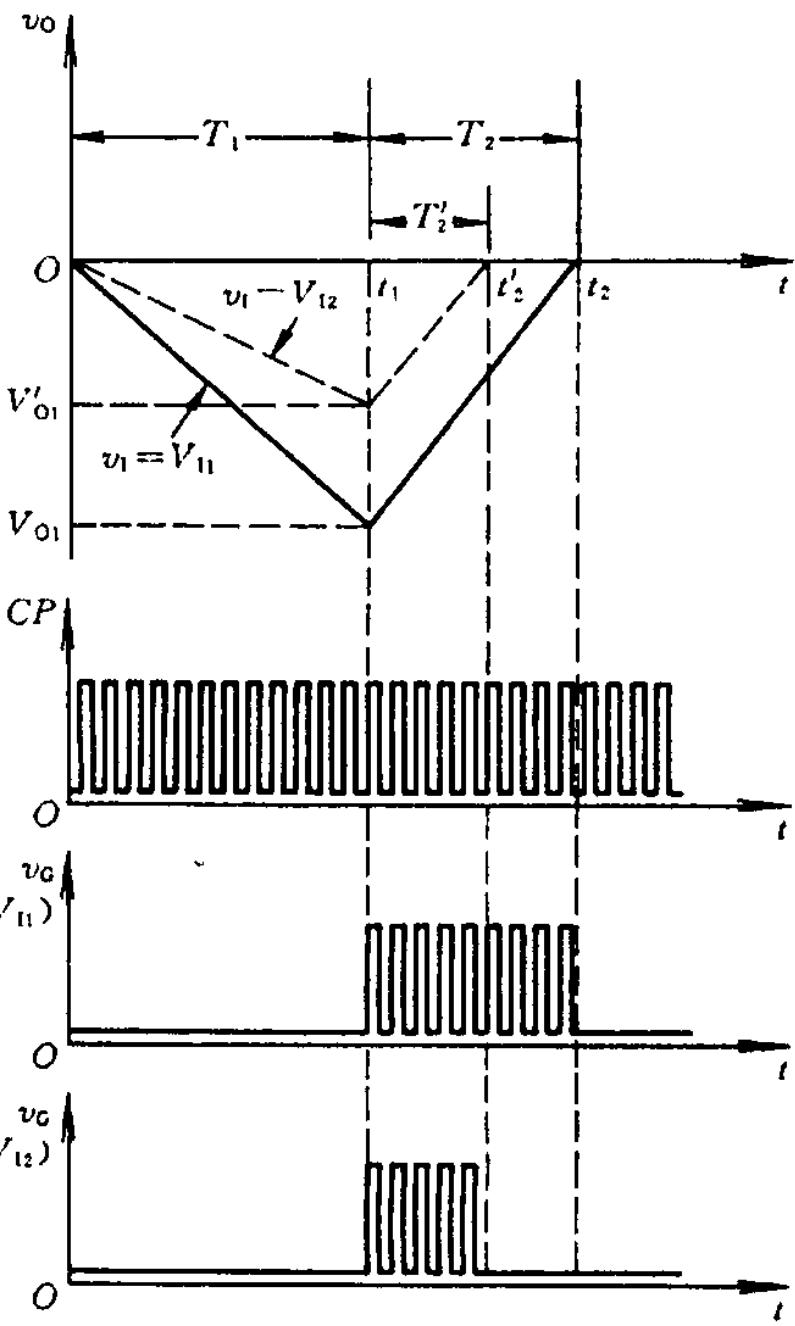
(c) Fixed-slope, positive-going ramp while the counter counts up again. When the ramp reaches 0 V, the counter stops, and the counter output is loaded into latches.

$D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0$

$$v_o = \frac{1}{C} \int_0^{T_2} \frac{V_{\text{REF}}}{R} dt - \frac{T_1}{RC} v_i = 0$$

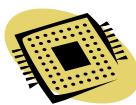
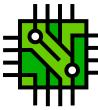
$$\frac{T_2}{RC} V_{\text{REF}} = \frac{T_1}{RC} v_i$$

$$T_2 = \frac{T_1}{V_{\text{REF}}} v_i$$



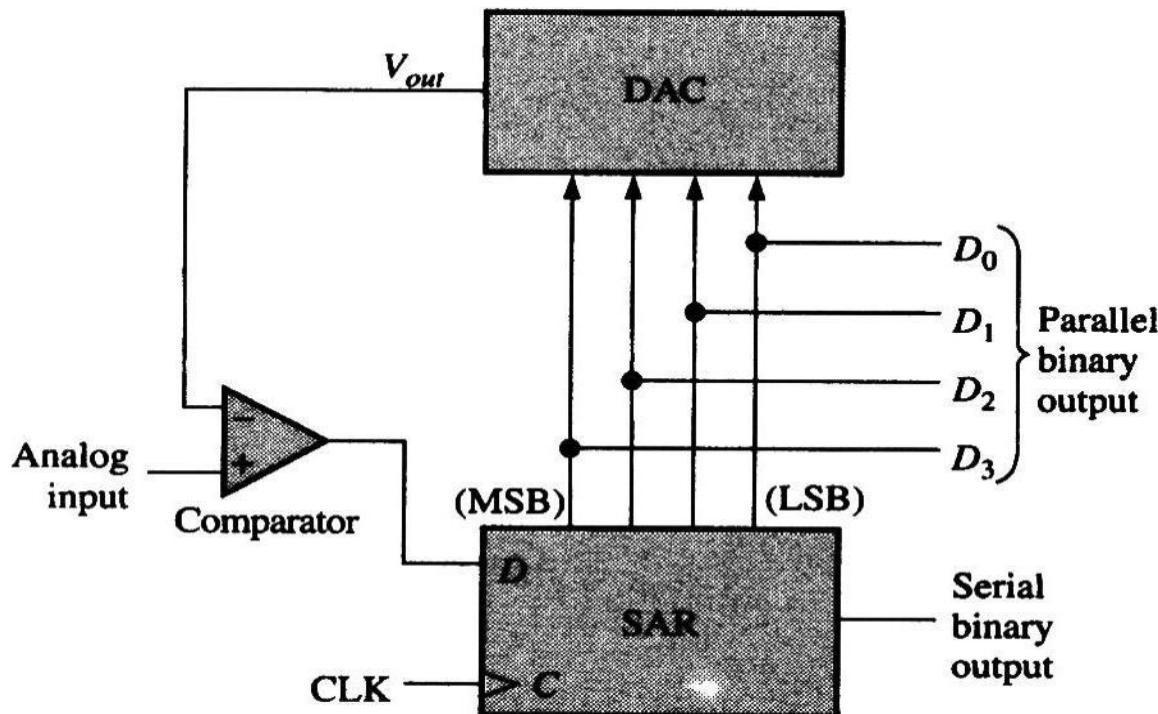
2018/12/6

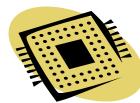
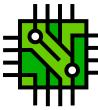
By Bao Qilian



# Successive-Approximation ADC (逐次比较型ADC)

- Perhaps the most widely used method of ADC is successive-approximation. It has a much faster conversion time than the other methods with the exception of the flash method. It also has a fixed conversion time that is the same for any value of the analog input.

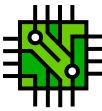




# Successive-Approximation ADC

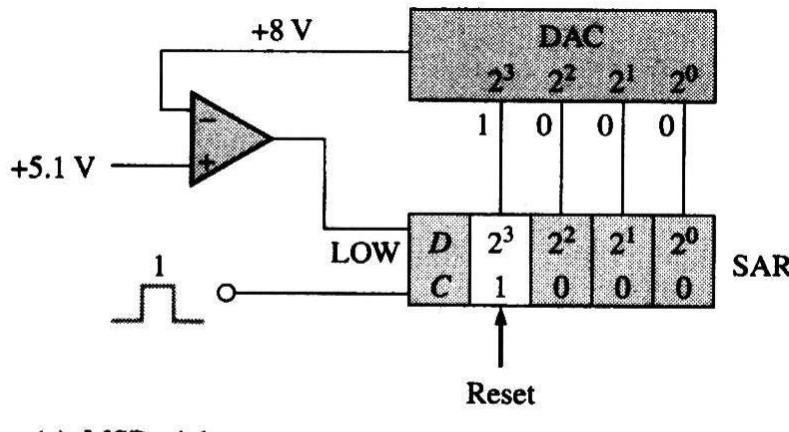
## (逐次比较型ADC)

- The basic operation is as follows:
  - The input bits of the DAC are enabled (made equal to 1) one at a time, starting with the MSB.
  - As each bit is enabled, the comparator produces an output that indicates whether the analog input voltage is greater or less than the output of the DAC.
    - If the DAC output is greater than the analog input, the comparator's output is LOW, causing the bit in the register to reset.
    - If the output is less than the analog input, the 1 bit is retained in the register.
  - The system does this with the MSB first, then the next most significant bit, then the next, and so on.
  - After all bits of the DAC have been tried, the conversion cycle is complete.

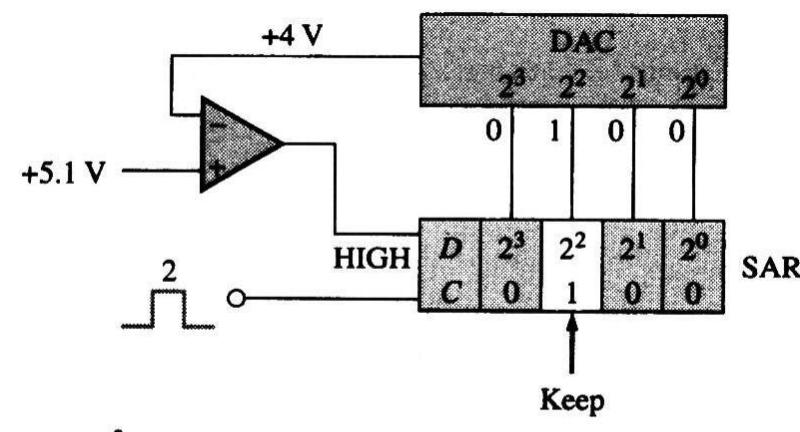


# Successive-Approximation ADC

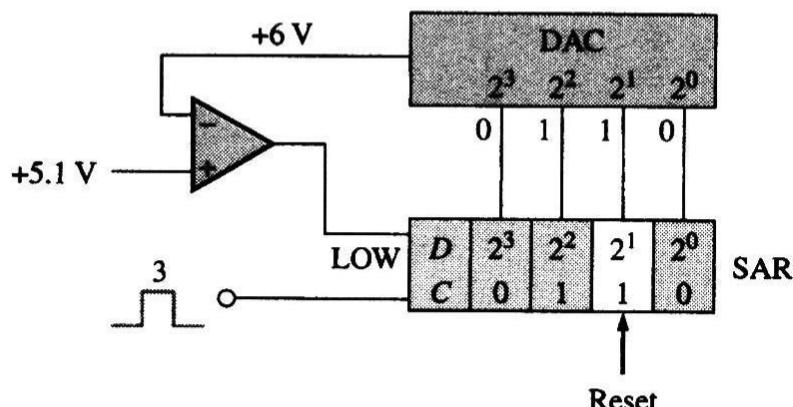
- Assume the analog input voltage is 5.1 volts and the 4-bit DAC has a quantization spacing  $Q = 1$  volt.



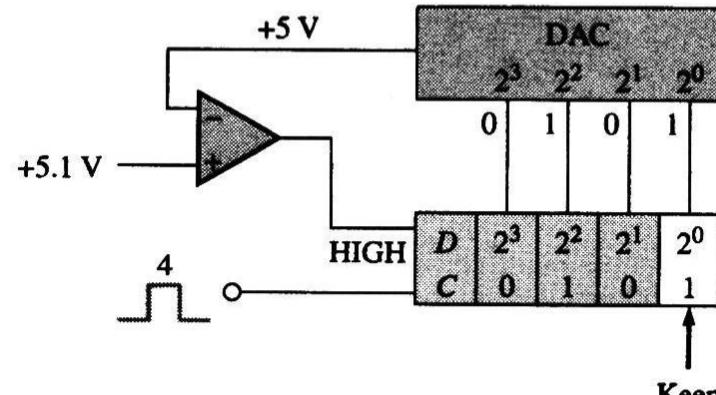
(a) MSB trial



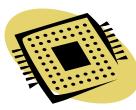
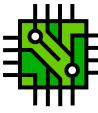
(b)  $2^2$ -bit trial



(c)  $2^1$ -bit trial

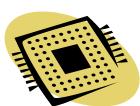
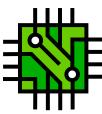


(d) LSB trial (conversion complete)

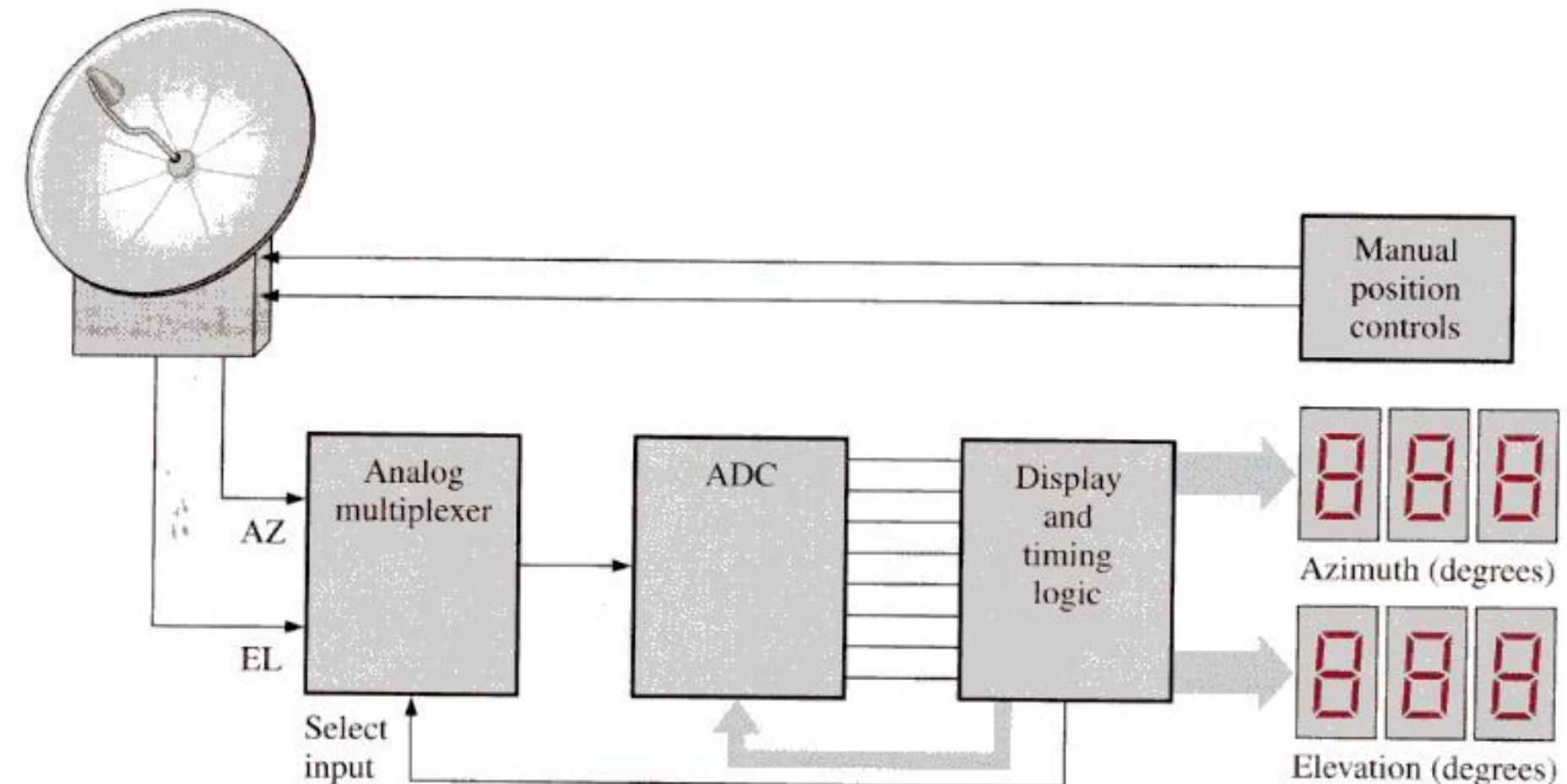


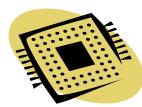
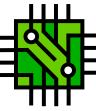
# Characteristics

- Resolution:
  - Number of output bits :  $n$
  - $\frac{1}{2^n} FSR$
- Accuracy
  - $\pm 1/2$ LSB of output
  - A percentage of FS input
- Speed
  - Flash ADC: <50ns
  - 10~100 $\mu$ s



# Application

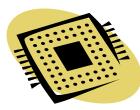
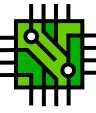




# Summary

## DAC

- Binary-weighted-input DAC
- R/2R ladder DAC
- ADC
  - Sampling and quantization
  - Flash ADC
  - Stairstep-ramp ADC
  - Tracking ADC
  - comparison



- chapter12: 6, 8, 10, 12, 14, 22, 23