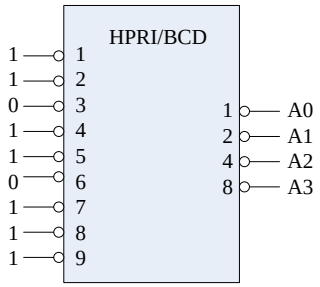
Self-Test

True/False

1. A periodic waveform has a time period of 25ms and a pulse width of 5ms. The duty cycle is 20%.
2. Repeated division-by-10 is used to convert decimal numbers to binary numbers.
3. $(11101000)_2$ is the 2's complement representation of -24.
4. The inputs to an AND gate are: A=1, B=0, C=1. The output will be LOW.
5. Full-adders can add two numbers and need not have a carry input or a carry output.
6. The look-ahead-carry adder is slower than the ripple-carry adder, since it requires additional logic circuits.
7. Full-adders can be used as a BCD-to-binary converter.
8. A multiplexer has multiple inputs and a single output.
9. Parity generators/checkers are useful because they do not require any additional data lines to function.
10. The commutative law of Boolean addition states that A+B=A B

Multiple Choice（单选题）

1. Pulse width is defined as the_____
   a. time that the pulse remains at the HIGH level.
   b. time differential between the rising and falling edges.
   c. length of the pulse measured at the LOW level.
   d. duration of the pulse at the 50% level.
2. A negative-AND gate is functionally equivalent to a/an _____
   a. AND gate with active-LOW inputs
   b. NOR gate with active-LOW inputs
   c. OR gate with active-LOW inputs
   d. NOT gate with active-HIGH inputs
3. Which type of gate can be used to add two bits?
   a. NAND b. NOR c. XOR d. XNAND
4. What is one disadvantage of the ripple-carry adder?
   a. The interconnections are more complex.
   b. More stages are required to a full-adder.
   c. It is slow, due to propagation time.
   d. All of the above are correct.
5. The following figure shows a _____ and for the inputs shown, the outputs(A3,A2,A1,A0) will be_____.



   a. BCD-to-decimal decoder,1001
   b. decimal-to-BCD priority encoder 0110
   c. BCD-to-decimal decoder,0110
   d. decimal-to-BCD encoder,1001
6. What is the decimal number for the BCD number, 10110110?
   a. 182
   b. 36
   c. 116
   d. Not a valid BCD number

7. Which of the following is not an important feature of the sum of products form of expressions?
   a. All logic circuits are reduced to nothing more than simple AND and OR gates.
   b. The delay times are greatly reduced over other forms.
   c. No signal must pass through more than 2 gates, not including inverters.
   d. The maximum number of gates that any signal must pass through is reduced by a factor of two.
8. A Karnaugh map will_____.
   a. eliminate the need for tedious Boolean simplifications.
   b. allow any circuit to be implemented with just AND and OR gates.
   c. produce the simplest sum of products expression.
   d. give an overall picture of how the signals flow through the logic circuit.

Problems

1. Design a decoding circuit with three input lines, when inputs *ABC*=001，011，101，111, the output is 1。

2. Try to implement the following logic function with a 4-16 decoder 74HC154 and logic gates。

$$F_1(A,B,C,D) = \sum m(0,2,4,10,11,12,13)$$

3. Please try to implement the following logic function with a 74HC151 and 74HC150：

$$\boldsymbol{F(A,B,C,D) = AB + CD}$$