电子技术
Introduction to Electronics

By Bao Qilian
鲍其莲
Digital_ie@163.com
201720170

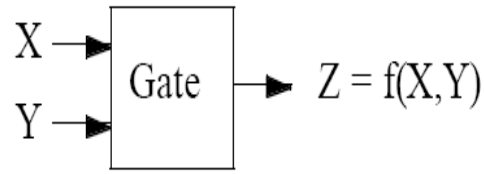
2018/9/13 1

Chapter 3 Logic Gates

- *Objectives:*
  - Basic gates: NOT,AND, OR
  - Extend gates: NAND,NOR, Exclusive-OR, Exclusive-NOR
  - Symbols
- *Reading assignment*
  - Chapter3 p98-p138

3.1 Gate

- Gate（门电路）: A simple electronic circuit (a system) that realizes a logical operation.
  - The direction of information flow is from the input terminals to the output terminal.
  - The number of input and output terminals is finite and they carry binary-valued signals.
  - The transformation of input signals to output signals can be modeled as a logical

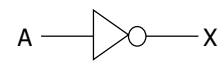


The Inverter Gate

The inverter (NOT：非门) performs the operation called inversion or complementation. The inverter changes one logic level to the opposite level. In terms of bits, it changes a 1 to 0, and a 0 to 1.

The INVERTER (NOT)Gate

•*Symbol*

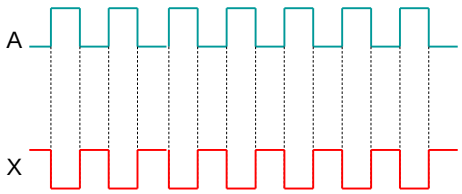


•*Logic expression* $X = \overline{A}$

•*Truth table*

Input A	Output X
0	1
1	0

•*IO-Waveform*



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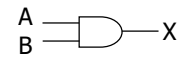
The AND Gate（与门）

•*Symbol*



•*Logic expression* $X = AB$

•*Truth table*

Inputs		Output
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

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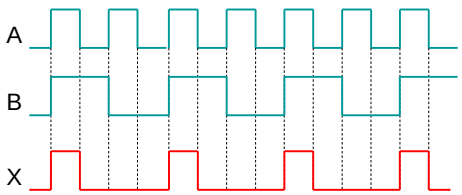
•*IO-Waveform*



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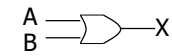
The OR Gate（或门）

•*Symbol*



•*Logic expression* $X = A + B$

•*Truth table*

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

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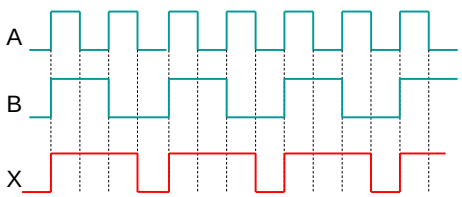
•*IO-Waveform*



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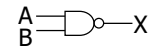
The NAND Gate（与非门）

•*Symbol*



•*Logic expression* $X = \overline{AB}$

•*Truth table*

Inputs		Output
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

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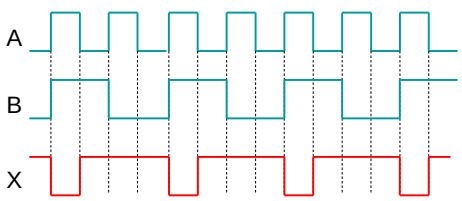
•*IO-Waveform*



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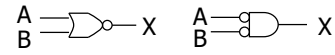
The NOR Gate（或非门）

•*Symbol*



Negative-AND gate

•*Logic expression*

$$X = \overline{A + B}$$

•*Truth table*

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

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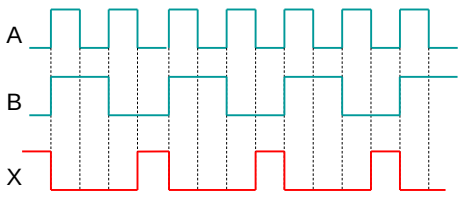
•*IO-Waveform*



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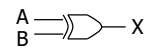
The Exclusive-OR(XOR) Gate（异或门）

•*Symbol*



•*Logic expression*

$$X = A \oplus B = A\overline{B} + \overline{A}B$$

•*Truth table*

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

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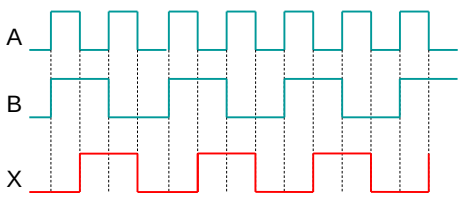
•*IO-Waveform*



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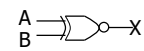
The Exclusive-NOR(XNOR) Gate（同或门）

•*Symbol*



•*Logic expression*

$$X = \overline{A \oplus B} = AB + \overline{A}\overline{B}$$

•*Truth table*

Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

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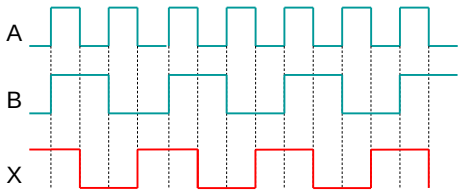
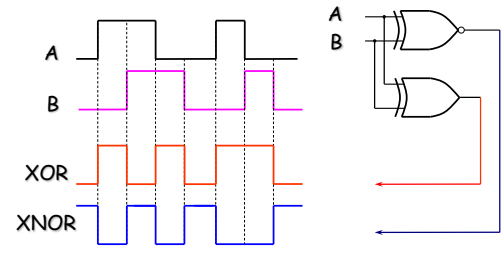
·IO-Waveform

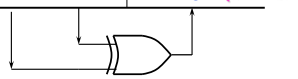


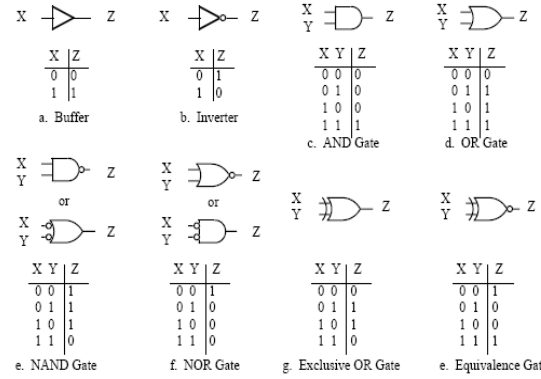
Example1: Determine the output waveform for the XOR gate and for the XNOR gate, given the input waveforms of A and B as follows:



Example2: The XOR gate used to add two bits.

Input bits		Output(sum)
A	B	∑
0	0	0
0	1	1
1	0	1
1	1	0 (without 1 carry)

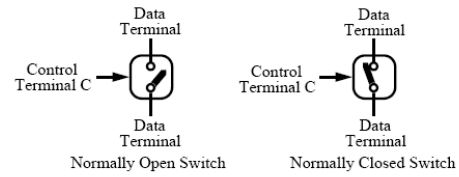




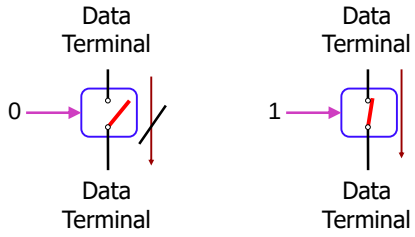
3.2 Gate Implementations

This section presents a very simple structural model of gates based on an idealized device called a Logic Switch.

- Definition: A Logic Switch is a three-terminal device that is used to control the connection of two points in a circuit.



Logic Switch



Switch States:

- Closed: Switch conducts between its data terminals.
- Open: No conduction between the data terminals.
- When C=0, the switch is in its normal state.
- When C=1, the switch is in its active or on state.
- When C=1, the arm is pulled towards the C input.

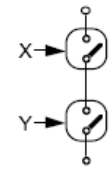
Ideal Switch Assumption:

- 0 resistance when closed, ∞ resistance when open.
- 0 delay switching between open and closed.

Real electronic switches are implemented with transistors, and they fail to meet the ideal switch assumptions in that:

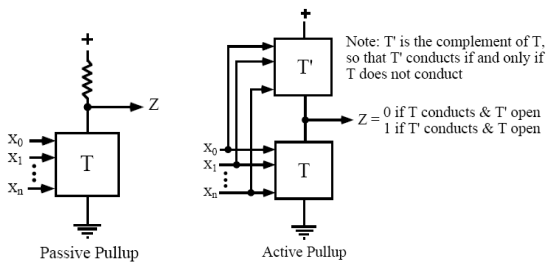
- Resistance in open state is high, but not infinite.
- Resistance in closed state is low, but not zero.
- Time required to change states is greater than zero.

Example: The following switch network conducts between its two terminals just in case both the signals X and Y are 1.

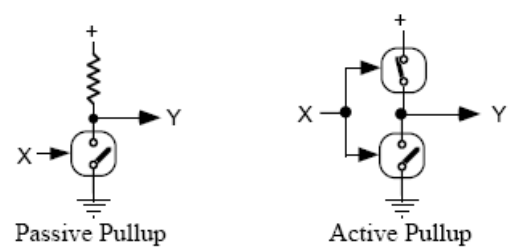


General Model

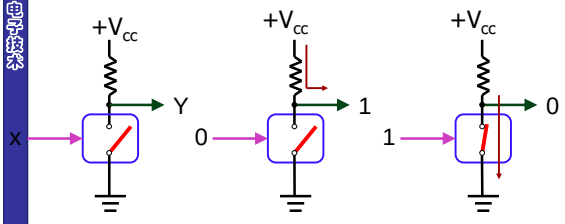
Passive pullup **Active pullup**



Inverters



Inverters (Passive pullup)



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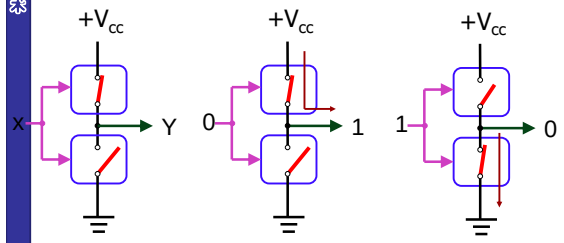
Inverters (Active pullup)



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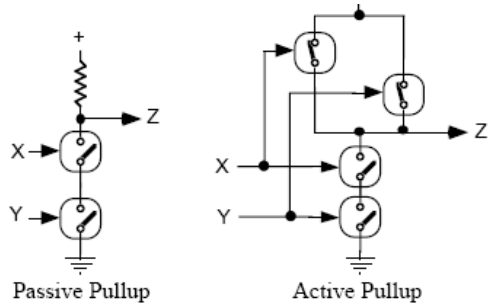
NAND Gates



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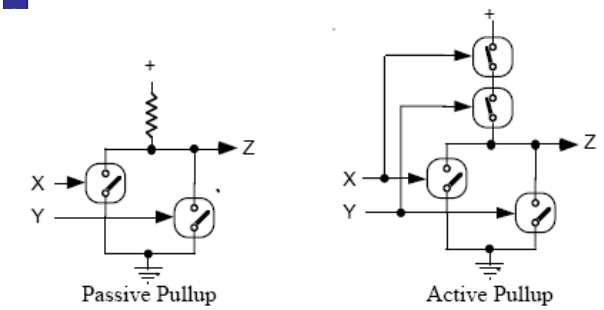
NOR Gates



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3.3 Integrated Circuit Technology

Objectives

- Basic characteristics
- TTL gate
  - Inverter
  - NAND
- CMOS gate
  - Inverter
  - NAND

Reading Assignment

P790-820

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Integrated Circuit technologies

IC technologies:

1.bipolar(TTL,LTTL,STTL,LSTTL,ECL ...)

2.MOS(PMOS,NMOS,CMOS,BiCMOS...)

Main IC logic families: TTL,ECL, CMOS

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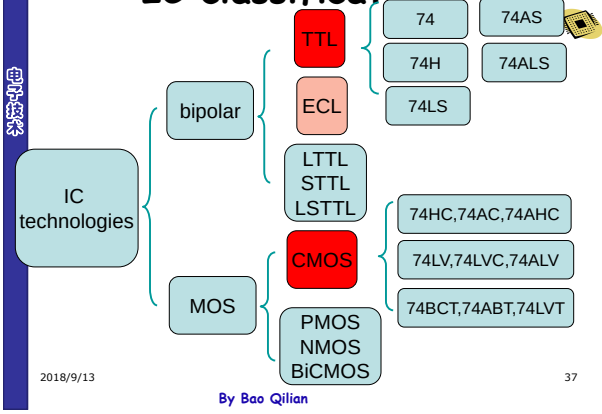
IC classification



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CMOS series

- The basic CMOS series for the 5 V category and their designations are as follows:
  - 74HC and 74HCT: High-speed CMOS
  - 74AC and 74 ACT: Advanced CMOS
  - 74AHC and 74AHCT: Advanced High-speed CMOS
- The basic CMOS series for the 5 V category and their designations are as follows:
  - 74LV: Low-voltage CMOS
  - 74LVC: Low-voltage CMOS
  - 74ALVC: Advanced Low-voltage CMOS
- In addition to the "pure" CMOS, there is a series that combines both CMOS and TTL called BiCMOS. The basic BiCMOS series and their designations are as follows:
  - 74BCT: BiCMOS
  - 74ABT: Advanced BiCOMS
  - 74LVT: Low-voltage BiCMOS
  - 74ALB: Advanced Low-voltage BiCMOS

TTL series

- The basic TTL series and their designations are as follows:
  - 74: standard TTL
  - 74S: Schottky TTL
  - 74AS: Advanced Schottky TTL
  - 74LS: Low-power Schottky TTL
  - 74ALS: Advanced Low-power Schottky TTL
  - 74F: Fast TTL

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1 Basic characteristics

- DC Supply Voltage
- Input and Output Logic level
- Noise Immunity
- Noise Margins

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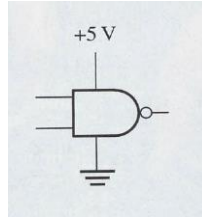
DC Supply Voltage

- *TTL* :
  - 5V
- *CMOS*:
  - 5V
  - 3.3V



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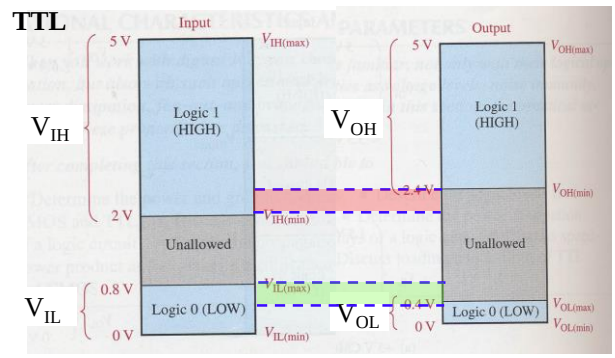
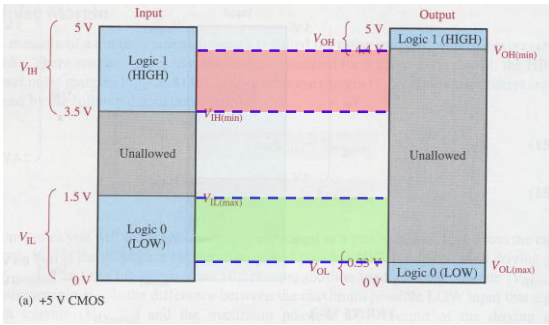
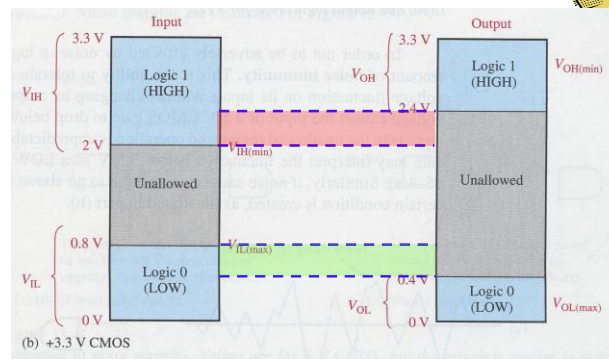
Input and Output Logic level



CMOS:5V



CMOS:3.3V



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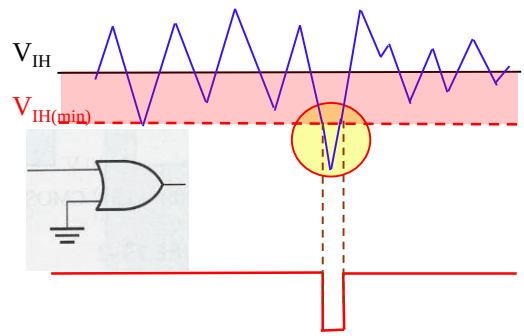
Noise Immunity

***Noise Immunity*: ability to tolerate a certain amount of unwanted voltage noise on its inputs without changing its output state.**



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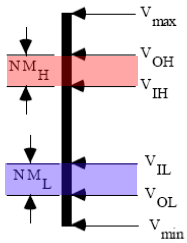
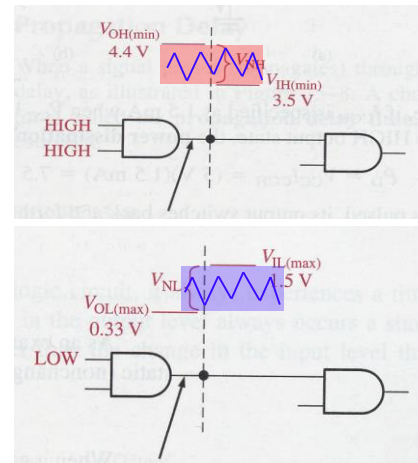
Noise Margins(噪声容限)



$V_{NH}=V_{OH(min)}-V_{IH(min)}$

$V_{NL}=V_{OL(max)}-V_{IL(max)}$

Example



Exercise

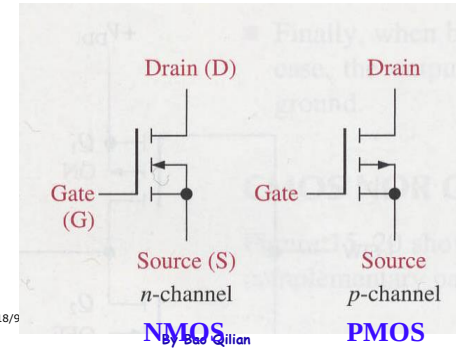
Assuming:

a) $V_{IH(min)}$=2.0V, $V_{IL(max)}$=0.8V, $V_{OH(min)}$=2.4V, $V_{OL(max)}$=0.4V ⇨ 3.3V CMOS TTL

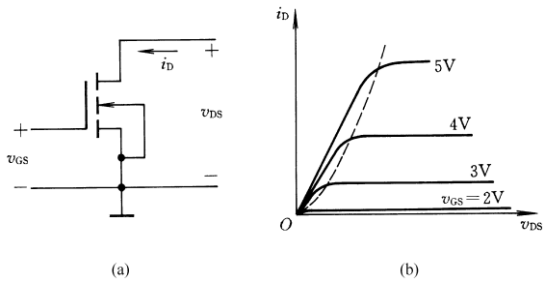
b) $V_{IH(min)}$=3.5V, $V_{IL(max)}$=1.5V, $V_{OH(min)}$=4.4V, $V_{OL(max)}$=0.33V ⇨ 5V CMOS

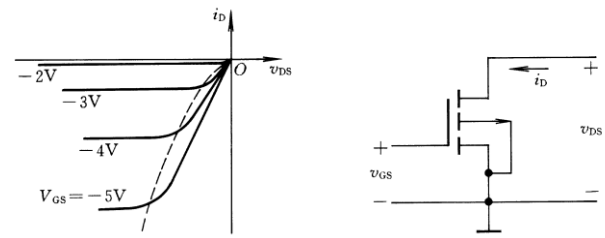
Determine the HIGH-level and LOW-level noise margins.

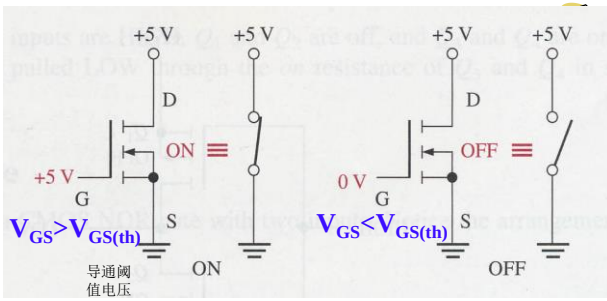
2 CMOS circuits

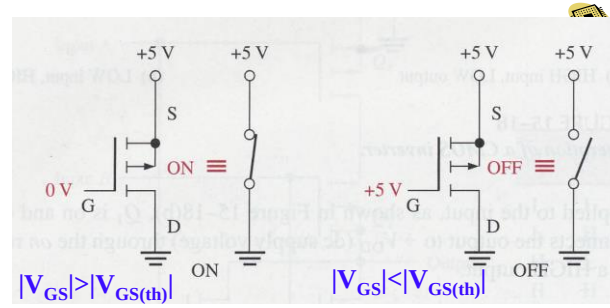


NMOS PMOS

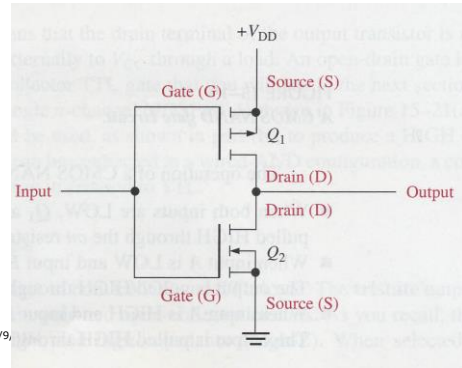


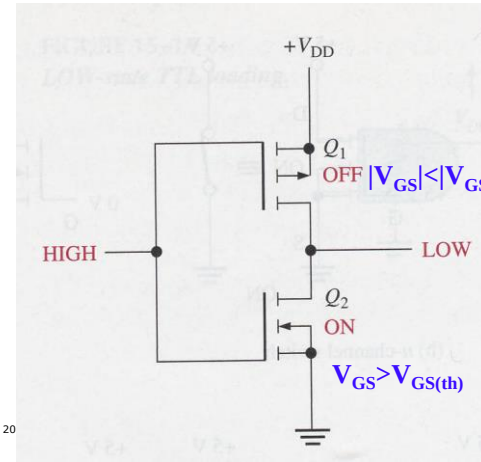


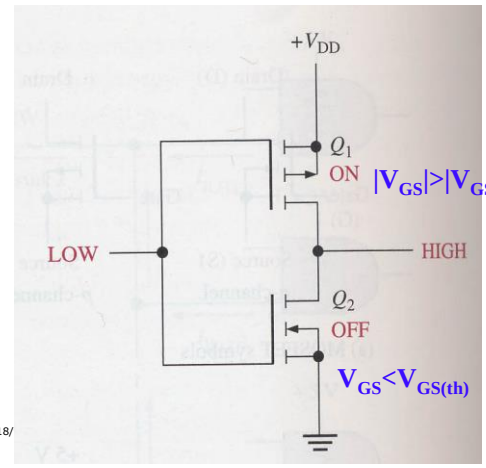




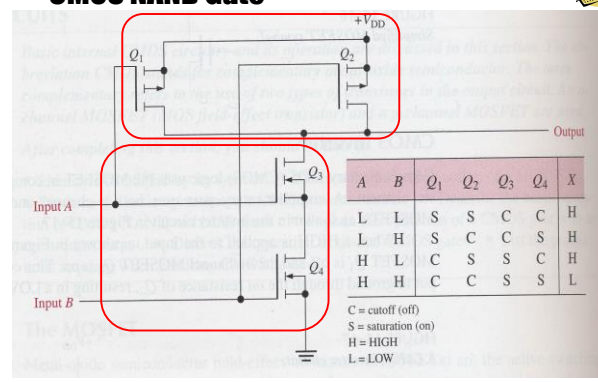
CMOS Inverter







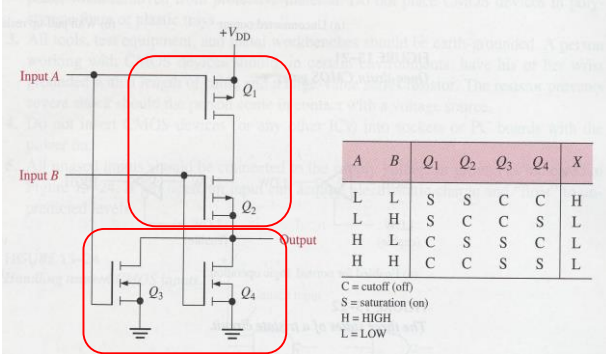
CMOS NAND Gate



A	B	Q_1	Q_2	Q_3	Q_4	X
L	L	S	S	C	C	H
L	H	S	C	C	S	H
H	L	C	S	S	C	H
H	H	C	C	S	S	L

C = cutoff (off)
S = saturation (on)
H = HIGH
L = LOW

CMOS NOR Gate



A	B	Q_1	Q_2	Q_3	Q_4	X
L	L	S	S	C	C	H
L	H	S	C	C	S	L
H	L	C	S	S	C	L
H	H	C	C	S	S	L

C = cutoff (off)
S = saturation (on)
H = HIGH
L = LOW

Summary

- Basic gates: NOT,AND, OR
- Extend gates: NAND,NOR, Exclusive-OR, Exclusive-NOR
- Symbols
- Implement of gates
- IC classification by technologies
- TTL , CMOS

By Bao Qilian

电子技术

Homework 3
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Problems:

2, 7, 9, 17, 20, 24