

Chapter 8 Counters

Objectives

- Asynchronous counter Operation
- Synchronous counter Operation
- Up/Down Asynchronous counter Operation
- Design of Synchronous Counters
- Analysis and Design of Sequence Circuit

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电子技术

- Cascaded Counters
- Counter Decoding
- Counter Application

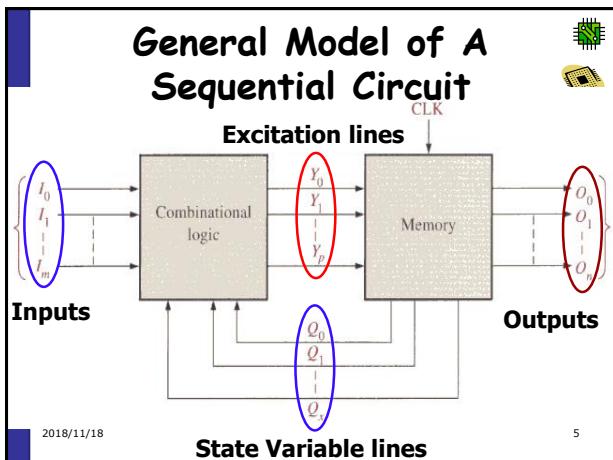
Reading assignments

- P454-P493

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- Combinational logic circuits(组合逻辑电路) : outputs are functions of inputs only.
- Sequential circuits (时序电路) : outputs depend on current states and/or inputs.
 - Mealy sequential circuits: output depend on both states and inputs
 - Moore sequential circuits: output depend on states only

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$$Y_0 = f_0(I_0, I_1, \dots, I_m, Q_0, Q_1, \dots, Q_x)$$

$$Y_1 = f_1(I_0, I_1, \dots, I_m, Q_0, Q_1, \dots, Q_x)$$

$$\vdots$$

$$Y_p = f_p(I_0, I_1, \dots, I_m, Q_0, Q_1, \dots, Q_x)$$

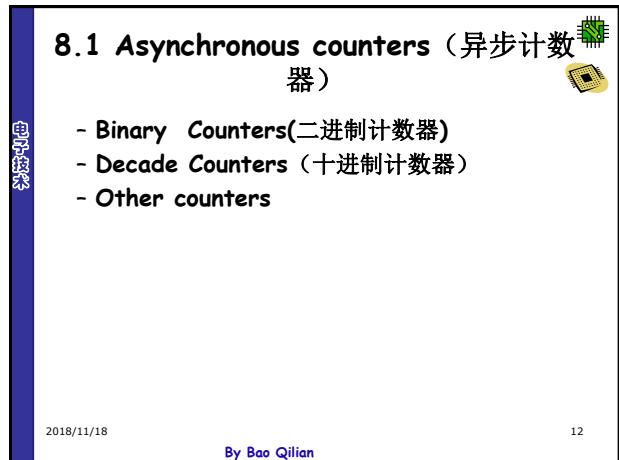
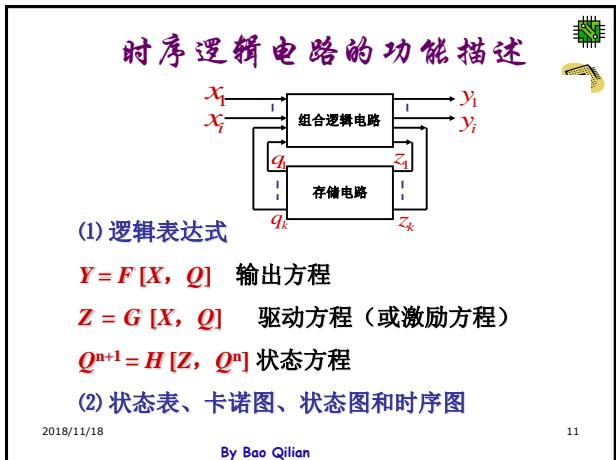
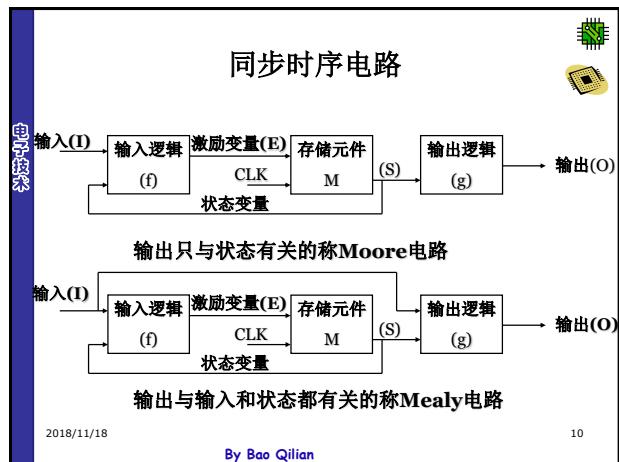
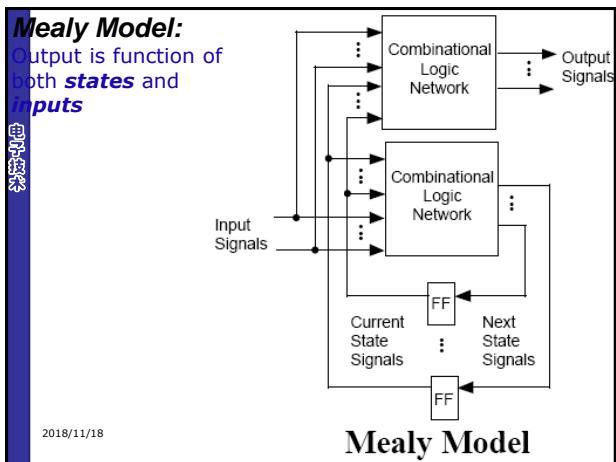
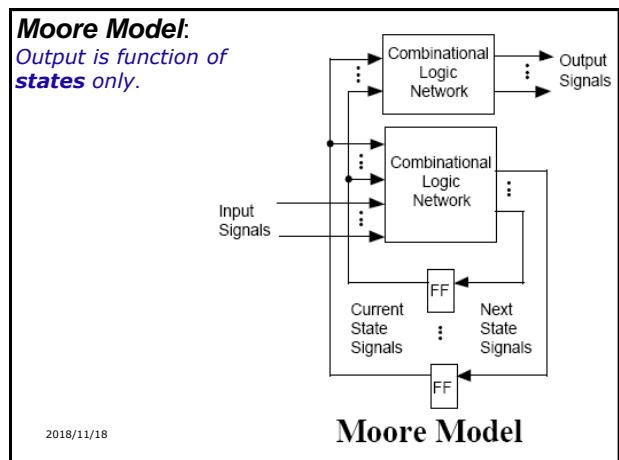
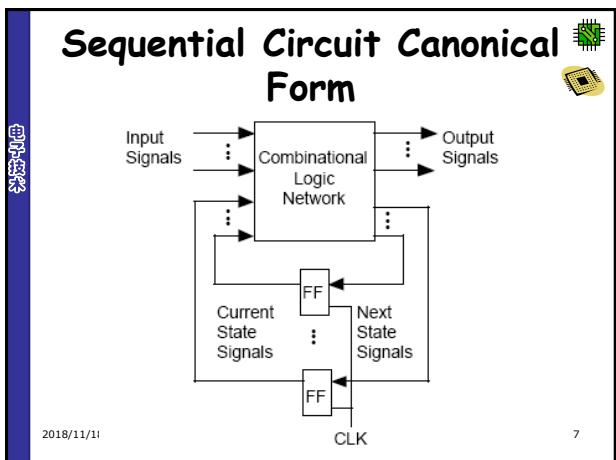
$$O_0 = g_0(Y_0, Y_1, \dots, Y_p)$$

$$O_1 = g_1(Y_0, Y_1, \dots, Y_p)$$

$$\vdots$$

$$O_n = g_n(Y_0, Y_1, \dots, Y_p)$$

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1 Binary Counters

- Counting in 2-modulus

电子学

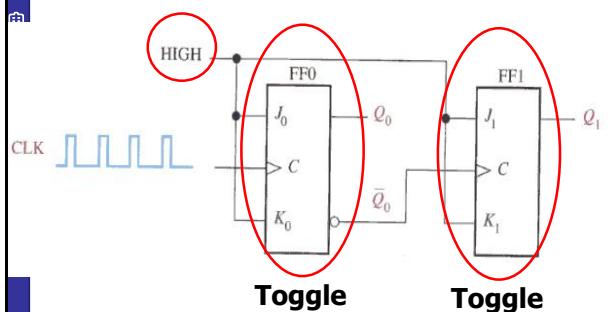
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2-bit Asynchronous Binary counter

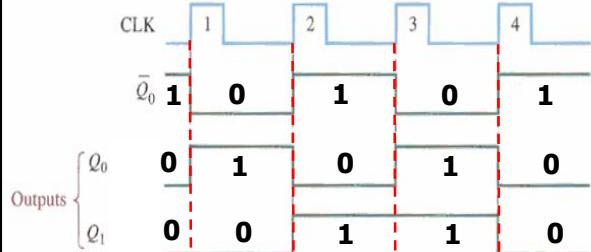


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Timing Diagram



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Binary state sequence

Clock Pulse	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycles)	0	0

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MSB
LSB

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Exercise: Design a 3-bit Asynchronous Binary counter by J-K FFs

电子学

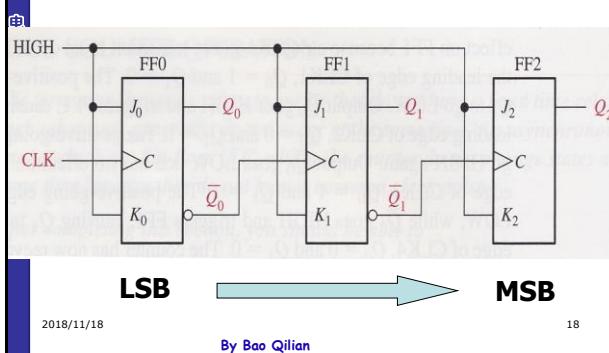
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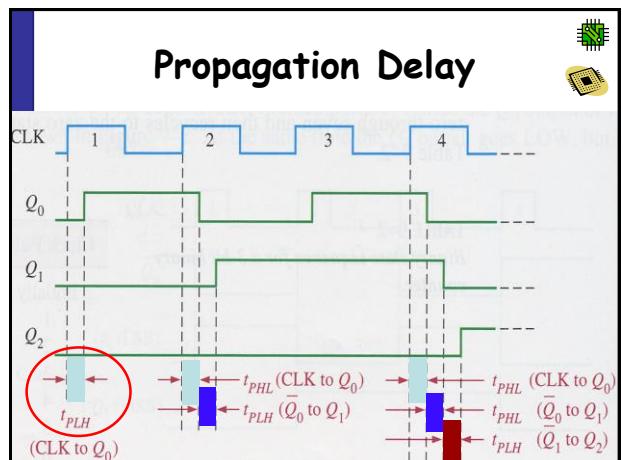
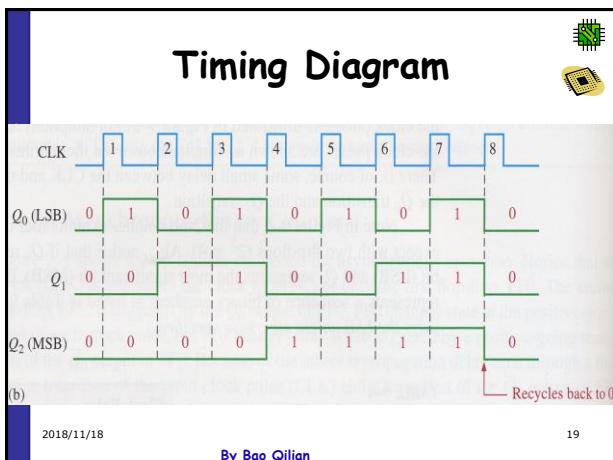
3-bit Asynchronous Binary counter



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Exercise:

For a 3-bit asynchronous counter, If the edge triggered J-K FFs has a propagation delay of 10ns, determine the maximum clock frequency at which the counter can be operated.

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Solution:

1. The propagation delay time for 3 FFs:
 $t_p = 3 \times 10 = 30\text{ns}$
 $T_{min} = t_p$
2. The maximum frequency for Clock:
 $f_{max} = 1/T_{min} = 1/30\text{ns} = 33.3\text{MHz}$

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Design of Asynchronous Binary Counters

- The number of bits of binary counters = the number of FFs
- The propagation delay time limits the operation frequency

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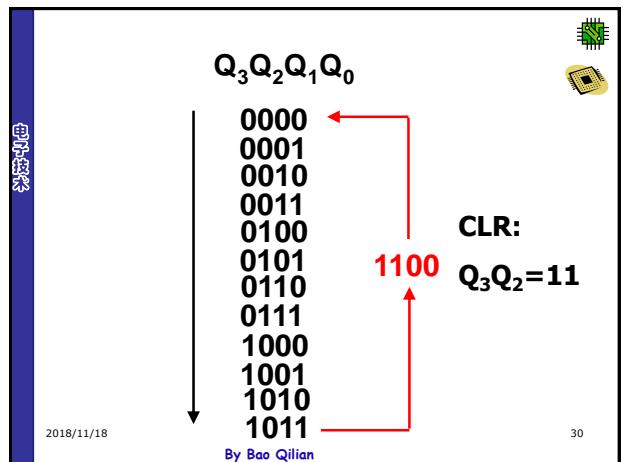
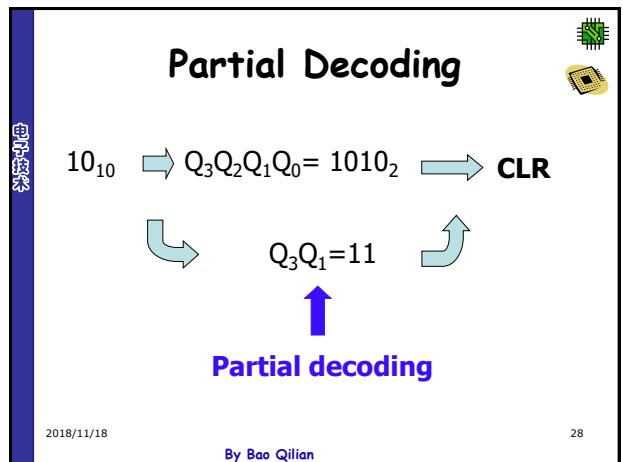
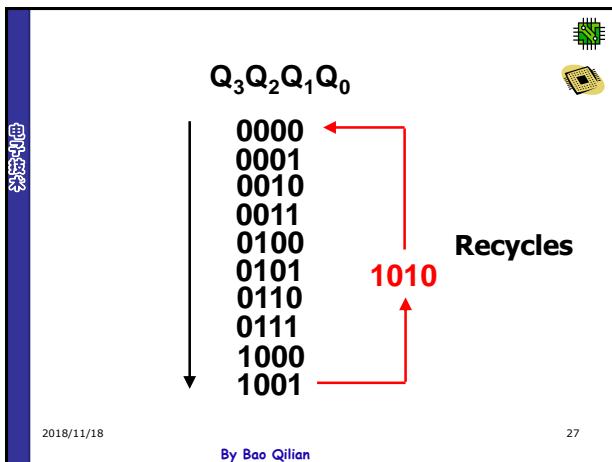
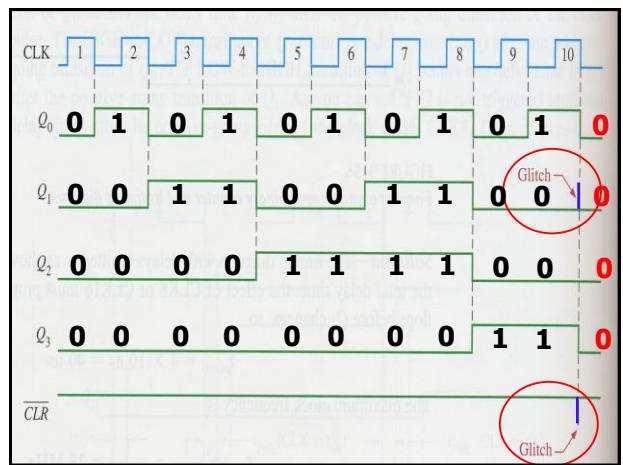
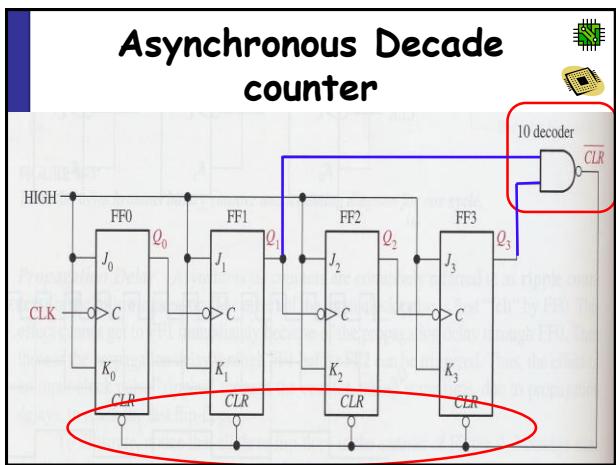
2 Asynchronous Decade counter

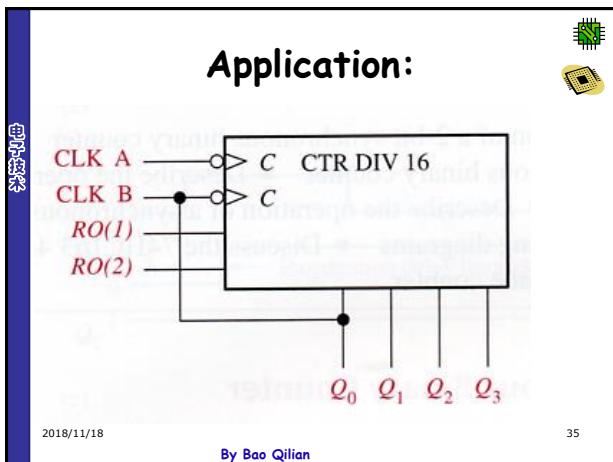
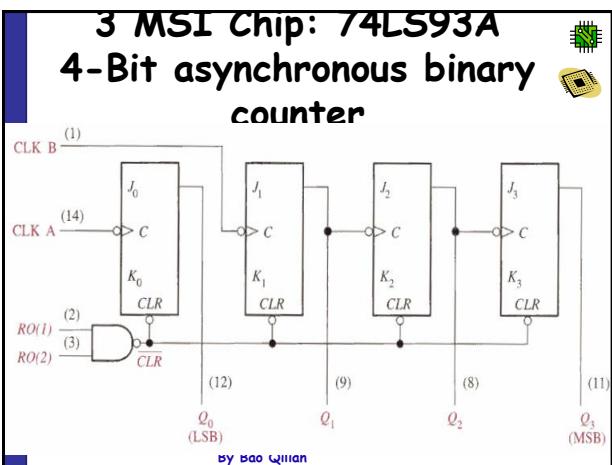
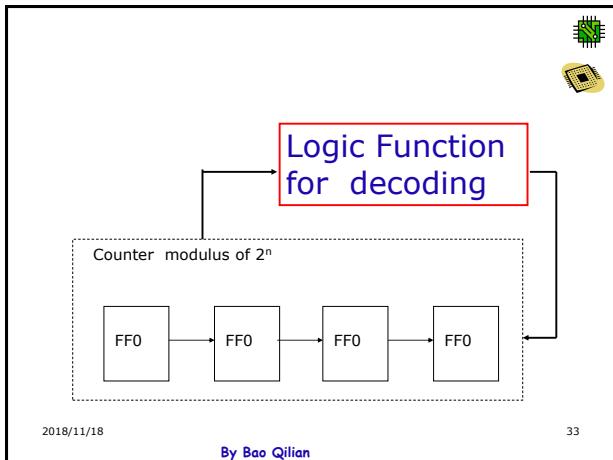
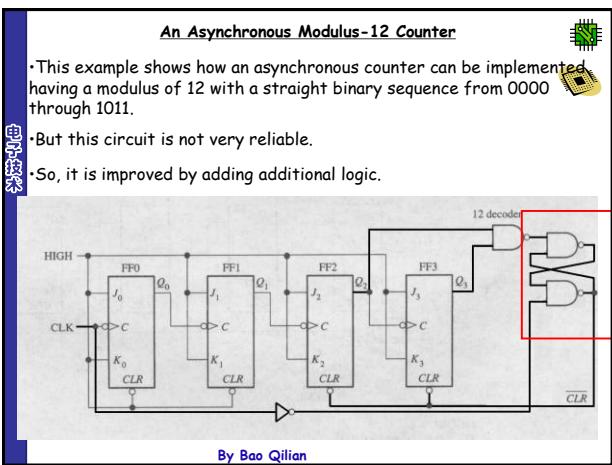
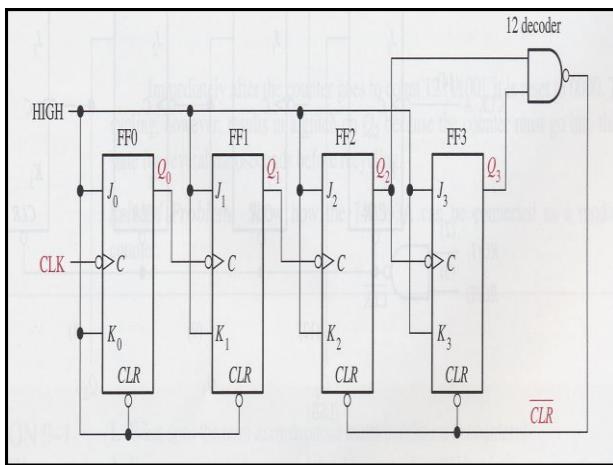
- The number of states = 2^n where n is the number of FFs
- Truncated sequence: the number of states is less than 2^n
- Using truncated sequence to design decade counters

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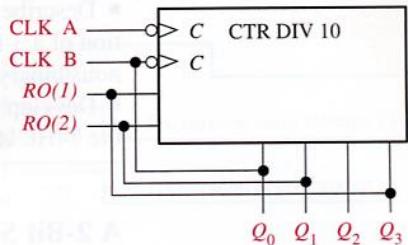
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Exercise: design a decade counter using 74LS93A.

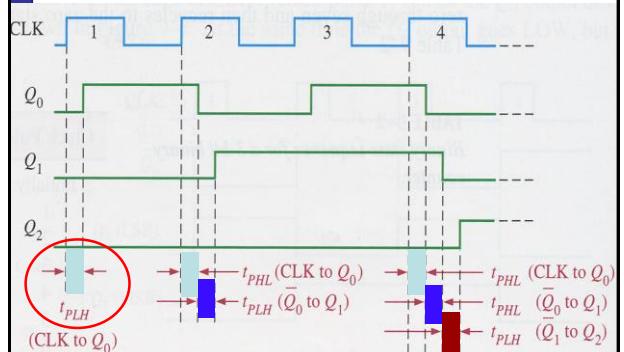


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Propagation Delay



8.2 Synchronous Counters

- Binary Counters
- Decade Counters
- Other Counters

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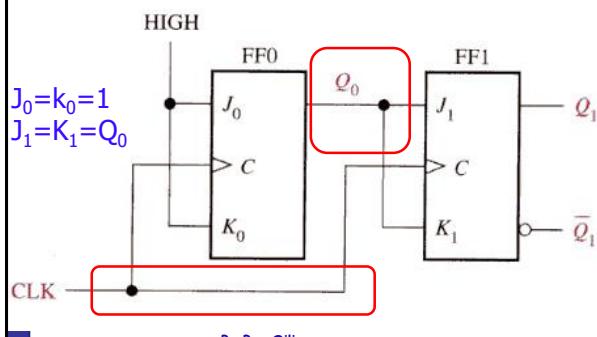
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1 Binary Counters

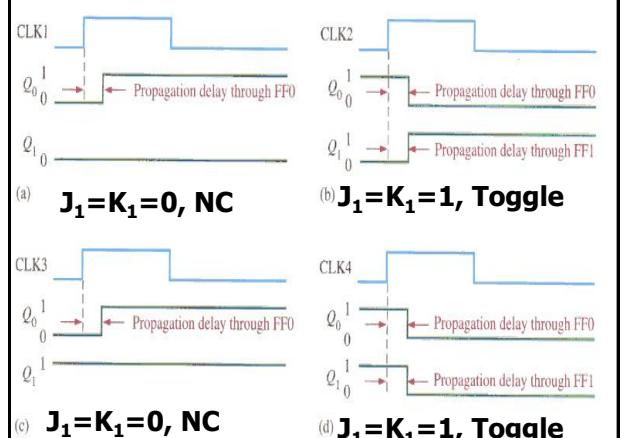
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2-Bit Synchronous Binary Counter

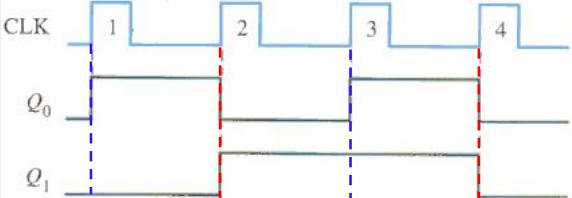


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Timing Diagram

00 \Rightarrow 01 \Rightarrow 10 \Rightarrow 11 \Rightarrow 00



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3-Bit Synchronous Binary Counter

Clock Pulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

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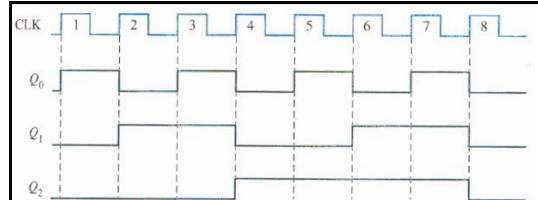
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3-Bit Synchronous Binary Counter

$$J_1 = K_1 = Q_0$$

$$J_2 = K_2 = Q_0Q_1$$

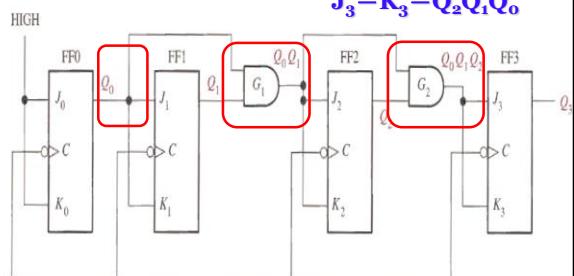


Clock Pulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

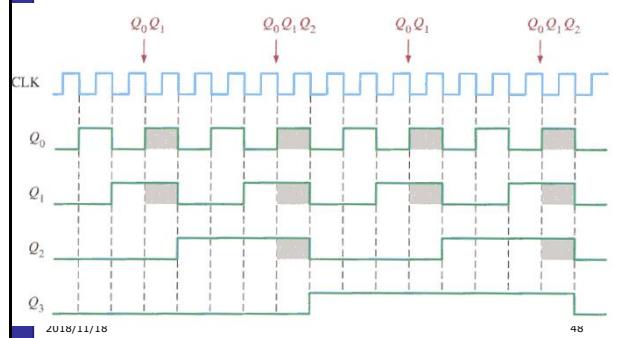
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4-bit Synchronous Binary Counter

$$\begin{aligned} J_0 &= K_0 = 1; \\ J_1 &= K_1 = Q_0; \\ J_2 &= K_2 = Q_0Q_1; \\ J_3 &= K_3 = Q_0Q_1Q_2 \end{aligned}$$



Timing Diagram



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Synchronous Decade Counter

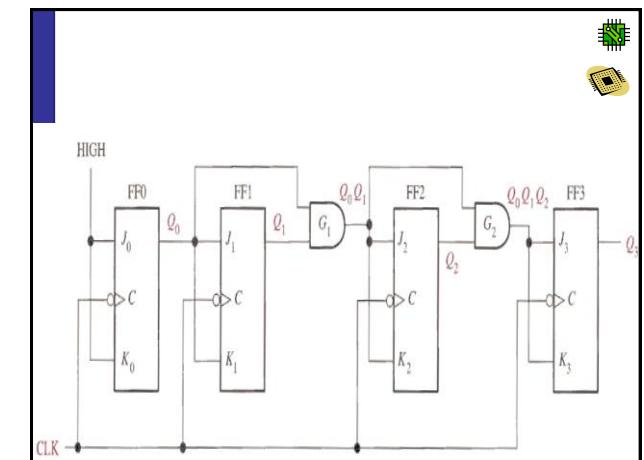
$Q_3 Q_2 Q_1 Q_0$

- 0000
 - 0001
 - 0010
 - 0011
 - 0100
 - 0101
 - 0110
 - 0111
 - 1000
 - 1001
- $Q_0 = \bar{Q}_0 \checkmark$
- $Q_1 = Q_1$
- $Q_2 = Q_2 \checkmark$
- $Q_3 = \bar{Q}_3$
- 1010

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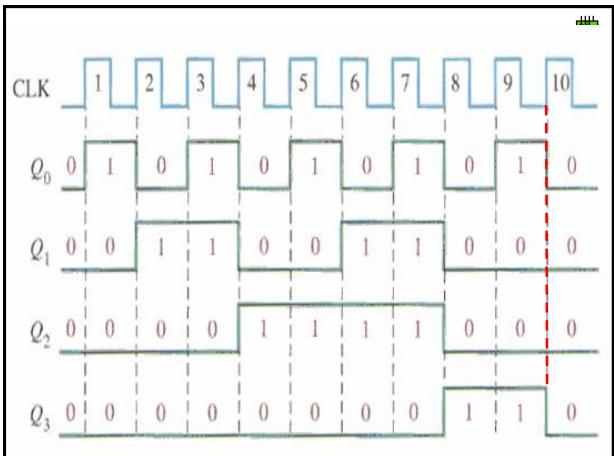
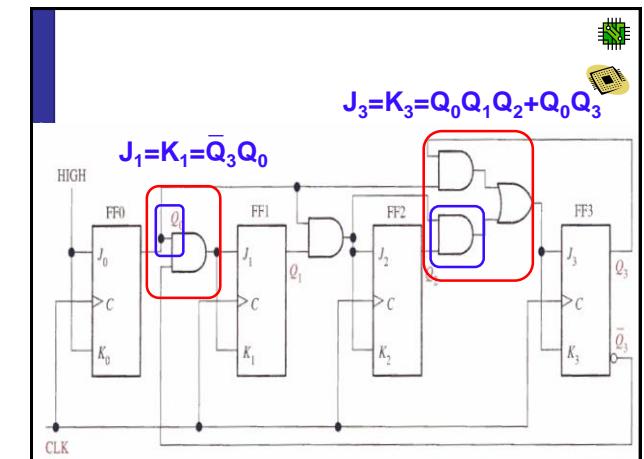
- For Q_0, Q_2 , no change for excitation equation
- For Q_3 : one more condition for Toggle
 $J_3 = K_3 = Q_2 Q_1 Q_0 + Q_3 \bar{Q}_2 \bar{Q}_1 Q_0$
- Partial decoding
 $J_3 = K_3 = Q_2 Q_1 Q_0 + Q_3 Q_0$
- For Q_1 : one more condition for NC
 $\bar{J}_1 = \bar{K}_1 = \bar{Q}_0 + Q_3 \bar{Q}_2 \bar{Q}_1 Q_0$
- Partial decoding:

$$\bar{J}_1 = \bar{K}_1 = \bar{Q}_0 + Q_3 Q_0 \Rightarrow J_1 = K_1 = \bar{Q}_3 Q_0$$

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Clock Pulse	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10 (recycles)	0	0	0	0

• MSI Chip

- 74HC160-module 10
- 74HC161-module 16
- 74HC163-module 16

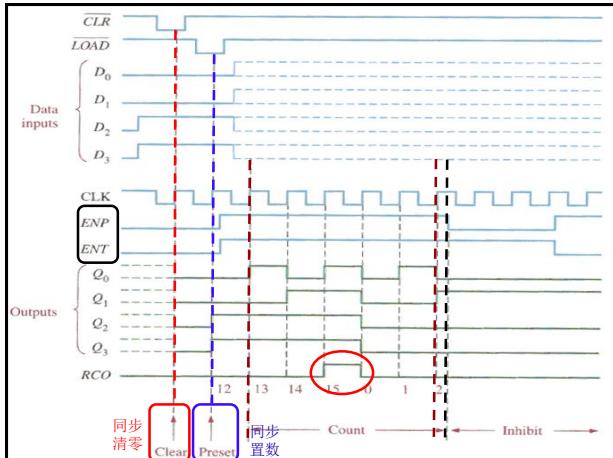
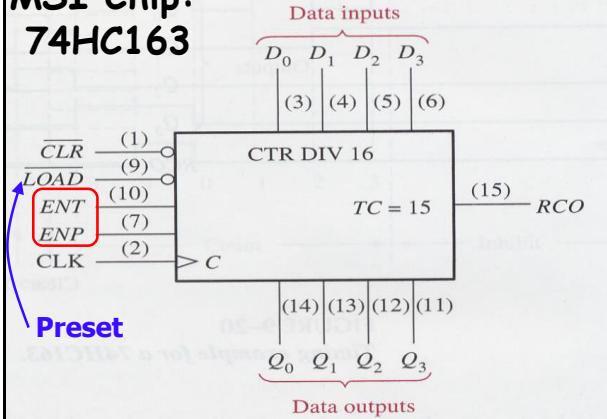
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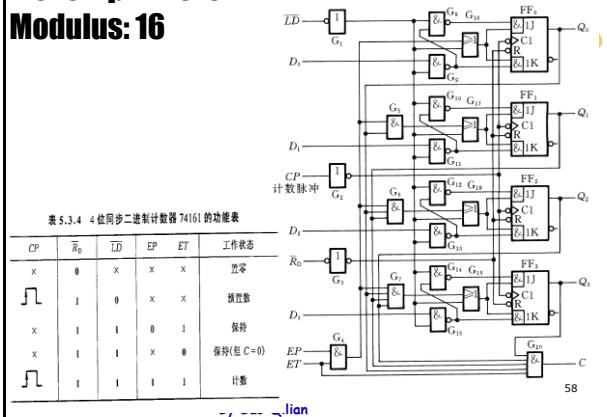


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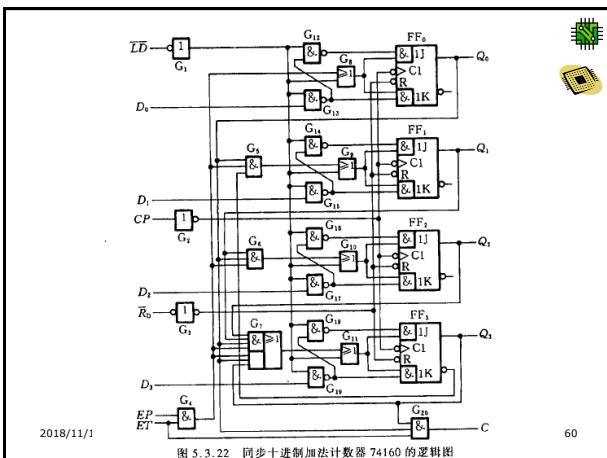
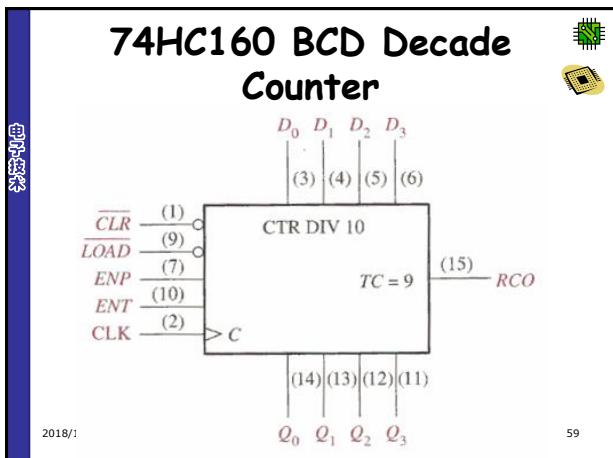
MSI Chip: 74HC163

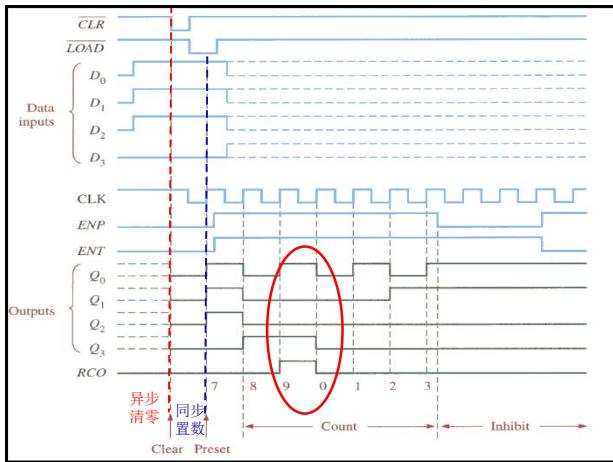


MSI Chip: 74LS161 Modulus: 16



异步置零, 同步置数





异步置零，同步置数

8.3 Up/Down Synchronous Counters

- A up/down counter (bi-directional counter)(加/减计数器或双向计数器)is one that is capable pf progressing in either direction through a certain sequence.

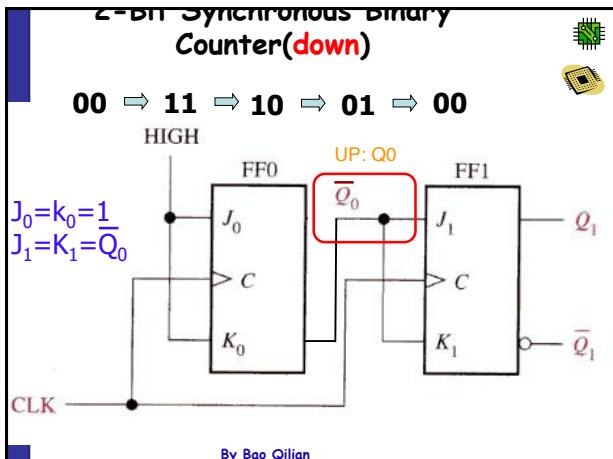
0,1,2,3,4,5,6,7→UP↑

7,6,5,4,3,2,1,0→DOWN↓

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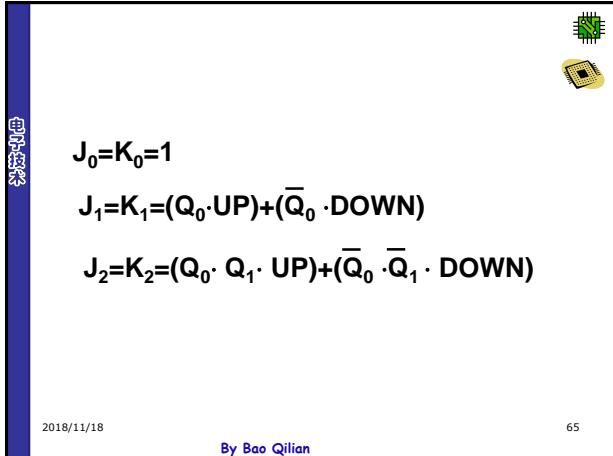
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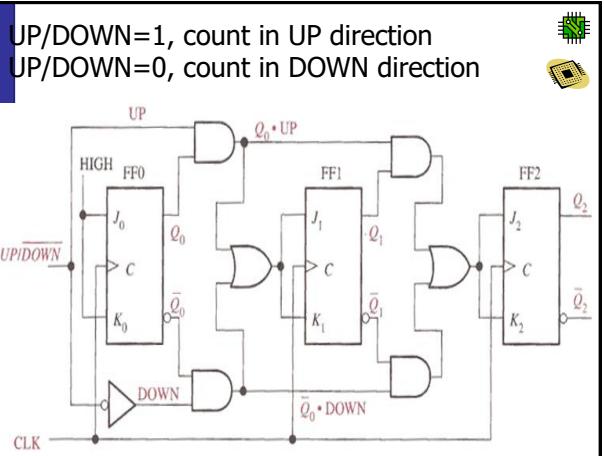
Clock Pulse	UP	Q_2	Q_1	Q_0	DOWN
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

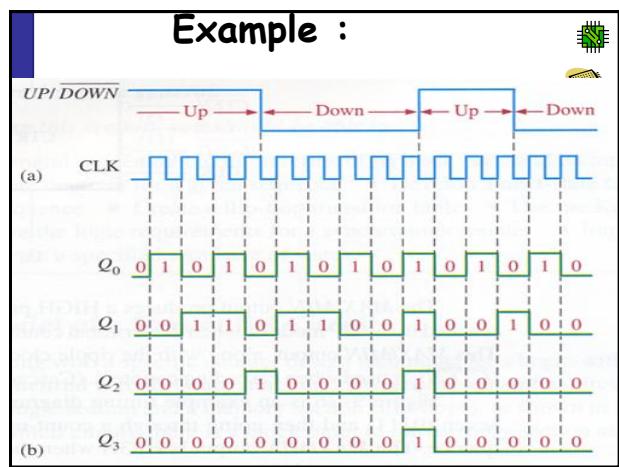
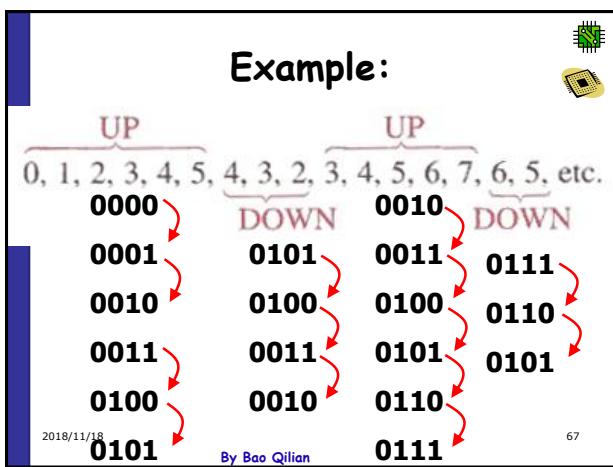


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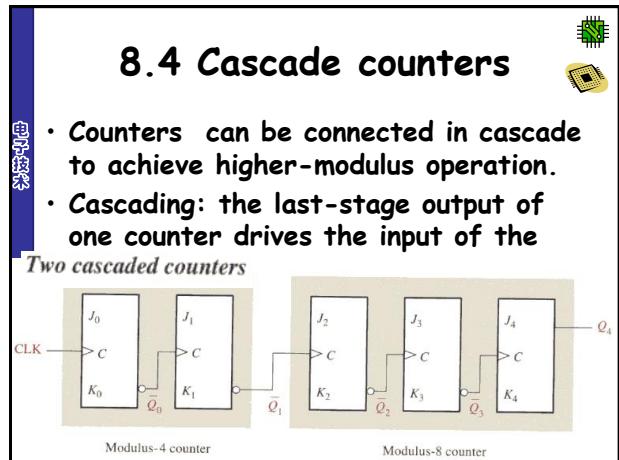
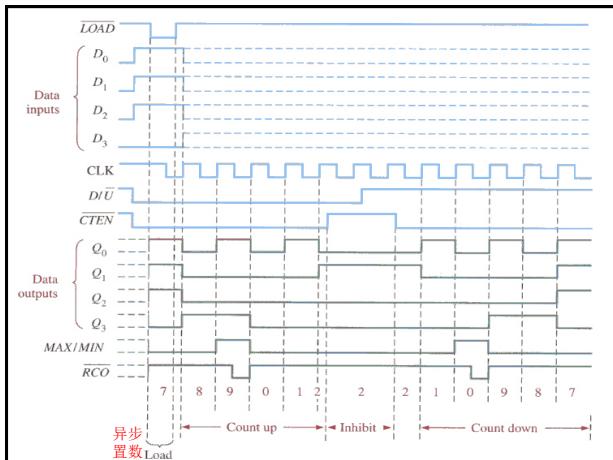
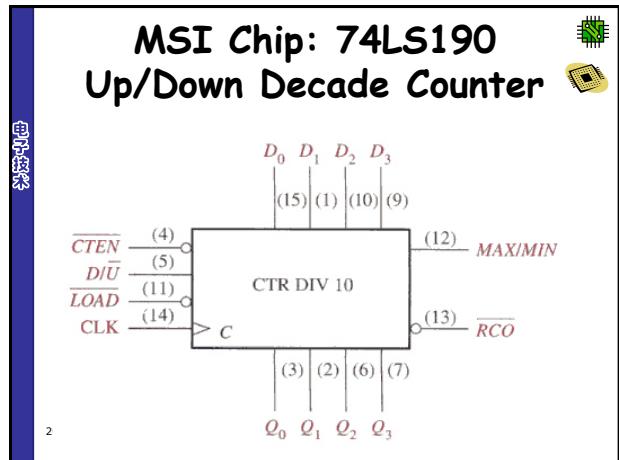


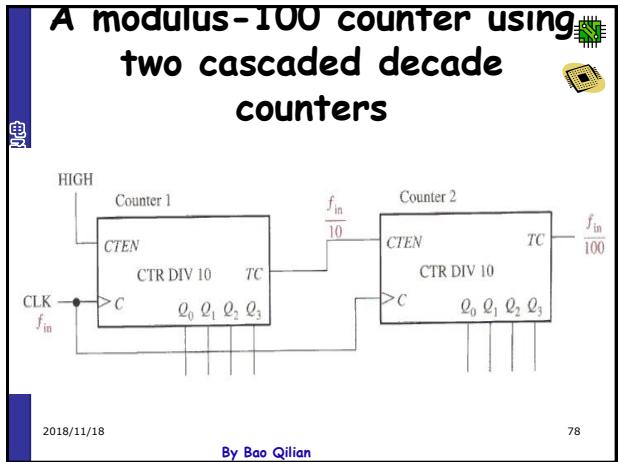
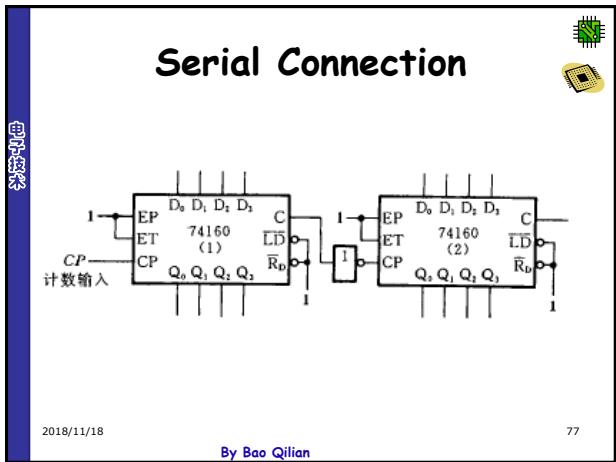
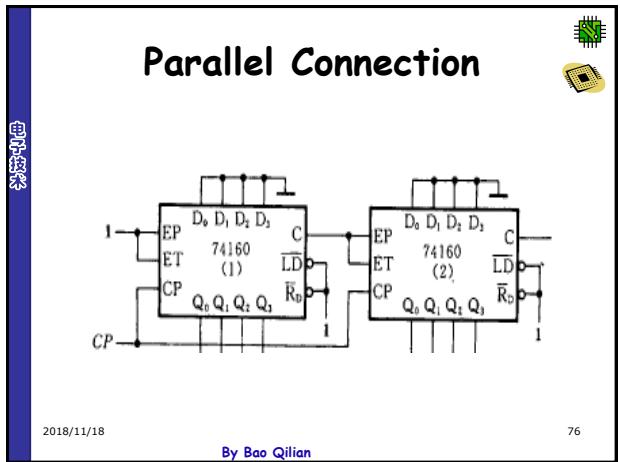
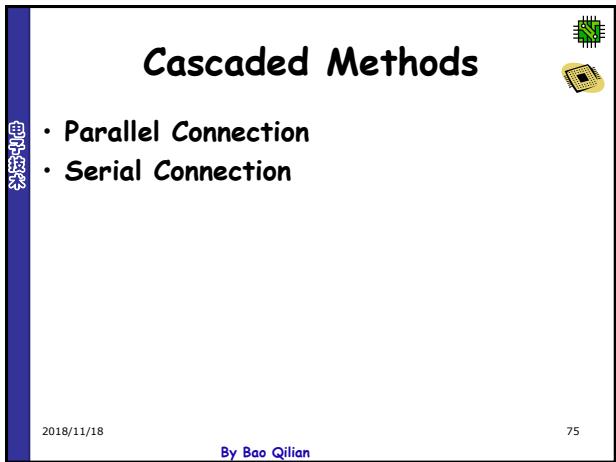
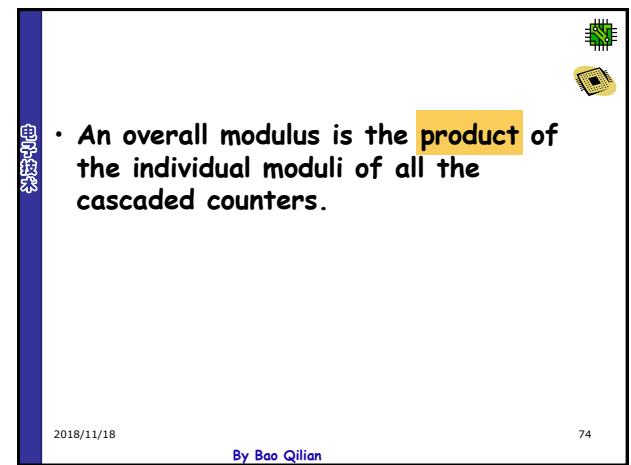
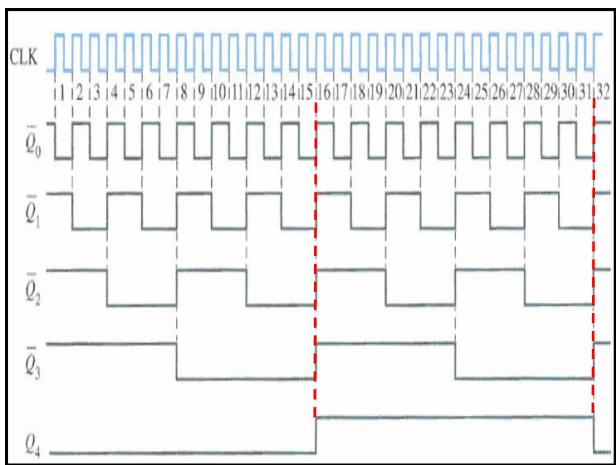
Sequence

Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	0	1	1
0	0	1	0
0	0	0	1
0	0	0	0
1	1	1	1
0	0	0	0
0	0	0	1
0	0	1	0
0	0	0	1
0	0	0	0

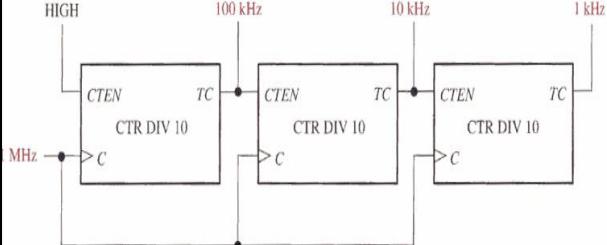
UP DOWN UP DOWN

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Frequency Divider



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Design of Any Modulus Counters

- RESET-based Design
- LOAD-based Design

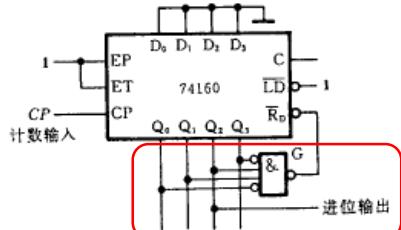
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RESET-based Counter Design

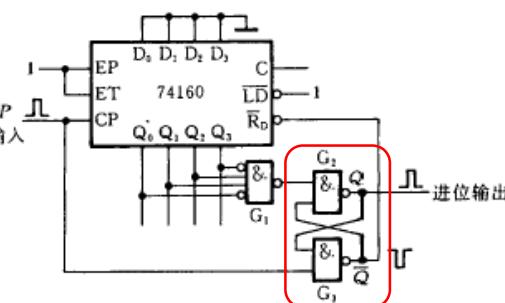
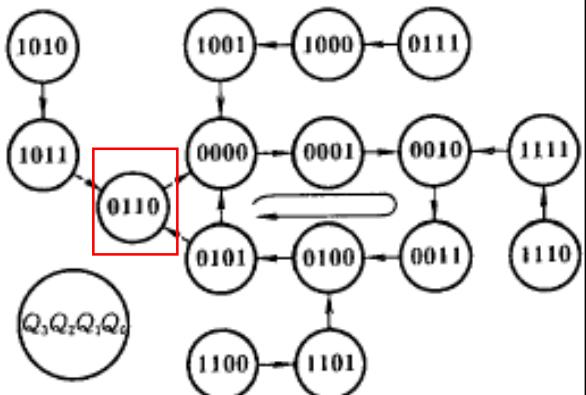
- Example:



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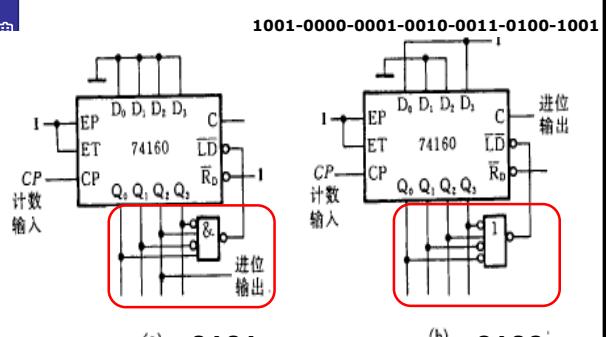


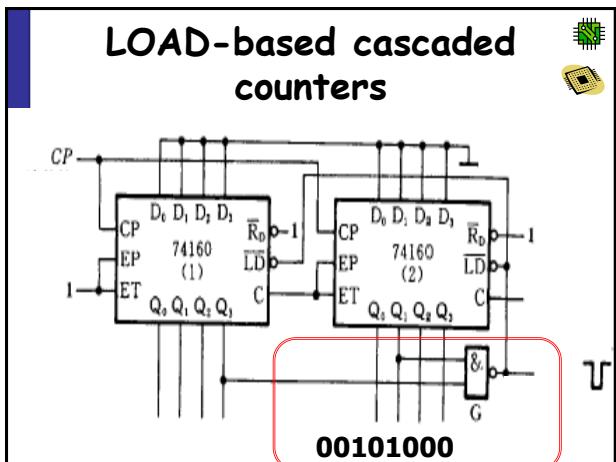
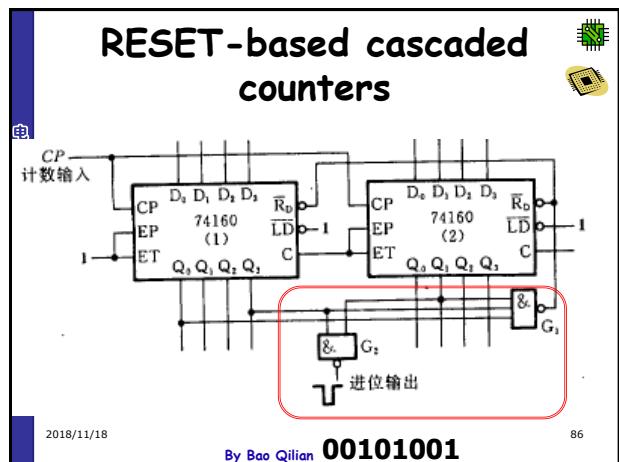
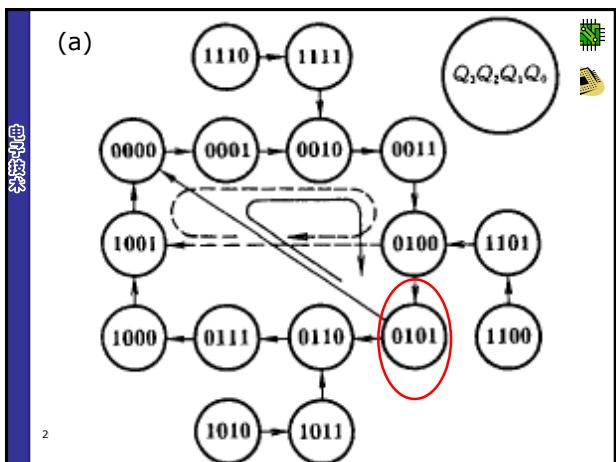
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LOAD-based Counter Design





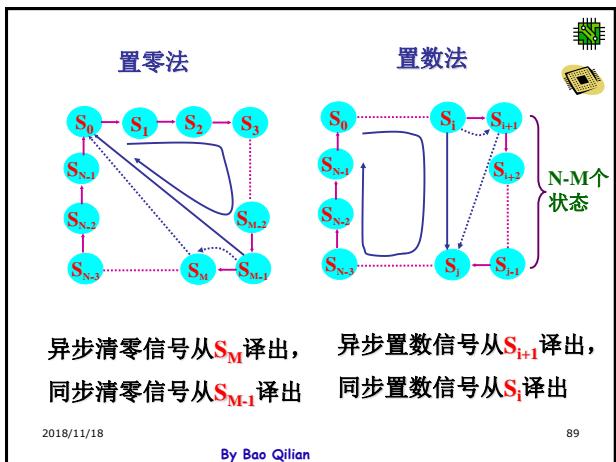
小结：任意进制计数器的构成方法

假定已有 N 进制计数器，需要得到 M 进制计数器

1. $M < N$ 的情况

在 N 进制计数器的顺序计数过程中，设法使之跳过 $N-M$ 个状态，就可得到 M 进制计数器
实现跳跃的方式有 **置零法** 和 **置数法**
置零法 适用于有置零输入端的计数器
置数法 适用于有预置数功能的计数器

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2. $M > N$ 的情况

必须使用多片 N 进制计数器构成 M 进制计数器
各片之间的连接方式：
串行进位、并行进位、整体置零、整体置数

若 M 可以分解为两个小于 N 的因数相乘即
 $M=N_1 \times N_2$

可采用串行进位或并行进位方式
串行进位： 低位进位输出信号作为高位时钟信号
并行进位： 低位进位输出信号作为高位计数使能信号

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当M为大于N的素数时，不能分解为N₁和N₂
必须采取整体置零或整体置数方式

整体置零：首先将两片N进制计数器按最简单的方式接成一个大于M的计数器（如N*N进制）
然后从M状态译出置零信号
将两片N进制计数器同时置零
基本原理和 M < N 时置零法一样

整体置数：基本原理和 M < N 时置数法类似

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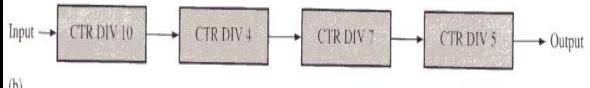
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Exercise: Determine the modulus



(a)



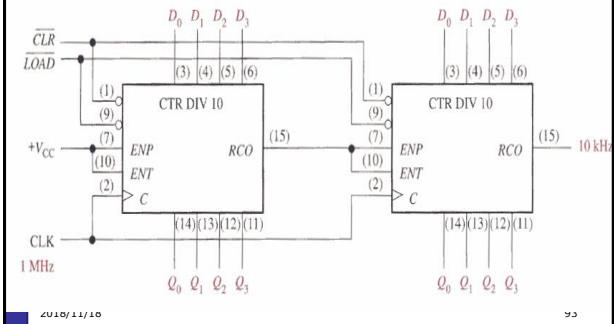
(b)

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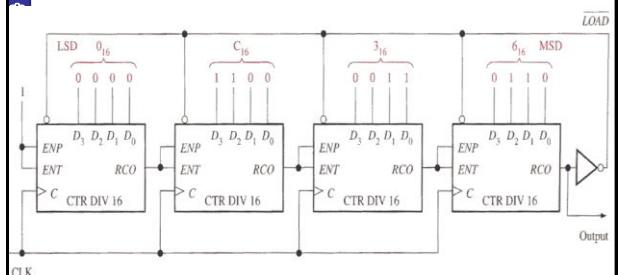
A divide-by-100 counter using two 74HC160



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Divide-by-40,000 counter using 74HC161

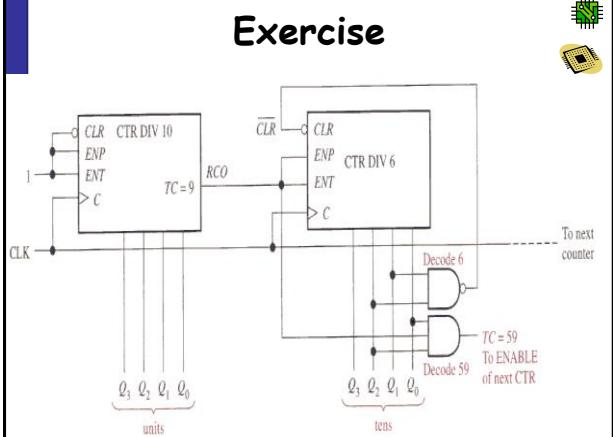


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Exercise



• Divide-by-60 counter

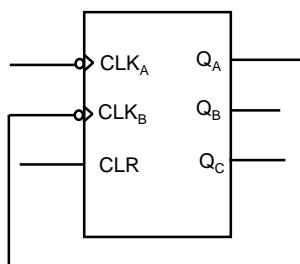
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MSI CHIP: 74LS57 (divide-by-60)

时序图
CLOCK
RESET

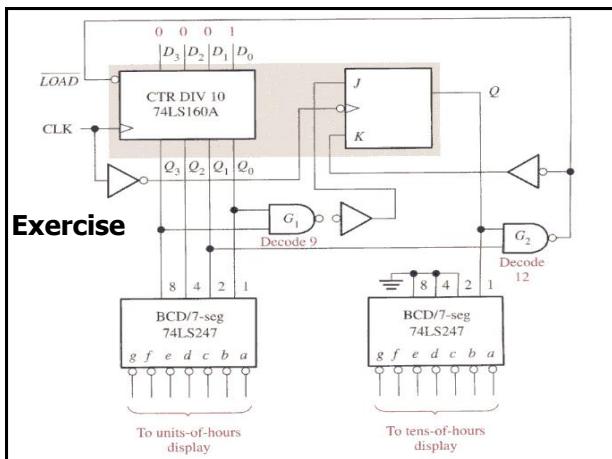
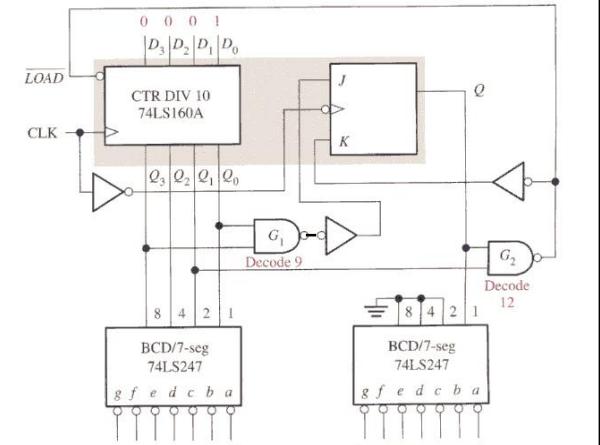


Divide-by-6
Divide-by-5
Divide-by-2

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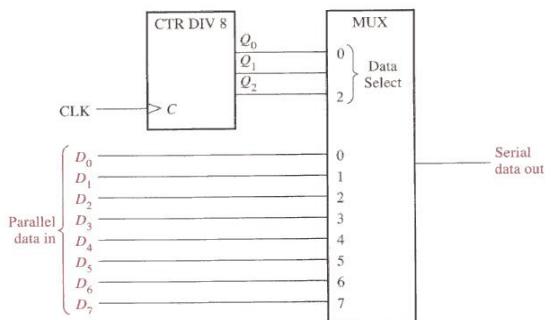
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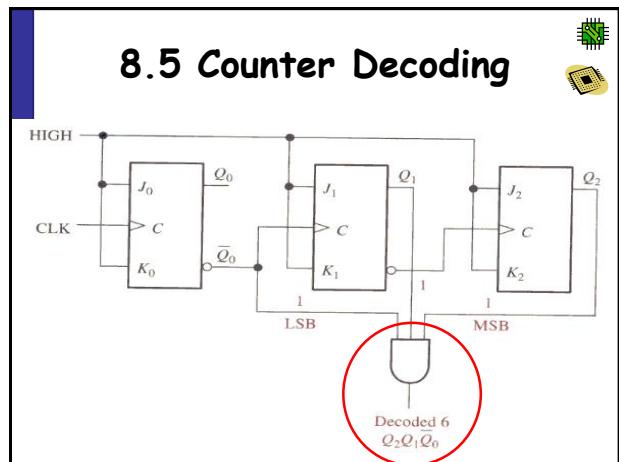
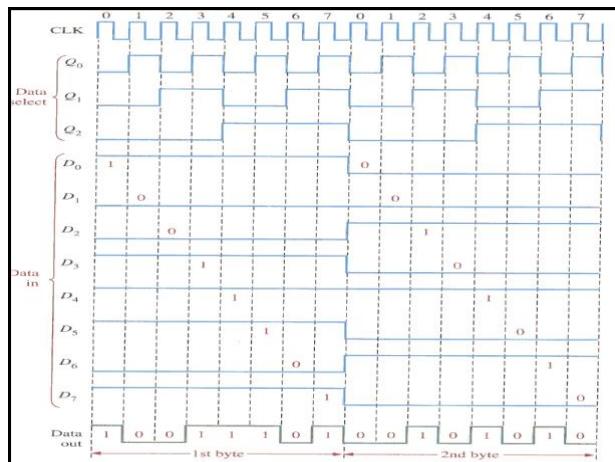


Exercise

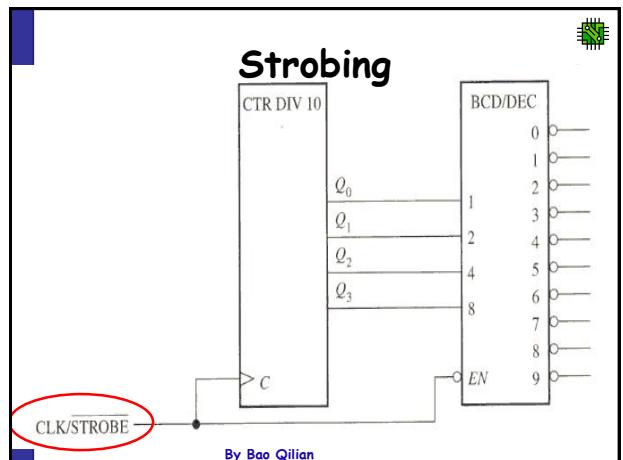
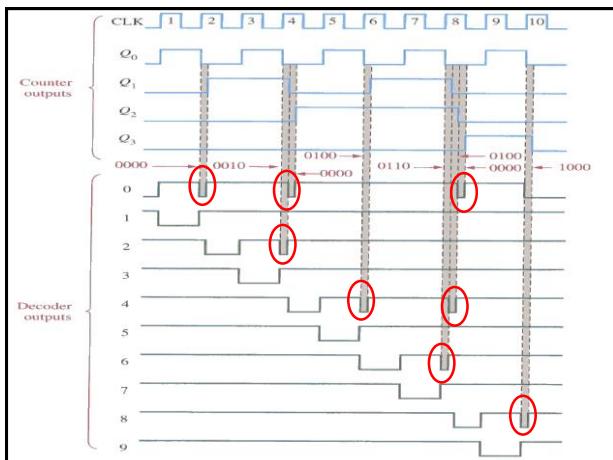
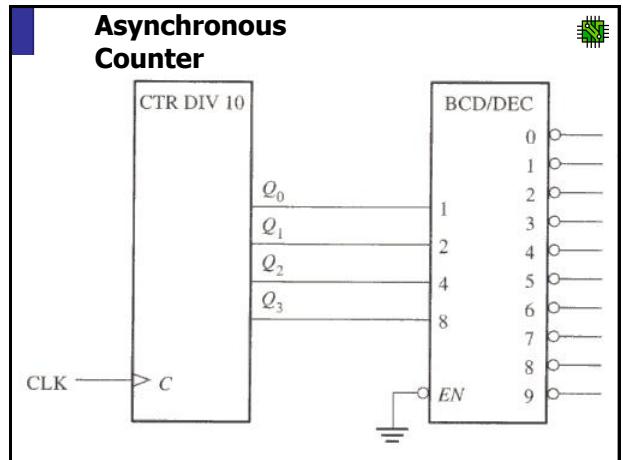
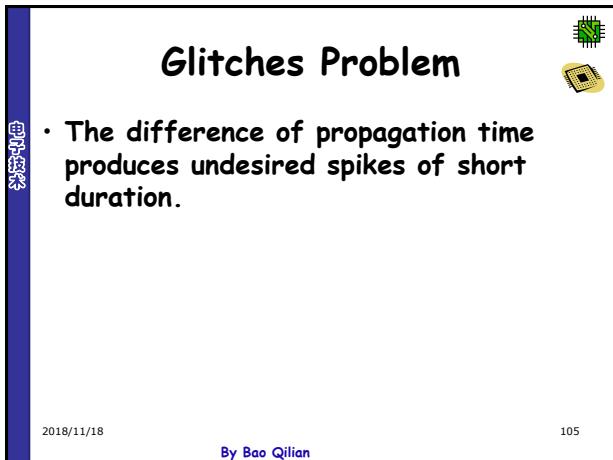
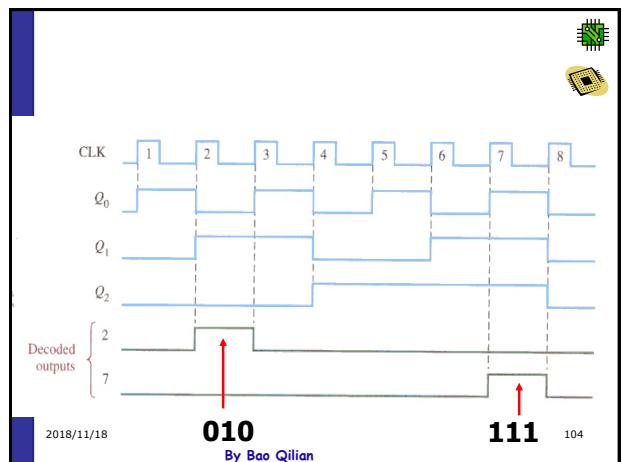
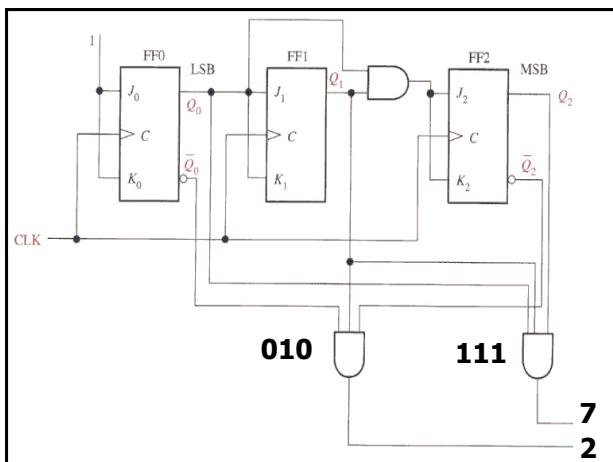
Parallel-to-serial conversion

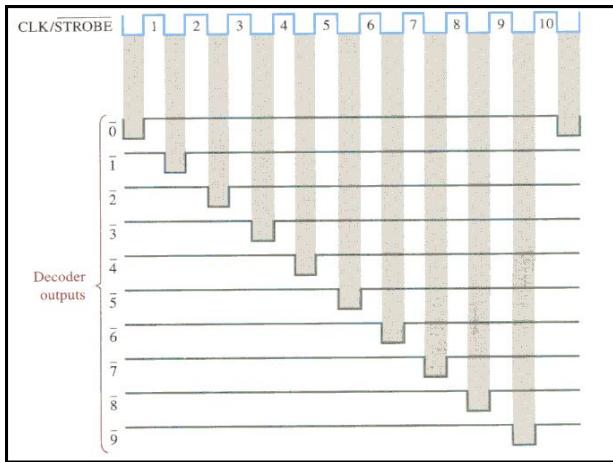


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8.5 Counter Decoding





Application Examples



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