

Direct Digital Pulse Width Modulation for Class D Amplifiers

Master Thesis preformed in Electronic Devices at the Department
of Electrical Engineering, Linköping University, Sweden

by

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LiTH-ISY-EX--07/3864--SE
Linköping 2007

Direct Digital Pulse Width Modulation for Class D Amplifiers

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Performed at:
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Linköping, 22 January, 2007

Presentationsdatum 2007-01-15 Publiceringsdatum (elektronisk version) _____	Institution och avdelning Institutionen för systemteknik Department of Electrical Engineering	 Linköpings universitet
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Språk _____ Svenska <input checked="" type="checkbox"/> Annat (ange nedan) Engelska / English Antal sidor 75	Typ av publikation _____ Licentiatavhandling <input checked="" type="checkbox"/> Examensarbete _____ C-uppsats _____ D-uppsats _____ Rapport _____ Annat (ange nedan) _____	ISBN (licentiatavhandling) ISRN LiTH-isy-ex--07/3864--SE Serietitel (licentiatavhandling) Serienummer/ISSN (licentiatavhandling)
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URL för elektronisk version http://www.ep.liu.se

Publikationens titel Direct Digital Pulse Width Modulation for Class D Amplifiers Författare Stefan Stark
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Sammanfattning / Abstract <p>Class D amplifiers are becoming increasingly popular in audio devices. The strongest reason is the high efficiency which makes it advantageous for portable battery-driven products.</p> <p>Infineon Technologies is developing products in this area, and has recently filed a patent application regarding an implementation of a part of the class D amplifier. The aim of this Master's thesis is to evaluate a digital open-loop implementation of a class D amplifier, using the pending patent solution, and discuss the differences from an analog closed-loop implementation.</p> <p>The focus has been on generating a high resolution PWM signal with a relatively low clock frequency. To achieve this, a hybrid of a counter and a self-calibrating tapped delay-line are used as a pulse generator. A model of the pulse generator was developed which made it possible to study how sampling frequency and different types of quantization affected quality parameters such as THD and SNR. With the results from the model two systems were implemented and simulated in HDL and as circuit schematics.</p> <p>The proposed digital open-loop class D amplifier was found to be useful in voice-band applications and for music. Since the open-loop structure suffers from poor rejection of power supply ripple, either error correction or a regulated power supply is needed. If much effort is put on the different parts of the amplifier the result can be really good but, depending on other constraints on the system, it may be simpler and less time consuming to use the analog circuit with feedback to achieve hi-fi quality.</p> <p>In summary, the combination of a counter and a self-calibrating tapped delay-line as a pulse generator is very useful in high resolution low-power systems. To avoid errors the delay-line and calibration can be made very accurate but with the expense of higher power consumption and area. However, the technique benefits from the small and fast logic devices available in deep sub-micron process technologies, which may finally lead to an advantage in power consumption and cost over the closed-loop analog solution.</p>
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Nyckelord PWM, Class-D, delay-line, calibration, direct digital modulation, delay element, high resolution PWM, open-loop amplifier

Abstract

Class D amplifiers are becoming increasingly popular in audio devices. The strongest reason is the high efficiency which makes it advantageous for portable battery-driven products.

Infineon Technologies is developing products in this area, and has recently filed a patent application regarding an implementation of a part of the class D amplifier. The aim of this Master's thesis is to evaluate a digital open-loop implementation of a class D amplifier, using the pending patent solution, and discuss the differences from an analog closed-loop implementation.

The focus has been on generating a high resolution PWM signal with a relatively low clock frequency. To achieve this, a hybrid of a counter and a self-calibrating tapped delay-line are used as a pulse generator. A model of the pulse generator was developed which made it possible to study how sampling frequency and different types of quantization affected quality parameters such as THD and SNR. With the results from the model two systems were implemented and simulated in HDL and as circuit schematics.

The proposed digital open-loop class D amplifier was found to be useful in voice-band applications and for music. Since the open-loop structure suffers from poor rejection of power supply ripple, either error correction or a regulated power supply is needed. If much effort is put on the different parts of the amplifier the result can be really good but, depending on other constraints on the system, it may be simpler and less time consuming to use the analog circuit with feedback to achieve hi-fi quality.

In summary, the combination of a counter and a self-calibrating tapped delay-line as a pulse generator is very useful in high resolution low-power systems. To avoid errors the delay-line and calibration can be made very accurate but with the expense of higher power consumption and area. However, the technique benefits from the small and fast logic devices available in deep sub-micron process technologies, which may finally lead to an advantage in power consumption and cost over the closed-loop analog solution.

Acknowledgements

I would like to thank my supervisor Dr. Mike Lewis for his help and expertise throughout the project. I am also grateful for the help from Mikael Hjelm who helped me with various technical questions when Mike was working in other parts of the world.

I would like to thank Professor Atila Alvandpour for believing in the project from the beginning and his positive attitude during the whole thesis work.

Finally thanks to Hans Bengtsson and Infineon for making this possible.

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Abbreviations

BTL	Bridge Tied Load
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analog Converter
DECT	Digital Enhanced Cordless Telecommunications
DLL	Delay Locked Loop
EMC	Electromagnetic compatibility
EMI	Electromagnetic interference
PCM	Pulse Code Modulation/Modulator
PDM	Pulse Density Modulation/Modulator
PSRR*	Power Supply Rejection Ratio
PWM	Pulse Width Modulation/Modulator
SNDR*	Signal to Noise and Distortion Ratio
SNR*	Signal to Noise Ratio
THD*	Total Harmonic Distortion
THD+N*	Total Harmonic Distortion plus Noise
V_t	Threshold voltage of transistor

*Defined in Appendix D

1 Introduction

1.1 Background

As the use of portable audio devices is increasing the demand for high efficient amplifiers is growing. The efficiency of classical linear amplifiers such as class A, B and AB is usually lower than 50 % while it is possible to get an efficiency greater than 90 % with a class D amplifier. The class D drawback is that large efforts need to be put on reducing the introduced distortion.

A class D amplifier uses pulse modulation, where a sequence of pulses are generated, at a much higher frequency than the input signal, which when low-pass filtered recreate the input signal. Usually pulse width modulation (PWM) is used. The output stage consists of switching transistors. This ideally results in power dissipation in the transistors only in the switching instant between the on and off states and therefore a high efficiency.

The "classical" way to do the pulse width modulation is to use a comparator to compare the analog input signal to a sawtooth signal. The result is a PWM signal where the width of each pulse is linear proportional to the amplitude of the input signal. But since many systems use digital samples to represent signals it is preferable to be able to do a direct digital modulation, i.e. to create the PWM direct from the samples.

There are several methods and algorithms to calculate the switching instants, resulting in more or less distortion. When the pulses are to be generated this can be done by using a counter to keep the pulse high for a number of clock cycles and low for the rest of the sample period. This solution would require a very high clock frequency for high quality audio (e.g. 48 kHz, 16 bits audio require a clock of 3.2 GHz) and is unreasonable for a low-power circuit. One way to get a lower clock frequency is to combine a counter with a tapped delay-line to get the smallest delay to be a fraction of the clock period.

Since the delay through each delay element in the delay-line is depending on temperature, the CMOS process etc. the delay through the delay-line needs to be calibrated. A method for calibration of the delay-line, to always have a total delay of one clock period, has been developed by Infineon Technologies and needs to be evaluated.

Typical products to use this application in are wireless speaker phones, mobile phones, laptops and other battery driven devices. At the moment a low power and low area voice-band amplifier is of interest at Infineon. The amplifier is to be used for the speaker phone function in a DECT project. For future products it is also interesting to look into the possibilities of achieving hi-fi quality.

1.2 Objectives

- Investigate how different parameters, in a direct digital modulator, affect the quality of the output signal.

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- Design a pulse generator based on a hybrid of a counter and a tapped delay-line with the aim to reach certain requirements and to minimize power consumption and chip area.
- Use as few analog parts as possible to avoid area consuming components such as large capacitors.
- Evaluate a calibration method for the tapped delay-line.
- Approximate the amount of distortion and noise the output stage will add, based on literature.
- Compare this solution with a corresponding analog class D amplifier.

1.3 Requirements

System clock frequency: 10 - 40 MHz.

PLL frequency available: 104 or 312 MHz.

CMOS process: 1.5 V, 0.13 μ m.

The aim is to minimize (in order of priority):

- a) Power consumption
- b) Chip area

1.3.1 Voice mode

Audio: 8 kHz sampled u-law / a-law encoded 8 bit audio (approx 12 bit linear)

Signal bandwidth: 3.4 kHz

SNDR: 50 dB (A-weighted, 1 kHz test signal)

PSRR: 50 dB*

1.3.2 Hi-fi mode

Audio: 48 kHz sampled 16-bit linear audio

Signal bandwidth: 20 kHz

SNDR: 76 dB (A-weighted, 1 kHz test signal)

THD: 0.1 %

PSRR: 50 dB*

*PSRR will not be affected by the design of the pulse generator in this work. It is strongly connected to the output stage and needs to be addressed in the design of the complete amplifier.

1.4 Method

Firstly, a literature study was done to examine prior art. The next step was to build and simulate a high-level model of the PWM pulse generation to get a good grip of what parameters are affecting the quality of the output signal. This was done with Synopsys Cocentric System Studio [33]. When this was done a good base had been achieved and the evaluation of the self-calibrating tapped delay-line started by designing and simulating it in the CAD tool Cadence [34]. On the basis of this work conclusions were drawn regarding the positive and negative properties of this solution.

2 The class D amplifier

A class D amplifier uses an output stage where the transistors are operated as switches. The power dissipation in the transistors is very low since the current through the transistor is zero when it is off and the resistance is low when it is on. These properties results in high power efficiency, usually more than 90 % and ideally 100 %.

More common amplifiers such as class A, class B and class AB have much lower efficiency but they are more linear. The efficiency of these devices are low because the transistors are working in the active region all or part of the time, i.e. they are somewhere between fully on and fully off, which leads to significant losses within the transistors. But the advantage of working in the active region is the output can be made proportional to the input, i.e. it is a linear device. In the figure below is a comparison in efficiency between class AB and class D amplifiers [15]. Also the principle of class D and class A are shown to the left of the efficiency comparison.

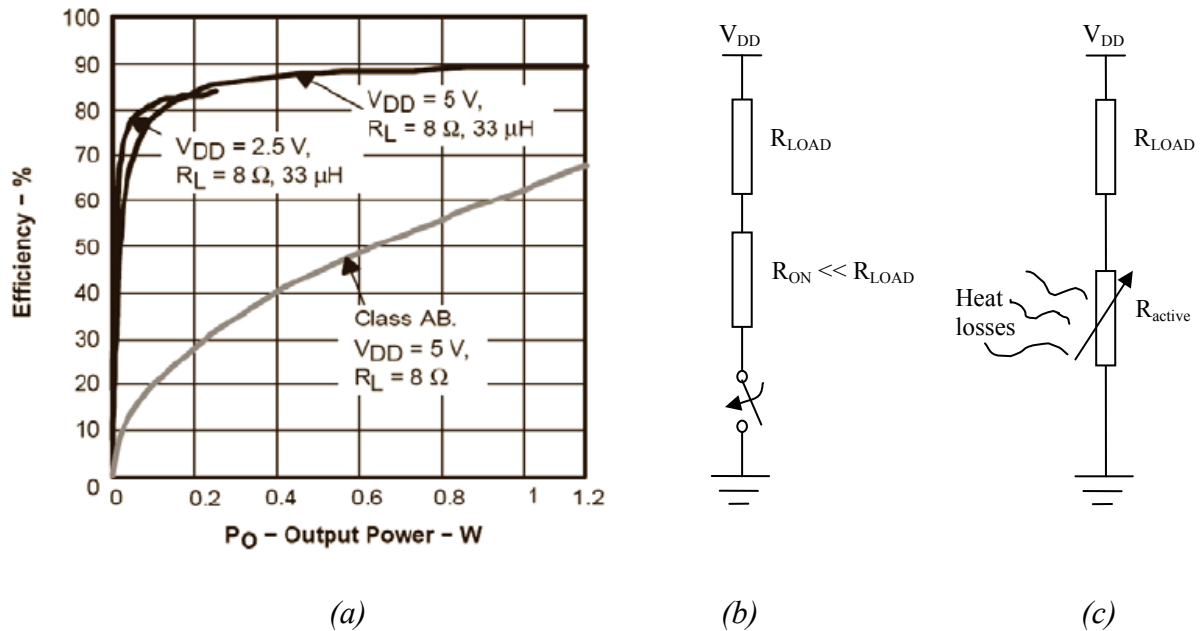


Figure 1. (a) Example: efficiency comparison between a class AB and class D. $P_{o,max} = 1.2\text{ W}$. (b) Class D principle. (c) Class A principle.

As the figure shows the efficiency is really poor at low levels for the class AB amplifier. The average person listens to a -40 dB music level (related to maximum output) 89 % of the time according to [10] ([12]). So by using the class D technique the battery time can be greatly increased in portable audio devices, especially at lower output levels. Another advantage, for higher power devices, is less or no need for heat sinks.

There are several techniques to generate a pulse train for the output stage to amplify [10]. Two common pulse modulation techniques are pulse width modulation (PWM) and pulse density modulation (PDM) (see figure below). PWM generates pulses with widths proportional to the input amplitude while PDM generates pulses with fixed width but

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where the density of the pulse train relates to the amplitude. A big drawback with PDM is the high number of pulses which causes greater switching losses, i.e. less efficiency.

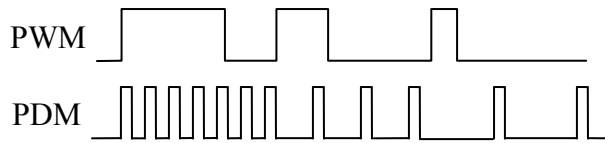


Figure 2. Example of PWM and PDM.

Delta-sigma ($\Delta\Sigma$) modulation is a popular method for PDM waveform generation that uses a high frequency bit stream as output and often about a 64 times oversampling. Delta-sigma can be used in class D amplifiers both for modulation and for quantization before doing the PWM. The advantage of using delta-sigma is that the quantization noise can be shifted away from the audio band (noise shaping). Using delta-sigma as pulse modulator causes high switching frequency due to the large oversampling [11] but it can be reduced by for example using bit flipping which is further described in [25]. A approach to delta-sigma is to use a self-oscillating circuit with hysteresis [27] which also is an alternative for modulation.

This thesis is based on the PWM technique. If the PWM sample frequency (carrier frequency) is high enough the input signal (modulating signal) can be recreated by low-pass filtering the PWM signal.

Depending on how each part of the class D amplifier is designed, different amounts of distortion and noise are added to the output [1],[2]. A general block diagram of the amplifier is shown in the figure below.

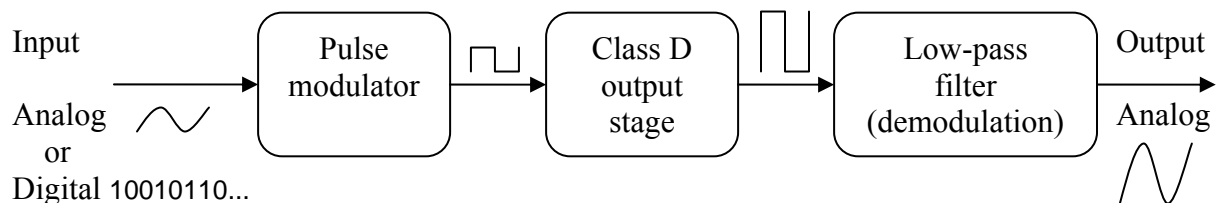


Figure 3. Block diagram of a general class D amplifier.

To get less high-frequency (carrier) harmonic components in the output spectrum it is possible to use three levels in the PWM-signal instead of the above two levels [10] (see figure below). It requires a more advanced circuit though, although in principle the work presented here can be applied in both cases. The abbreviations used for two and three levels of PWM are AD respectively BD where D stands for class D and A/B for in which order they where invented.

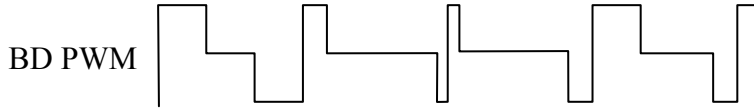


Figure 4. Example of three-level PWM.

2.1 Analog generation of PWM

The classic way to construct a pulse width modulator is to use a comparator and compare the analog input to a triangular or sawtooth signal thus getting a linear relationship between the amplitude of the input signal and the pulse width [3]. Depending of what kind of carrier that is used it is possible to modulate either the leading or trailing edge (sawtooth carrier) of the pulses, or both (triangular carrier). This sampling process is called natural sampling. One challenge in this case is to generate a linear carrier to minimize harmonic distortion. See figure below.

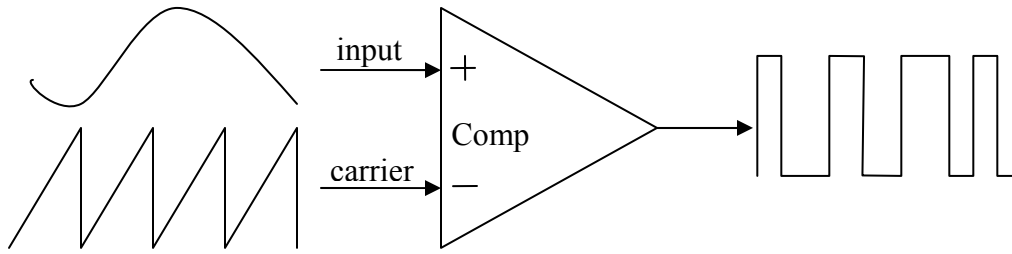


Figure 5. Analog PWM generator performing leading edge natural sampling.

2.2 Digital generation of PWM

If the input signal is digital it is preferable to do a direct digital modulation since the analog generation would require a DAC causing a lower overall power-efficiency [24]. See [29] for reference. The digital PWM can be divided into two parts as shown in the figure below.

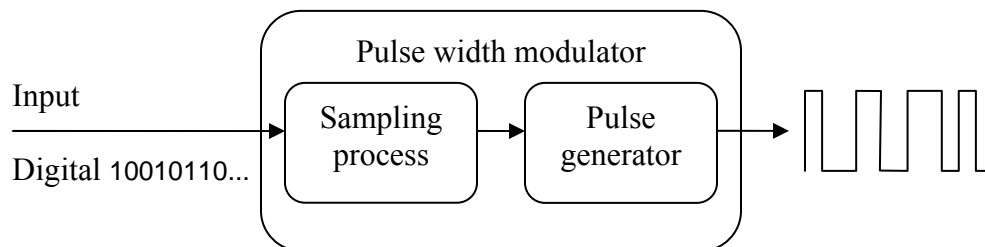


Figure 6. Digital pulse width modulator.

The input signal to the digital modulator is often pulse code modulated (PCM), meaning the samples arrives uniformly and represents the magnitude of the original signal with a binary word. This modulation is often called PCM to PWM conversion.

2.2.1 Sampling processes

To generate the PWM signal the most straightforward process, to find the switching instances, is the uniform sampling [2]. The width of the pulses in the uniform sampling process corresponds to the value of the digital input and this introduces non-linearity resulting in harmonic distortion. A comparison between natural and uniform sampling is shown in the figure below.

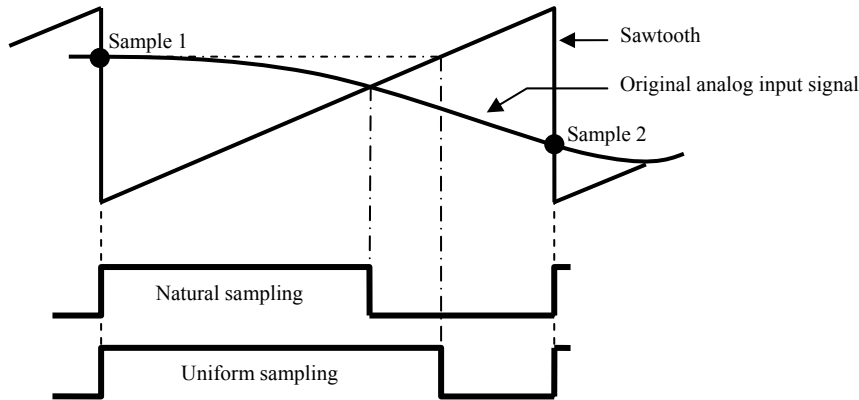


Figure 7. Comparison between natural and uniform sampling.

There are other sampling processes using algorithms to get as close to the natural sampling as possible to achieve a more linear system; in principle it is possible to achieve exactly the same result as in natural sampling, although at the expense of algorithmic complexity. Since these methods lie between the natural and uniform sampling they are called hybrid sample methods.

2.2.2 Pulse generator

The pulse generator creates the PWM signal based on the switching instances calculated by the sampling process. The accuracy with which the pulses can be created is a big issue in digital PWM and there are several methods [4] to generate the pulses. One way is to use a counter to count to each switching instant, but it would require a very fast system clock. As an example would a counter based pulse generator with 16-bit input and 100 kHz carrier frequency require several GHz clock frequency to get full accuracy. A solution for this is a “hybrid” pulse generator which is a combination of a counter and a tapped delay-line which makes it possible to generate pulses with higher resolution, not limited by the system clock. Another solution would be to use delta-sigma to quantize the input to a more reasonable bit length and shift the quantization noise away from the audio band and then use a counter to produce the PWM signal [11].

A simplified overview of the hybrid pulse generator is shown below.

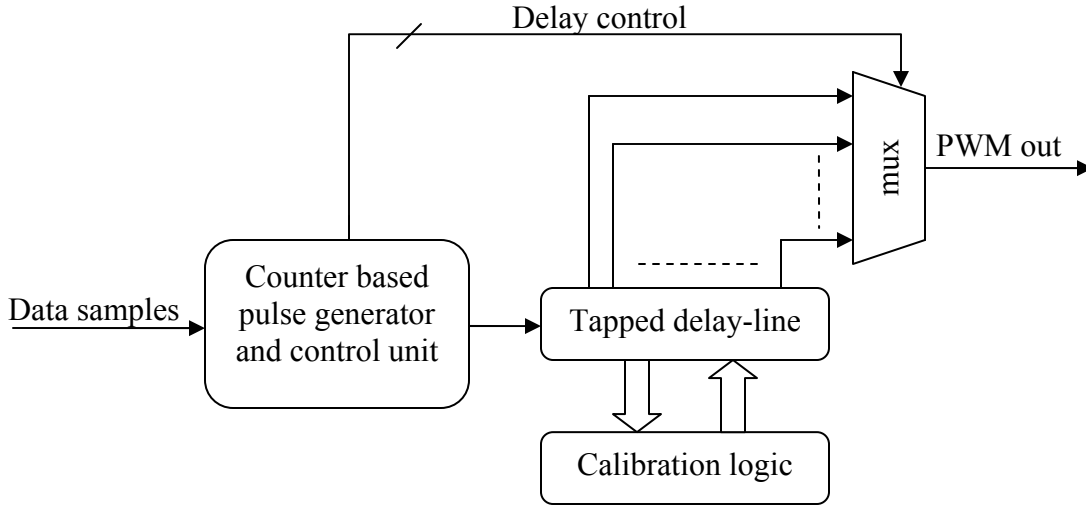


Figure 8. Hybrid pulse generator.

The delay-line is further explained in part 3.

2.3 Output stage

The class D output stage [6] amplifies the incoming pulses. A very simplified stage, actually an inverter, is shown below. Often, especially in low-voltage systems, an H-bridge (full-bridge) is used at the output to get double output voltage swing i.e. four times more power. An H-bridge is also illustrated below.

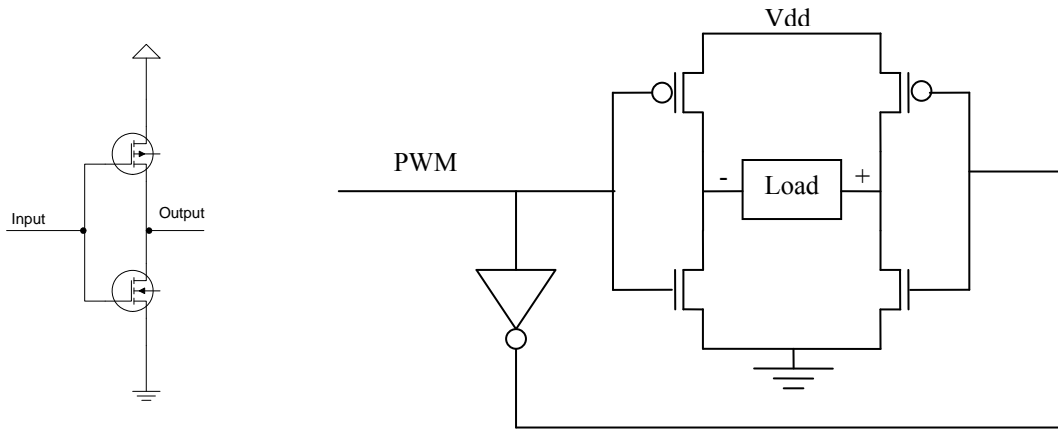


Figure 9. Simple output stage (half-bridge) and H-bridge (full-bridge).

If both a negative and positive supply voltage are available one can use the easier half-bridge and in such a way use less components [23]. In reality the output stage is more complex and contains, among other things, gate drivers.

Since the switching between the on and off stages is not ideal the output stage will add distortion and noise. It is important to handle the timing error that is introduced by the power stage. Any noise introduced by the power switch will be fed directly to the output if no error correction is used. There is also no rejection of power supply perturbations

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(zero PSRR) since, in the ON state, the output is directly connected to the power supply. Below is a comparison between an ideal output and an exaggerated expected output.

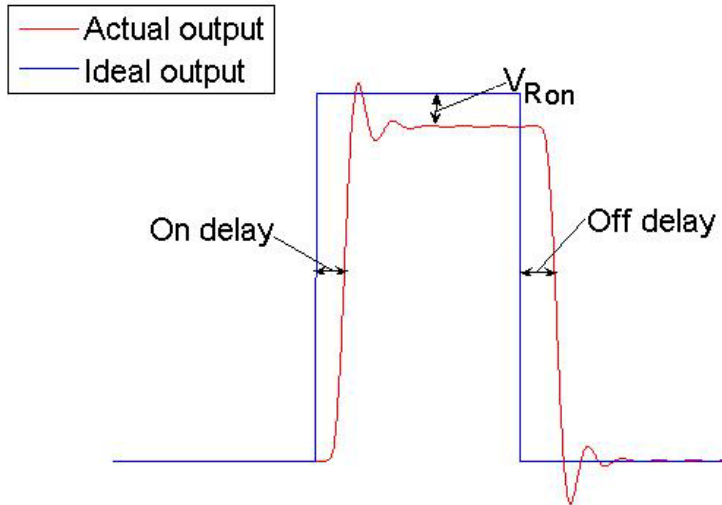


Figure 10. Example of power stage output.

2.3.1 EMI

Due to the quite large currents driven by the output stage EMI (electromagnetic interference) can be a problem. Harmonics of the carrier will radiate and also the ringing caused by under/overshoot in the switching instants. The ringing causes radiation in the 10 to 100 MHz region [18]. These effects can couple within the chip to the supply and ground rails, to the substrate, etcetera. It can also radiate to surrounding devices and interfere with these. When designing a class D amplifier it is important to have EMC (electromagnetic compatibility) in mind. The board layout and wiring should be designed to avoid current loops and the speaker wires can for example be laid out as a twisted pairs [15], [23].

2.3.2 Dead time and shoot through

The dead time is the time when both the NMOS-net and PMOS-net in a CMOS circuit are turned off. Dead time is needed to avoid shoot through, when both NMOS and PMOS are conducting, which causes a large current between the power rails due to the low on resistance of each transistor. Large currents can damage the transistors, and causes unnecessary power dissipation, so it is important to avoid. The dead time introduces another source of non-linearity though, so the goal is to keep the dead time as low as possible without causing any shoot through [19]. Dead time is handled by the output stage driver.

2.3.3 Power dissipation

Most of the power dissipation in the class D amplifier is generated in the output stage [14]. Conduction losses (MOS on losses), switching losses (shoot through) and capacitive losses (gate capacitance) are the three main contributors to the total dissipation. This can be summarized in the below equations[19], [32].

- Direct Digital Pulse Width Modulation for Class D Amplifiers -

$P_{diss} \approx P_{cond} + P_{sw} + P_{cap}$	R_{on}	—	Resistance of MOS when on
$P_{cond} = R_{on} I_{D,rms}^2$	I_D	—	Drain current
$P_{sw} = V_{DD} I_{D,peak} T_{sw} f_{pwm}$	V_{DD}	—	Supply voltage
$P_{cap} = 2C_G V_{DD}^2 f_{pwm}$	T_{sw}	—	Switch time
	f_{pwm}	—	PWM frequency
	C_G	—	Gate capacitance

Since both R_{on} and C_G are wanted small it is a trade-off between these. A small on resistance would require a large transistor with significant gate capacitance. The $R_{on}C_G$ product is an important parameter to minimize for the power transistor manufacturers [23].

2.4 Demodulation filter

To recreate the analog signal the PWM signal is low-pass filtered to remove the carrier frequency and high frequency products. An illustration of this is shown in the figure below.

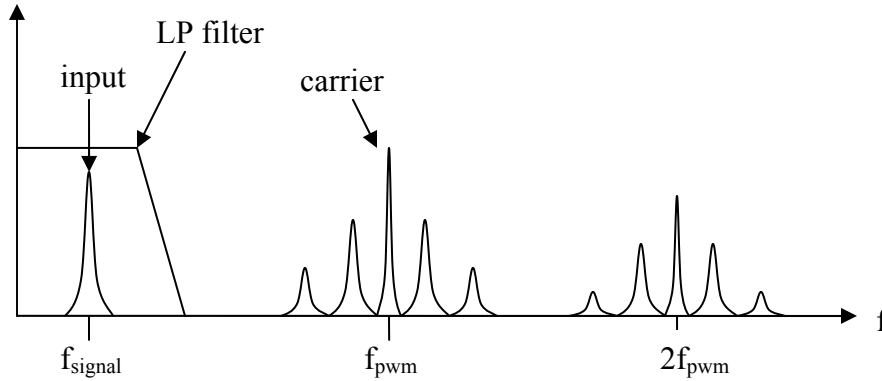


Figure 11. Recreation of the analog signal.

To get a good fidelity of the output signal it is important to remove all the high frequency components of the PWM. Letting high frequencies pass on to the speaker could overload it and if it is non-linear cause unwanted signals in the audio-band by intermodulation. High frequencies can, as mentioned earlier, also cause EMI. Removing the high frequency components often requires high-order filters which contain expensive and bulky inductors. If the three level PWM (BD) is used it is possible to relax the requirements of the demodulation filter since the carrier components are not as intense as with two level PWM (AD). Also, complexity of the filter can be traded against higher power consumption by increasing the switching frequency. Sometimes it is even possible to run without a filter [17] if the speaker can handle the high frequencies. There are other ways to suppress the high frequency components as well such as using a feed-forward network to counteract the switching frequencies at the speaker [16].

One problem with the filter is that it has high sensitivity to load variations [22]. Every filter is specified to work with a specified load. If the load changes, the properties of the filter changes as well. Firstly, the load of speakers are not always the same, four and eight ohms are common though. Secondly, the specified impedance of a speaker is just an

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overall value, actually it changes with frequency and can for example change between 2 Ω and 30 Ω . Of course can every component be affected by temperature, tolerances etcetera as well. A typical demodulation filter is shown below.

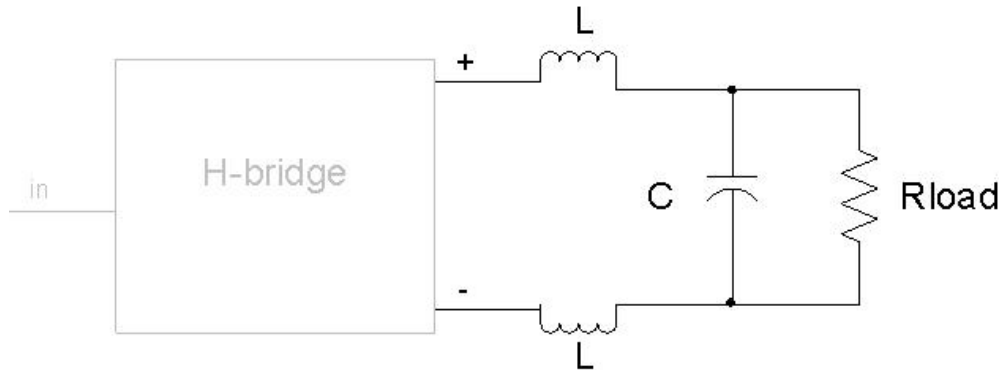


Figure 12. Typical demodulation filter: Second order Butterworth LC filter (BTL).

2.5 Error correction

There are several methods used for error correction such as multiple-loop linear feedback, feed-forward and non-linear feedback [13]. By using these methods it is possible to enhance linearity of the complete system and it results in better THD and PSRR [5][11]. Feedback is often used in analog systems. Even though feedback complicates the amplifier design and stability is an issue that needs to be addressed, it is important to be able to achieve linearity.

In pure digital systems it is harder to implement feedback since the most straightforward way would be using analog circuits. The digital systems are often designed in an open-loop structure where other methods are used to try to enhance linearity like trying to precompensate for different expected errors like timing errors and nonidealities in the modulator [23], [26].

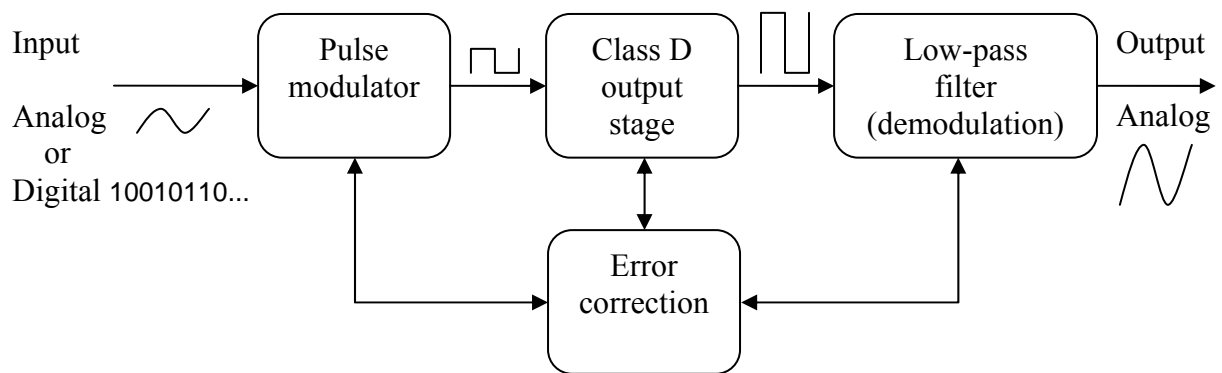


Figure 13. Class D system with error correction.

3 Delay-lines

A tapped delay-line is a series of delay elements where the input signal is delayed fractions of a clock cycle. The total delay through the whole delay-line should be exactly one clock cycle. An example of a delay-line is shown below.

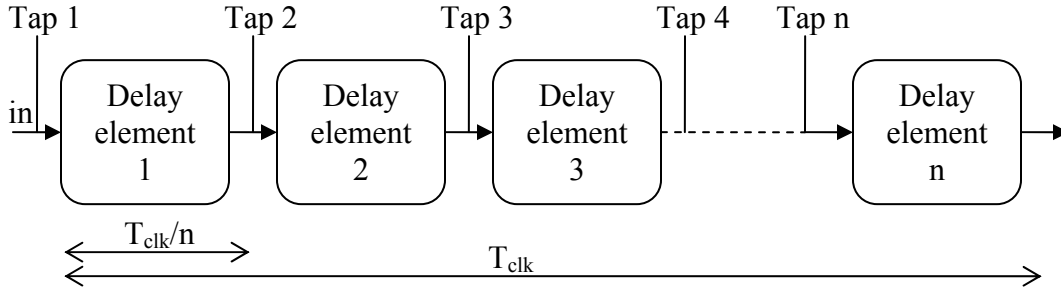


Figure 14. Example of a tapped delay-line

Since variations in the CMOS process and the temperature etcetera will affect the delay the delay-line needs to be calibrated [7], [8] to compensate for these variations. Often this is called a delay locked loop (DLL). Normally DLLs are used in systems to generate multiple-phase clocks [31]. An overview is shown below.

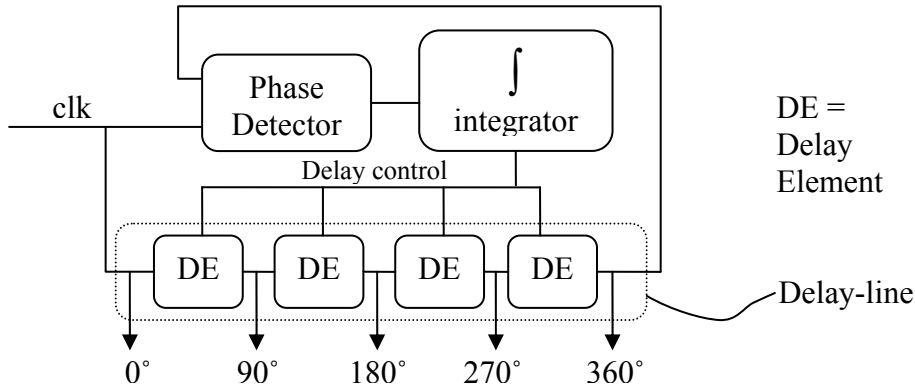


Figure 15. DLL for multiple-phase clock generation.

One common way to implement the integrator in the above figure is to use a charge-pump and loop filter. The charge-pump generates a voltage which is active for a period of time according to the phase difference detected by the phase detector. The voltage is filtered by the loop filter and the resulting voltage level controls the delay elements. To avoid as much analog parts as possible a digital calibration circuit will be used in this work.

As the pulses in our case are arriving at the input with a width of a number of clock periods the pulse is compared to the signal delayed one clock cycle by a D flip-flop. To be able to detect errors in the total delay a SR-latch is used to detect differences on the falling edge. The principle is presented in the figure below.

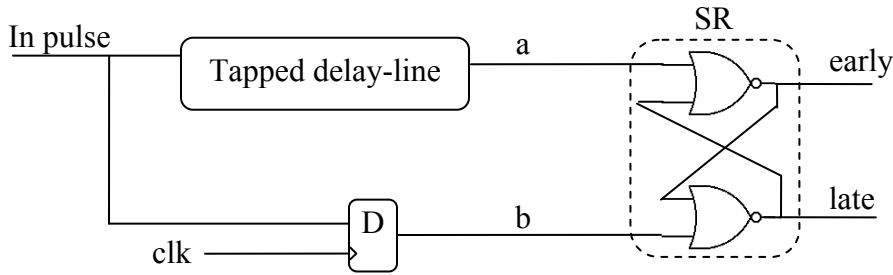


Figure 16. Delay-line with falling edge error detector.

The signals early and late are handled by the calibrator which calibrates the delay-line to delay the signal exactly one clock cycle. Below the functionality of the SR-latch is shown.

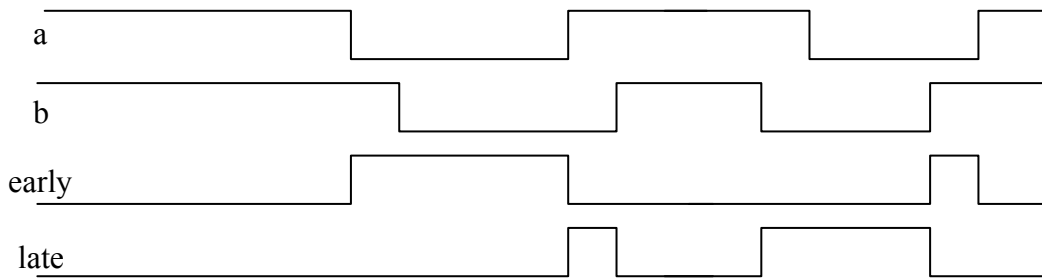


Figure 17. Inputs and its corresponding outputs of the falling edge error detector.

The order of arrival of the two inputs can be determined with a precision of less than one picosecond [20]. If the inputs arrive very close the circuit will enter a metastable state where both the outputs attempt to go high. This will not be a problem since the pulses at the output are sampled a clock edge later and, if the device is symmetrical and matched right, the input that arrived first will gain a small advantage and have time to resolve the metastability. A corresponding setup of the SR-latch with NAND gates can be used to detect differences in the rising edge. By using both of these SR-latches it is possible to calibrate both the rising and falling edges and in such a way not limit the accuracy with which each flank can be calibrated. This calibration solution (together with a class D amp) is protected by a pending patent [8]. As can be viewed in the above figure there will always be a small pulse on the “wrong” output before the SR-latch is reset. This pulse does not affect the calibrator because the early/late signals are sampled before its arrival.

3.1 Delay elements

A simple way to construct a variable delay element is by using a couple of chains of logic gates and a multiplexer. See example in figure below.

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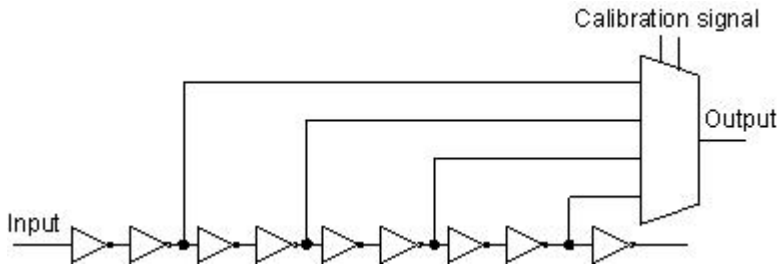


Figure 18. Delay element using inverters and a multiplexer.

The multiplexer is used to choose the appropriate delay. Under normal conditions we ought to be using a delay through a chain in the middle. A slow condition would require a shorter chain and a fast would require a longer to compensate for the delay change in each inverter.

If finer tuning is needed a more complex solution would for example be to adjust the driving ability of each inverter [9] or to have separated chains with two inverters each where these are sized differently between the chains. The latter would require a large driving ability on the output of the multiplexer to be able to drive the large input capacitance of the next delay element. Another more complex option is to use an adjustable voltage regulator to vary the supply voltage of the inverters (this gives in principle a continuously variable range of delays) or to use current starved inverters or shunt capacitor delay elements which all can be controlled by a voltage [30]. Vernier delay lines [21] is also a option which is based on two slightly different delay-lines in parallel. The delays of the two lines are compared and the difference is a pulse with very high resolution. Some of the above mentioned circuits are shown below.

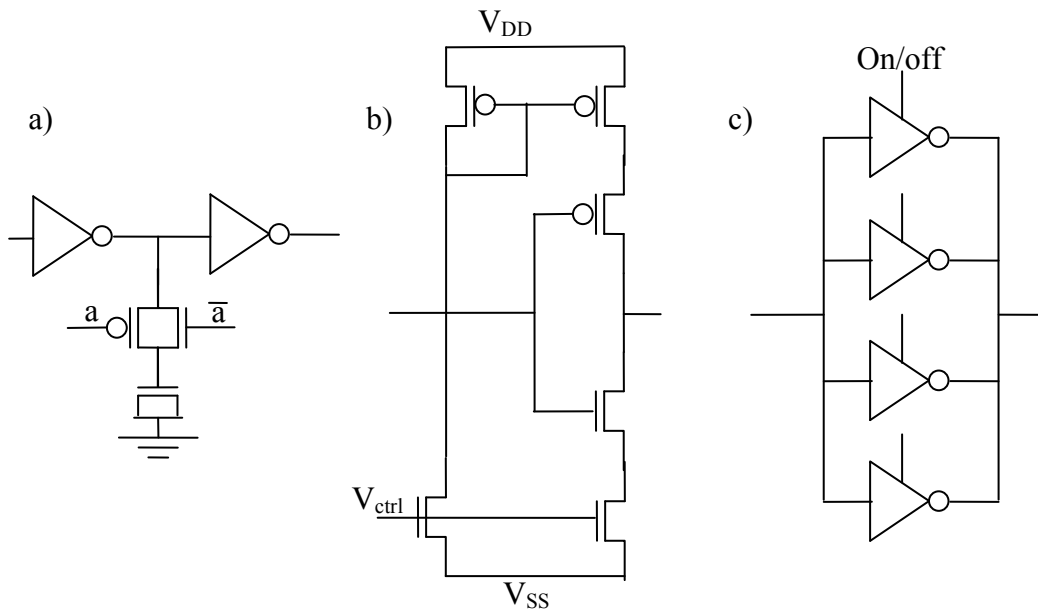


Figure 19. a) Shunt-capacitor delay element. b) Current starved inverter. c) Inverter arrangement to control driving ability.

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The drawback of systems that are controlled by a varying voltage is, as already mentioned, the need of filtering. Capacitances and inductors are very area consuming when placing them on-chip and using discrete components off-chip is neither preferable since nowadays cheap single-chip solutions is what the customers are looking for.

4 High-level simulations of distortion and noise

To be able to study how different implementations of the digital pulse width modulator affect the quality of the signal a model of the pulse width modulator was programmed in Synopsys Cocentric System Studio. The sampling process used is natural sampling where the switching instances are calculated from a deterministic signal through the binary search algorithm. The sampling instants are converted into a pulse train represented as a uniformly sampled discrete time signal, containing the duty cycle, so that conventional signal processing / analysis can be performed. A fifth order Butterworth low-pass filter step response is used in the pulse generator to generate a sampled signal with the cutoff frequency chosen so as to fulfill the Nyqvist criterion at the chosen sampling frequency. By changing the cutoff frequency of the filter it can also be used to do the low-pass filtering to generate the final wanted signal in the same step as the PWM generation. This is why a quite high order filter is chosen, to heavily suppress the high frequencies. See Appendix A for source code. An overview of the system is shown in the figure below.

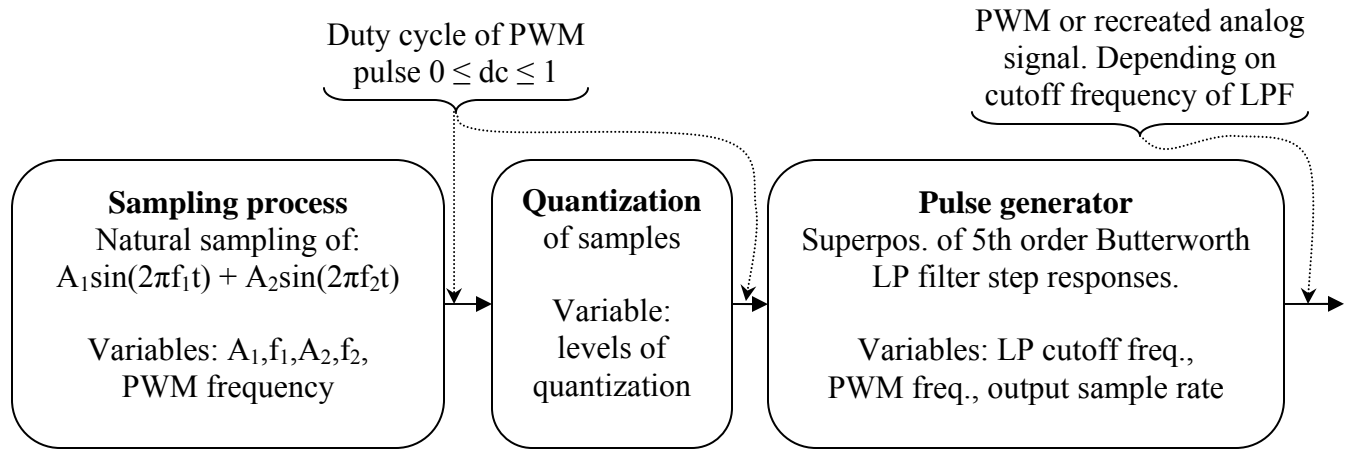


Figure 20. System Studio simulation setup.

With this setup it is possible to compare lots of cases where one for example can study how the quantization or the PWM frequency affects the signal quality. The quantization models the time resolution in the circuit, i.e. the delay through a delay element. The maximum input amplitude of the sine-signal should be 1 to keep the modulation index equivalent or lower than 1.

The principle for generating the pulses with step responses is shown below.

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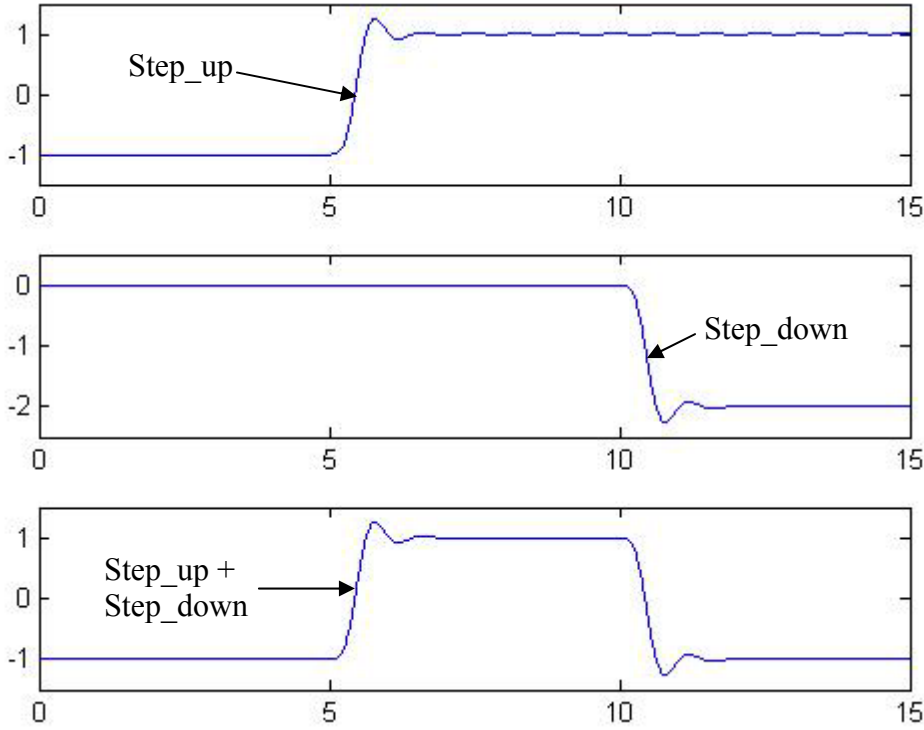


Figure 21. Pulse generation with step responses of a low-pass filter.

Each output sample was generated by adding the contribution of the current input duty cycle and a number of saved earlier duty cycles. A more mathematical explanation of how to generate one output sample is provided below.

$s(t)$ – step response of low-pass filter

Δt – amount of time elapsed from the start of the PWM pulse to the current sample

n_{\max} – number of saved earlier duty-cycle inputs

$\text{mem}[i]$ – vector containing the earlier duty-cycles, $0 \leq i \leq n_{\max}$

$$up = \sum_{n=0}^{n_{\max}} s(\Delta t + nT_{pwm})$$

$$down = \begin{cases} \sum_{n=1}^{n_{\max}} s(\Delta t + T_{pwm}(n - \text{mem}[n])) & \text{when } \Delta t < T_{pwm} * \text{mem}[0] \\ \sum_{n=0}^{n_{\max}} s(\Delta t + T_{pwm}(n - \text{mem}[n])) & \text{when } \Delta t \geq T_{pwm} * \text{mem}[0] \end{cases}$$

$$out = 2(up + down) - 1$$

An example of the spectrum for the PWM signal and the recreated signal are shown below. If nothing is specified, the spectrums presented in this report are generated with the Matlab function `pwelch` using default settings.

- Direct Digital Pulse Width Modulation for Class D Amplifiers -

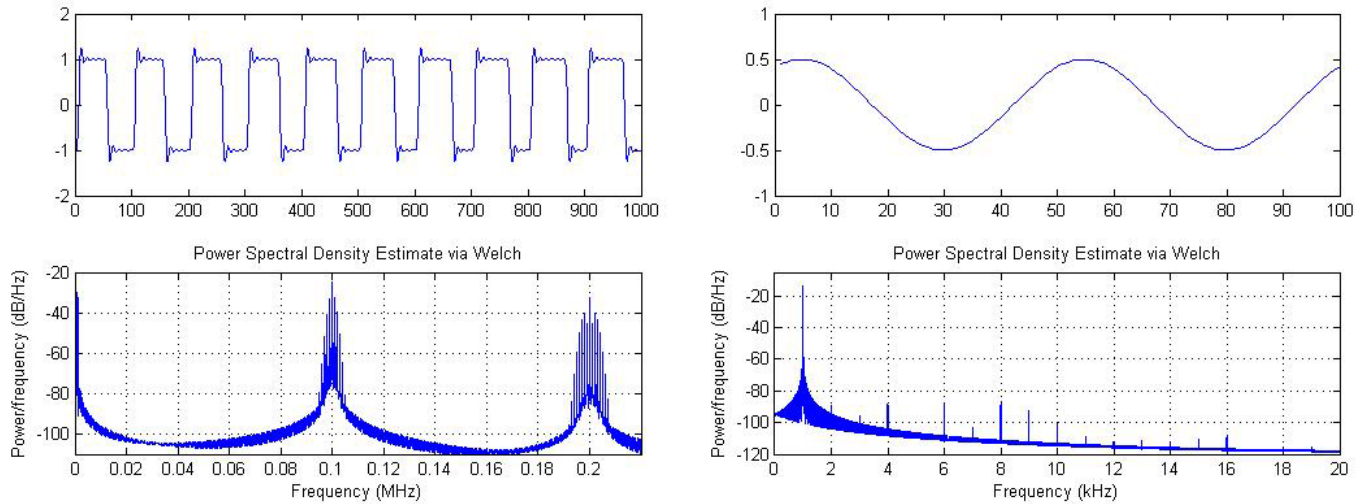


Figure 22. PWM signal and filtered PWM signal with spectrums.

4.1 Ideal delay simulations

To get a feeling of how the PWM sampling frequency (f_{pwm}) and the quantization of the duty cycle affects the quality of the signal the above model of the direct digital modulation was simulated. Three different quantization methods were used with the following setup.

- Input: $0.5\sin(2\pi 1000t)$, this means a modulation index, M , of 0.5
- Frequency span for calculations: $0 < f < 25$ kHz
- Pulse generator output sample frequency: 50 kHz
- Low-pass filter cutoff frequency: 3.4 kHz or 20 kHz
- PWM frequency: 100 – 500 kHz
- Quantization bits: 7 – 16

4.1.1 Normal quantization

First, a “normal quantization” were used, meaning quantization by rounding to the nearest quantization level. Simulation results are shown in figures below.

- Direct Digital Pulse Width Modulation for Class D Amplifiers -

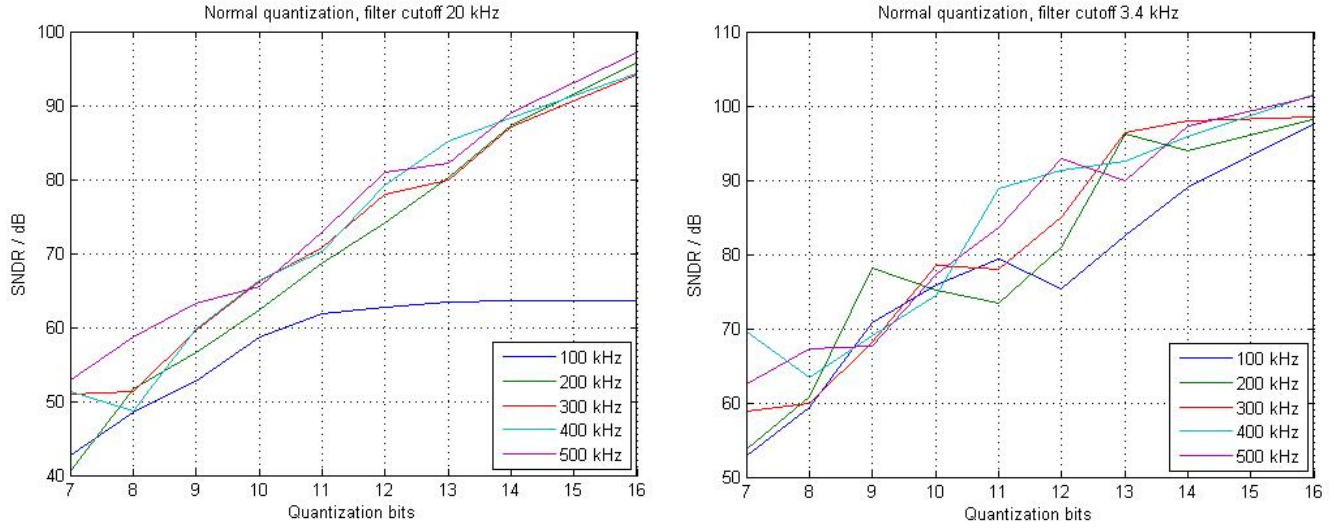


Figure 23. SNDR dependence of f_{pwm} and quantization levels.

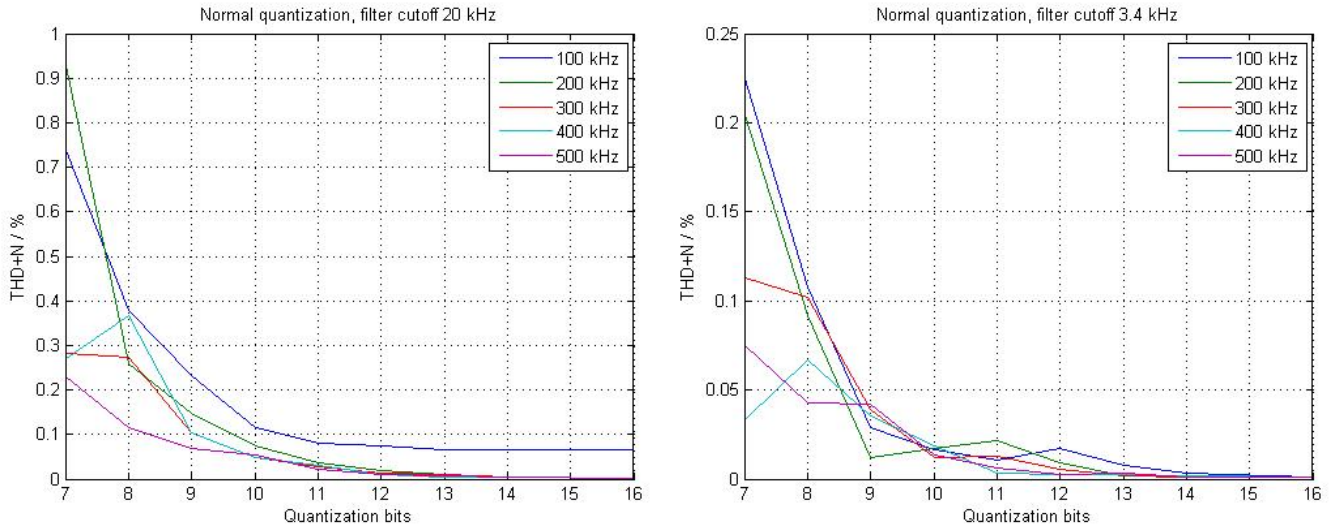


Figure 24. THD+N dependence of f_{pwm} and quantization levels.

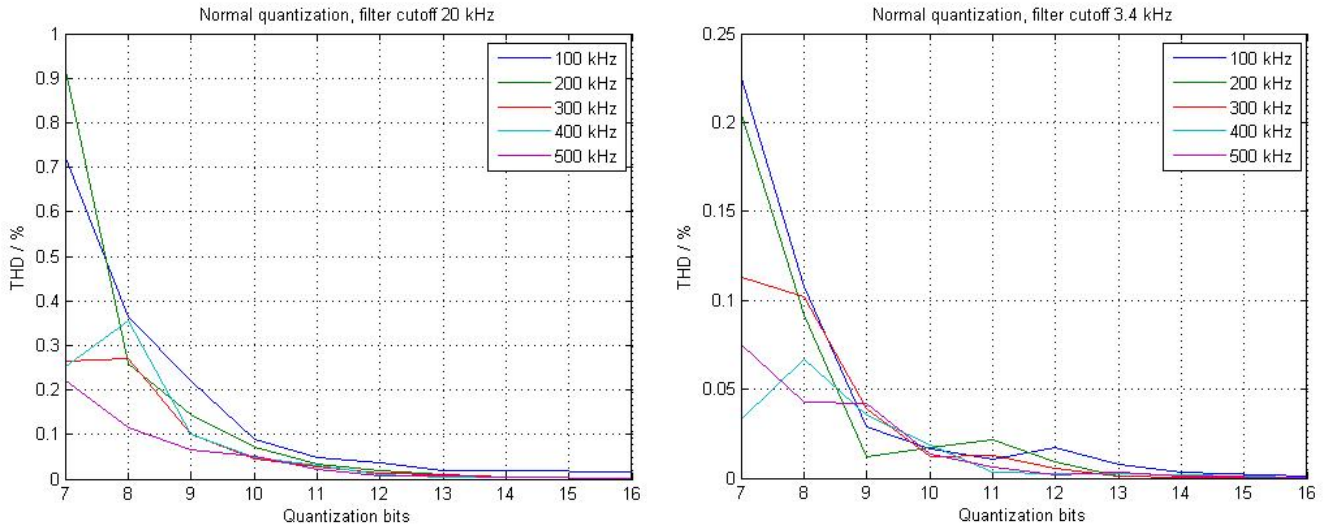


Figure 25. THD dependence of f_{pwm} and quantization levels.

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The simulation above shows that the SNDR depends heavily on the number of quantization levels. The higher the PWM sampling frequency the better SNDR is the general result but the non-linearity in the quantization causes some irregularities. In some way the quantization error is correlated with the input signal and the PWM frequency which causes more or less errors at certain frequencies. The expected dependency is the higher PWM frequency the better SNDR since the low-pass filter has better attenuation for higher frequencies, i.e. the carrier components will be attenuated more.

The two above figures gives a clear picture of that THD and THD+N are affected much when the quantization levels are increasing. This is depending on the quantization error. THD is affected much because the quantization error is showing up at frequencies correlated to the input frequency. The expected dependency of the PWM sampling frequency here is that if it is high it should be less THD and noise with the same reason as above.

An example of the output spectrum showing quantization error at certain frequencies is attached below.

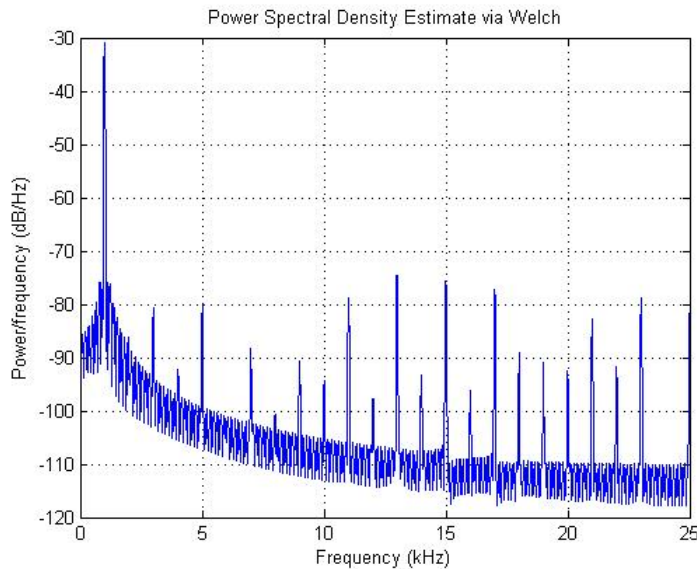


Figure 26. Output spectrum. 20 kHz cutoff, $f_{pwm} = 500$ kHz, normal 5-bit quant.

4.1.2 Quantization with dithering

To get rid of the correlation between the input frequency and the quantization error a small portion of noise of ± 0.25 LSB is added to the input of the quantizer. This is known as dither or dithering.

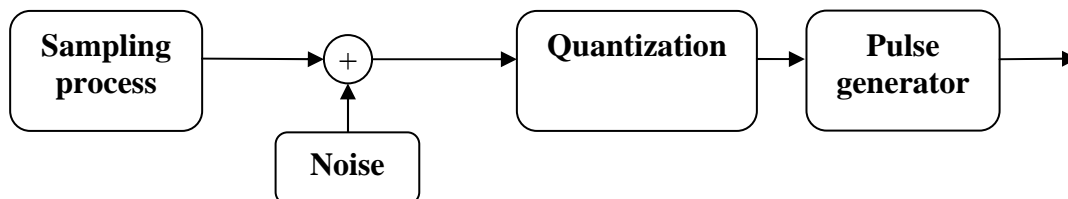


Figure 27. Simulation setup with dithering.

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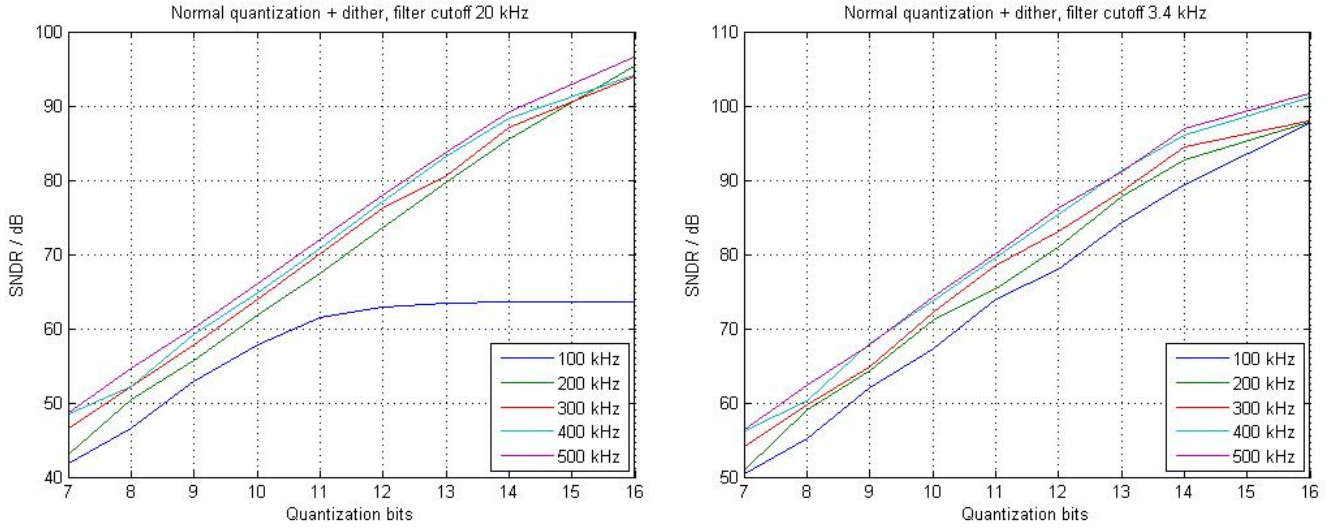


Figure 28. SNDR dependence of f_{pwm} and quantization levels.

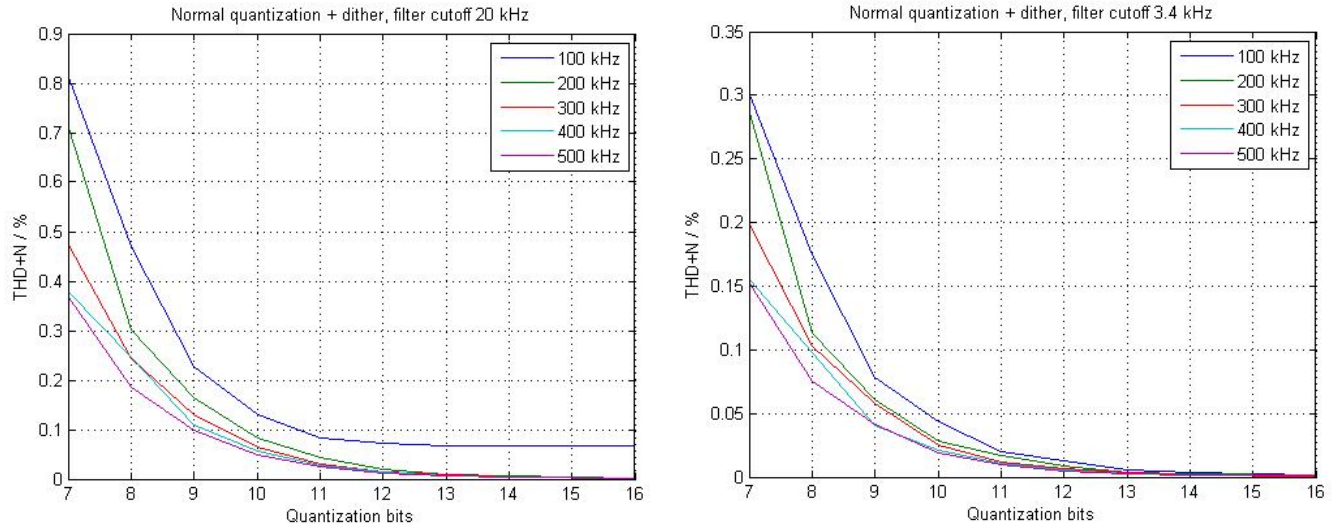


Figure 29. THD+N dependence of f_{pwm} and quantization levels.

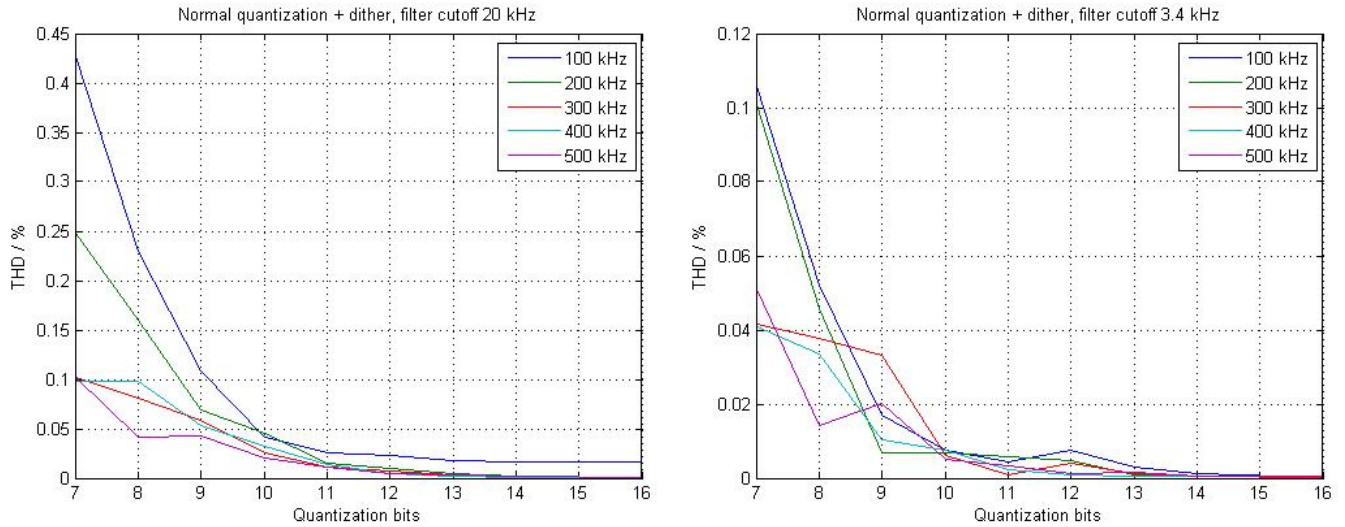


Figure 30. THD dependence of f_{pwm} and quantization levels.

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With dithering a more linear and expected result is achieved.

An example of the output spectrum showing quantization error acting more as noise is attached below.

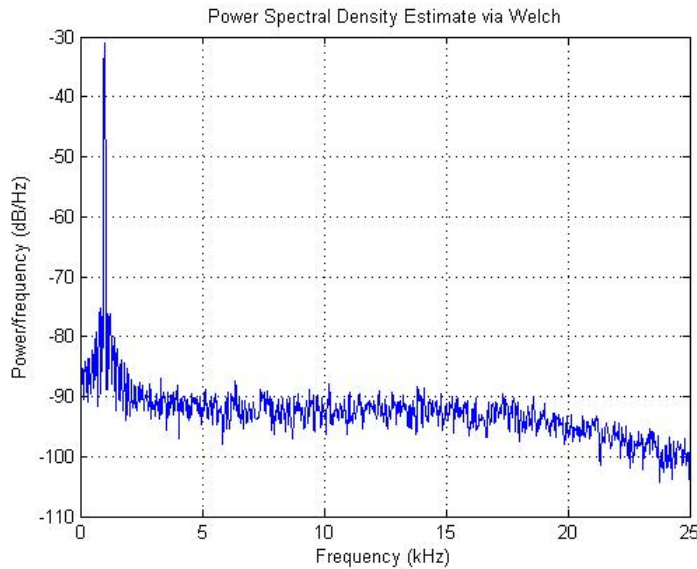


Figure 31. Output spectrum. 20 kHz cutoff, $f_{pwm} = 500$ kHz, normal 5-bit quant + dither.

4.1.3 Quantization with delta-sigma

By using delta-sigma for quantization it is possible to reach even better results regarding the signal quality. Delta-sigma shifts the quantization noise to higher frequencies. Below the results of the non-linear quantization are shown.

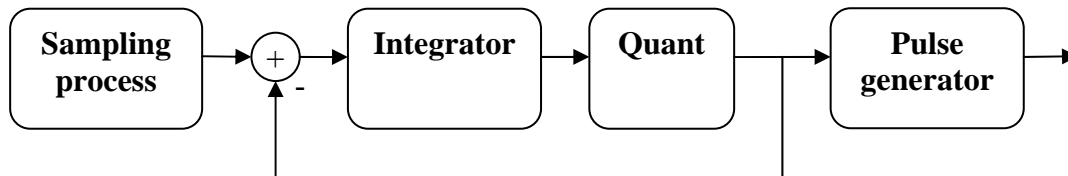


Figure 32. Simulation setup with delta-sigma (1st order).

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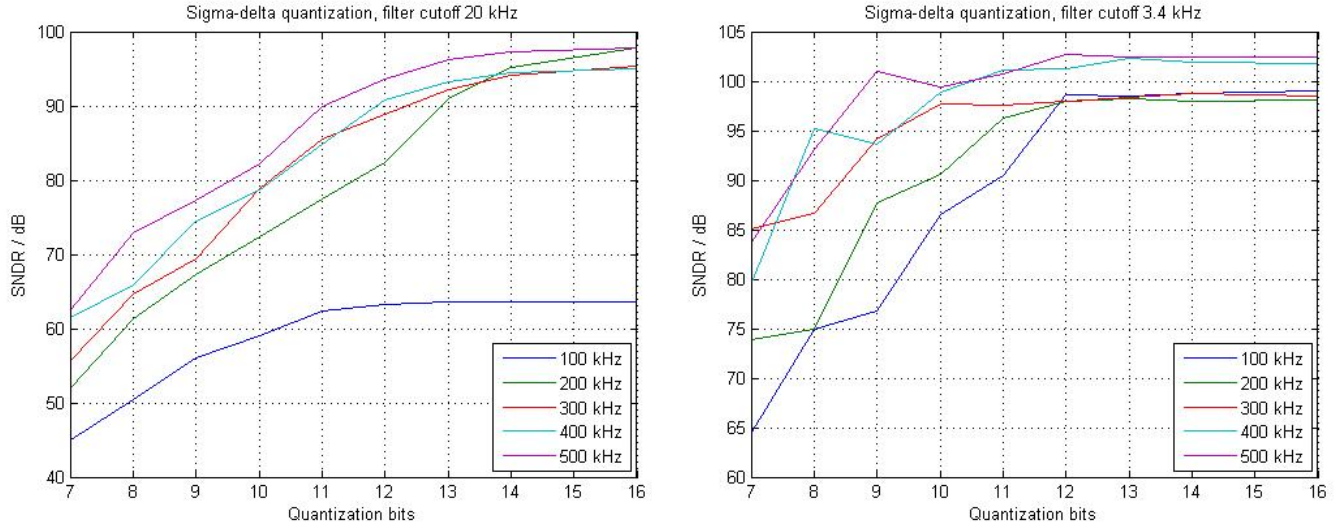


Figure 33. *SNDR dependence of f_{pwm} and quantization levels.*

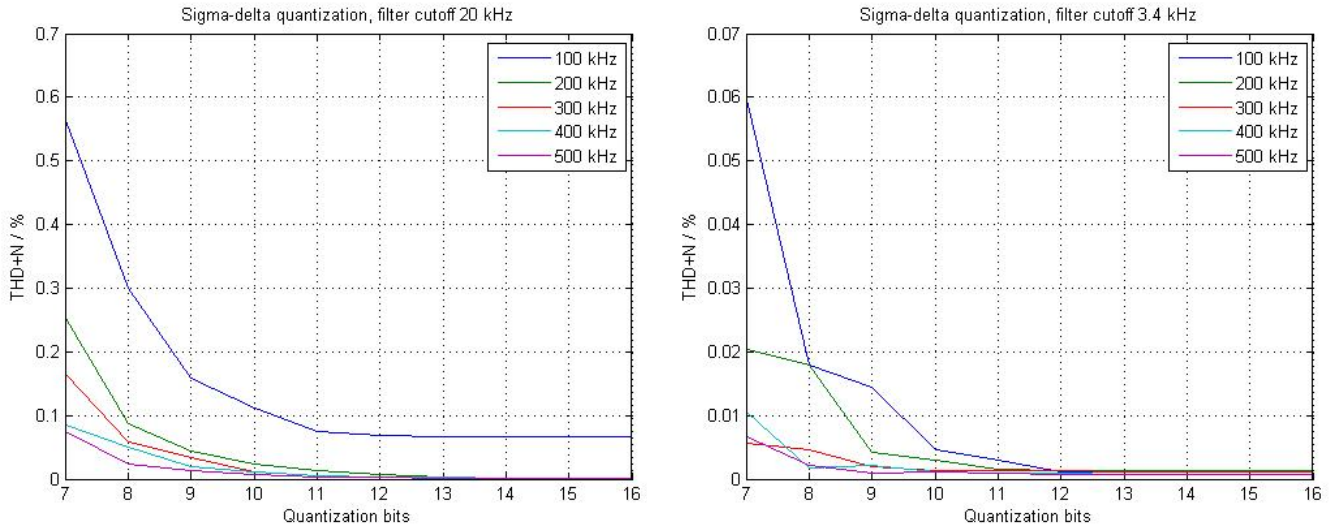


Figure 34. *THD+N dependence of f_{pwm} and quantization levels.*

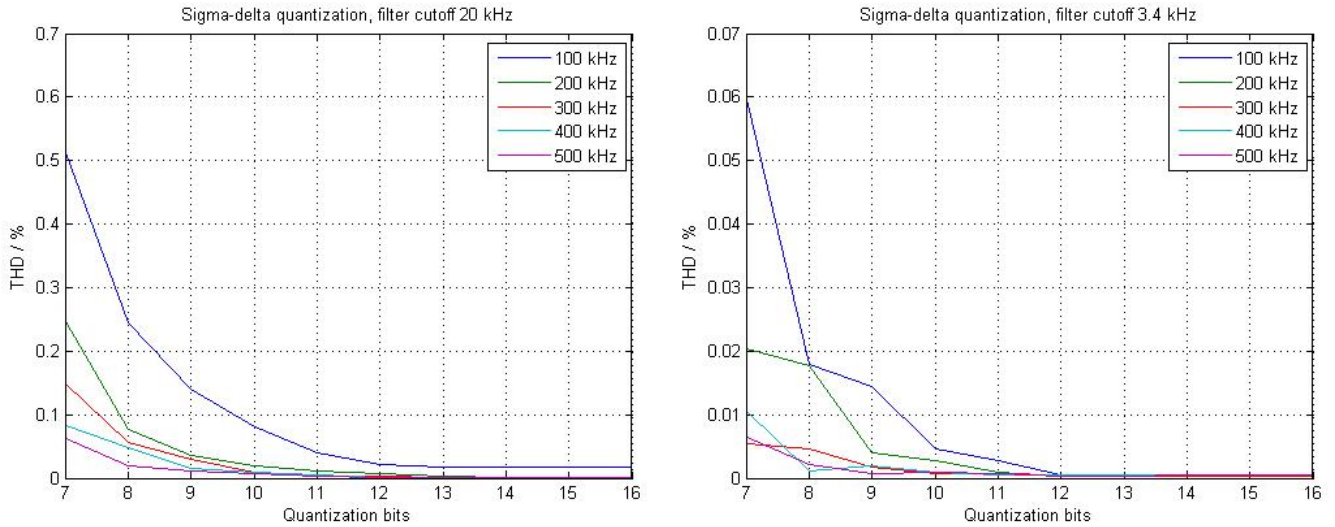


Figure 35. *THD dependence of f_{pwm} and quantization levels.*

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Delta-sigma quantization gives the overall best result but once again a non-linearity.

An example of the output spectrum showing quantization noise caused by the non-linearity is attached below.

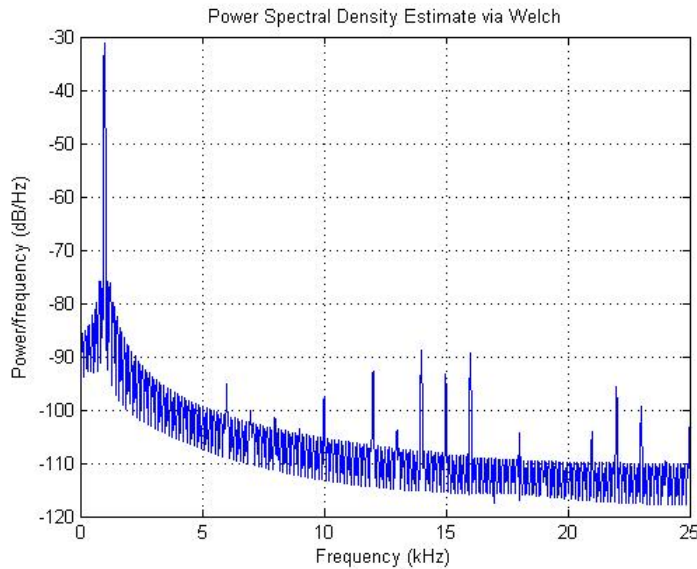


Figure 36. Output spectrum. 20 kHz cutoff, $f_{pwm} = 500$ kHz, delta-sigma 5-bit quant.

To be sure that the delta-sigma quantization gives a better result than normal quantization the sampling frequency (f_{pwm}) needs to be high enough. This is because delta-sigma shifts the noise to higher frequencies (lower than Nyquist frequency). A figure to illustrate this is attached below.

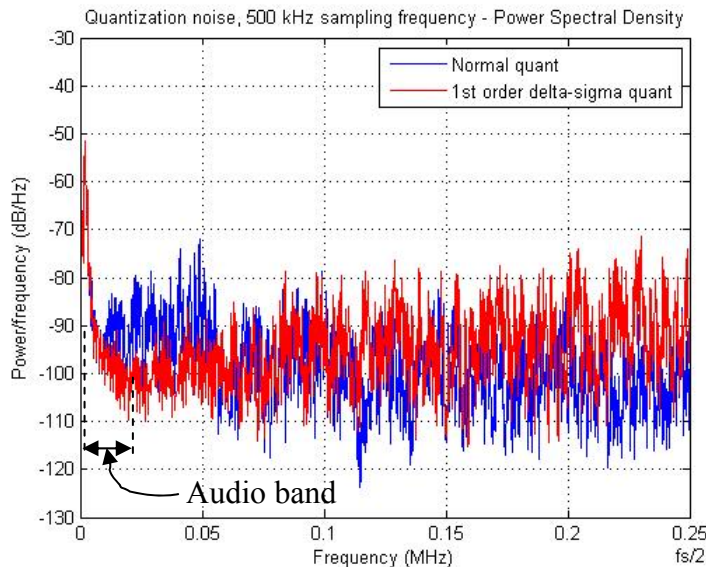


Figure 37. Quantization noise comparison. 500 kHz sampling frequency.

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Delta-sigma has lower noise in the audio band (20 Hz – 20 kHz) but this may not be the case if the sampling frequency is too low.

4.1.4 Summary of simulation results

A summary of the results from the simulations in Cocentric System Studio is presented in the table below.

Requirement	Quantization	Required bits at different f_{pwm} (kHz)				
		100	200	300	400	500
Voice	Normal	7	7	6	6	6
	Dither	7	7	6	6	6
	Delta-sigma	<6	<6	<6	<6	<6
Hi-fi	Normal	-	13	12	12	12
	Dither	-	13	12	12	12
	Delta-sigma	-	11	10	10	9

Table 1. Summary of simulations.

4.2 Two tone simulation

To investigate whether any intermodulation occurs due to any non-linearity apart from quantization a simulation with two sine signals were performed. The below figure shows the spectrum of a simulation with no quantization and a 500 kHz PWM frequency.

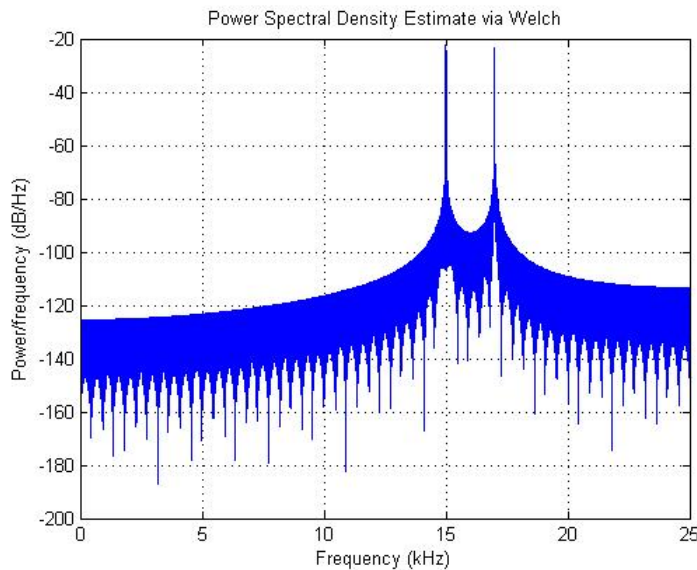


Figure 38. Two tones – 15 kHz and 17 kHz.

According to the above figure no intermodulation occurs so the combined pulse generator and low-pass filter are linear.

4.3 Delay error simulations

As mentioned earlier, variations in the CMOS process and environment will affect the delays in each delay element. This introduces a non-linearity (especially since the delay

elements can't be tuned in small steps). To keep a stable delay the delay elements need to be calibrated continuously. A simulation has been done to study how the SNDR, THD and THD+N vary with the amount of error in the delays. The error is generated from a pseudo-random source, based on the Mersenne Twister algorithm, with a uniformly distributed output. See figure below for simulation overview.

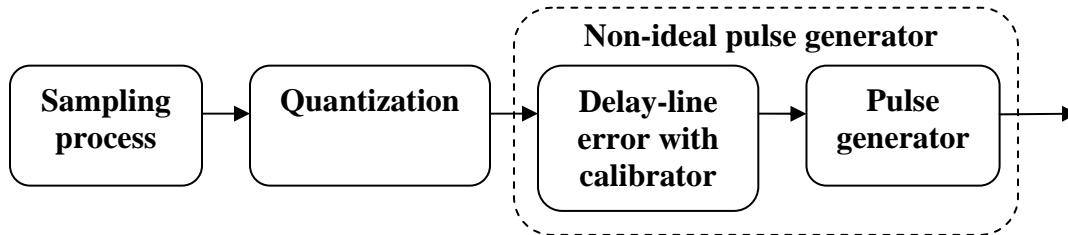


Figure 39. Simulation setup for modeling delay error.

Since a calibrator will be keeping the total delay-line delay to one clock cycle there is only error introduced in each delay-element while there will be no error when looking at the whole delay-line. This will cause different errors at different taps in the delay-line. The following setup was used.

- Input: $0.5\sin(2\pi 1000t)$
- Frequency span for calculations: $0 < f < 25$ kHz
- Pulse generator output sample frequency: 50 kHz
- Low-pass filter cutoff frequency: 20 kHz
- PWM frequency: 200 kHz
- Quantization bits: 12 (7-bit counter + 5-bit delay-line)
- Quantization: Normal
- Error in delay elements: 1-100 %

4.3.1 Simulation results

Simulation results are shown in the below figures. Since the added error is random, five simulations were made with the same setup and the maximum and minimum values from these are shown in the figures. Also the A-weighted versions are plotted. A-weighting is a filtration, where the energy at the low and high ends of the audio band is attenuated, to adapt to the human hearing.

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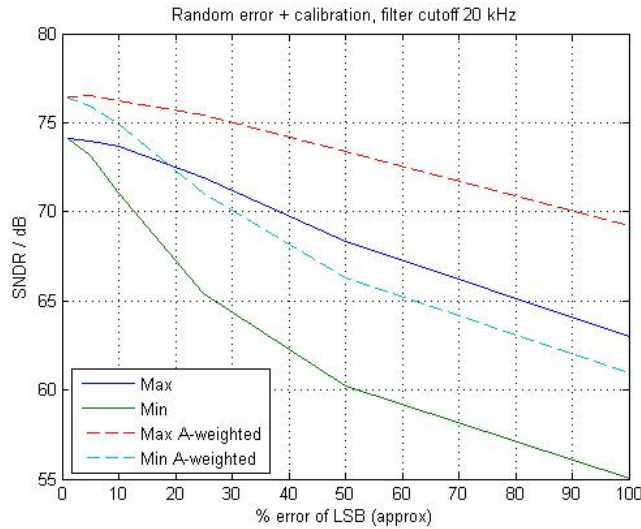


Figure 40. SNDR with different errors in delay element.

The addition of a random error in each delay element affects the SNDR heavily. If the error in the delay elements goes up to 100 % and a five bit delay-line is used we can get up to about a 20 dB deterioration of the SNDR. By using A-weighting we get a more fair result.

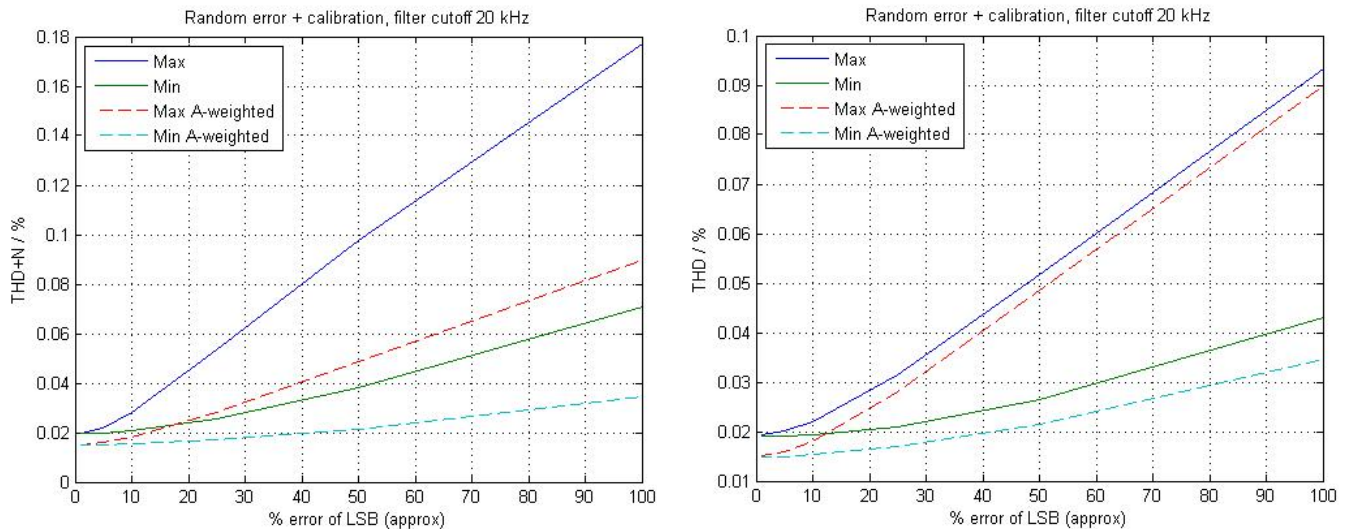


Figure 41. THD+N and THD with different errors in delay element.

The above simulation results show that the quality of the signal is heavily affected by the random errors. It is going to be really hard to meet up with the hi-fi requirements since the above setup can nearly not tolerate any error at all to reach the required 76 dB SNDR. A 300 kHz PWM frequency, delta-sigma quantization and less quantization would probably give enough SNDR to be able to tolerate some error. THD is obviously no problem so it is probably a good idea to raise the PWM frequency to shift the high frequency components away even more from the audio band. This will lead to less bits to handle in the pulse generator, i.e. less accurate, and therefore higher THD but better SNDR.

5 Schematic / HDL design and simulation

5.1 Delay element

To find out how much the delay is affected by variations in temperature, supply voltage and process a simulation was done in Cadence with the schematics shown below (representing a series of delay elements, i.e. a delay-line, with the shortest chain of inverters active, delay of multiplexer not included).

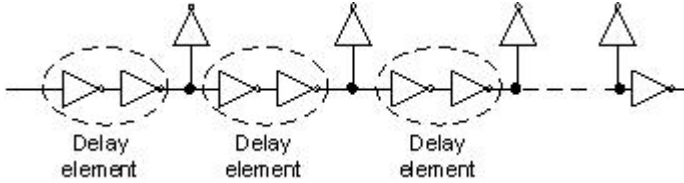


Figure 42. Simple delay-line with inverters simulated in Cadence/spectre.

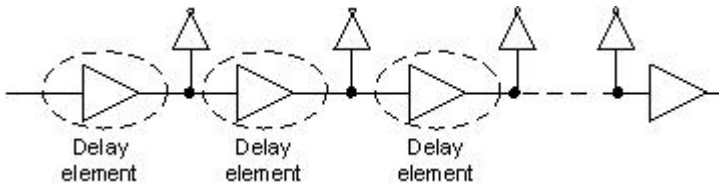


Figure 43. Simple delay-line with buffers simulated in Cadence/spectre.

By simulating these circuits we are able to find the worst case delay that limits the quantization resolution. The simulation was done with the two above setups. One with minimum sized CMOS inverters and the other one with a minimum sized buffer. Minimum sized inverters were used at each tap in both setups. All these components were taken from a standard cell library (high V_t). The delay-lines were simulated with seven taps/outputs. Results from the simulations in the fastest, slowest and standard corners are shown in the tables below. The extremes are shown in grey.

V_{DD} (V)	Temp (°C)	Delay (ps)			
		Only inverters		Buffers and inverters	
		Rising	Falling	Rising	Falling
1,35	-40	56	51	56	54
	27	60	55	60	59
	100	63	59	63	63
1,5	-40	46	43	46	46
	27	50	47	51	50
	100	54	50	54	53
1,65	-40	40	38	40	40
	27	44	41	44	44
	100	47	44	47	47

Table 2. Delay of pulse through a delay element. Standard corner.

V_{DD} (V)	Temp (°C)	Delay (ps)			
		Only inverters		Buffers and inverters	
		Rising	Falling	Rising	Falling
1,35	-40	80	74	82	79
	27	88	81	89	87
	100	94	88	96	94
1,5	-40	65	60	66	64
	27	73	67	73	72
	100	78	73	80	78
1,65	-40	55	52	56	55
	27	61	58	63	61
	100	67	63	69	67

Table 3. Delay of pulse through a delay element. Slowest corner.

V_{DD} (V)	Temp (°C)	Delay (ps)			
		Only inverters		Buffers and inverters	
		Rising	Falling	Rising	Falling
1,35	-40	41	38	41	40
	27	44	41	44	43
	100	46	43	46	46
1,5	-40	35	32	35	34
	27	38	35	38	37
	100	40	38	40	40
1,65	-40	31	29	31	30
	27	33	31	33	33
	100	36	34	36	35

Table 4. Delay of pulse through a delay element. Fastest corner.

As the tables show, the delay varies between 29 and 96 ps and under normal conditions we should have a delay of about 50 ps. The design with buffers and inverters gives a result where the rising and falling edge of the test pulse are delayed more similarly.

The biggest problem with the design of the variable delay element is that the aim is to get as short delay as possible. This results in big delay steps within the delay element. So the above solution would only be able to produce a few different delays in each element where for example one buffer is active for slow conditions, two buffers active for normal conditions and three for fast conditions thus giving quite a large error in a single element when the condition is somewhere between slow and normal or normal and fast. The total error through the whole delay-line, or to a certain tap, can however be minimized by using a good calibration algorithm.

5.1.1 Design choice

To be able to use standard cells the below delay element design is proposed and used as base for further design.

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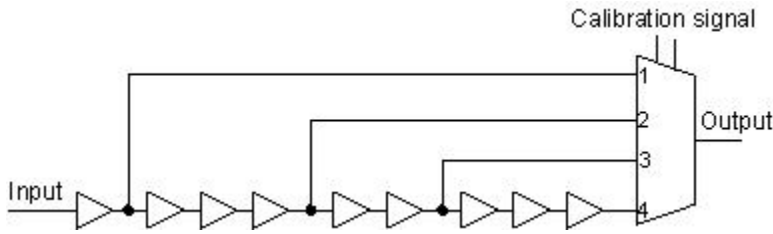


Figure 44. Delay element 1.1. Chosen delay element design. Nine minimum sized buffers and a four- input multiplexer.

The delay of the required four-input multiplexer affects the delay really much. To reduce the delay the transistors used in the cells were replaced with regular V_t . In the table below the possible delays of the proposed delay element is presented.

Chain	Corner	V_{DD} (V)	Temp (°C)	Possible delays (ps)	
				Rising	Falling
1	Slowest	1,35	100	213	242
	Nominal	1,5	27	112	124
	Fastest	1,65	-40	68	72
2	Slowest	1,35	100	389	423
	Nominal	1,5	27	209	223
	Fastest	1,65	-40	128	134
3	Slowest	1,35	100	512	554
	Nominal	1,5	27	276	293
	Fastest	1,65	-40	170	177
4	Slowest	1,35	100	680	730
	Nominal	1,5	27	366	387
	Fastest	1,65	-40	226	234

75 % diff

Table 5. Possible delays through delay element.

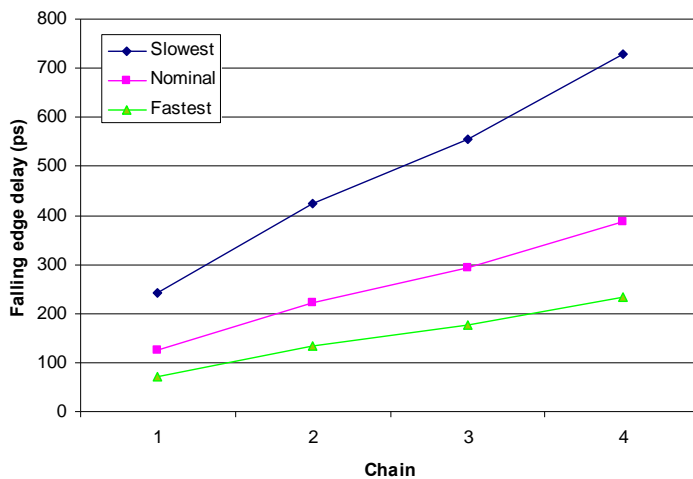


Figure 45. Possible delays of falling edge in different chains and corners.

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We see that the largest error that can occur in one element, when the calibration unit change chain, is about 75 %. To see how process differences in each transistor could affect the delay in each element a Monte Carlo simulation was performed and the result is that we can expect up to about ± 10 % delay change. With this included the largest error can be up to 100 % in a delay element.

The worst case is 240 ps delay so each element should roughly have this delay. Depending on temperature, supply voltage and process the calibration unit will choose the appropriate chain in each element to obtain a total delay of one clock cycle. The maximum number of bits in the two different parts in the hybrid pulse generator are shown below, based on the element delay of 240 ps and $f_{pwm} = 200$ kHz.

f_{clk} (MHz)	T_{clk} (ns)	Delay-line		Counter		total bits
		fractions of T_{clk}	max bits	max value	max bits	
10	100,0	416,7	8	50	5	13
40	25,0	104,2	6	200	7	13
104	9,6	40,1	5	520	9	14
312	3,2	13,4	3	1560	10	13

Table 6. Number of bits each part can handle in the hybrid pulse generator.

Putting these values back into our delta-sigma model (figure 39), where the counter based part always have maximum bits, we find the following requirements. Based on five simulations with the worst case of the five random error simulations is displayed below.

Mode	f_{clk} (MHz)	Delay-line bits	Counter bits	Total bits	Max delay error allowed
Voice $f_{pwm} = 200$ kHz	10	7	5	12	400%
	40	5	7	12	>400%
	104	3	9	12	>400%
	312	2	10	12	>400%
Hi-fi $f_{pwm} = 200$ kHz	10	8	5	13	20%
	40	6	7	13	28%
	104	5	9	14	20%
	312	3	10	13	85%

Table 7. Maximum error in delay elements with different setups. Signal A-weighted.

The voice mode requirements are fulfilled if the error in the delay elements could be kept below 400 %. The hi-fi mode requirements can be fulfilled even though not all the 16 bits are used if it is possible to keep the error low. It is good to have a large margin to the requirements since other parts of the amplifier also will add noise and distortion.

5.2 System specifications

Based on the above delay element design the following system specifications are chosen as a test to very generously fulfill the voice mode requirements:

- $f_{\text{pwm}} = 203.125 \text{ kHz}$, to keep the carrier at a safe distance from the input and still keep the switching rate at a reasonable level.
- $f_{\text{clk1}} = 26 \text{ MHz}$
 - 7-bit counter
 - 5-bit delay-line
- $f_{\text{clk2}} = 104 \text{ MHz}$
 - 9-bit counter
 - 3-bit delay-line

Two different system clocks are used to be able to compare two designs at a lower level than the earlier simulations. To get full swing on the output it is important to remember that $T_{\text{pwm}} = 2^{(\text{counter bits})} T_{\text{clk}}$ should be fulfilled. A total of 12 bits is used in the system even though 7 bits should be enough to fulfill the voice requirements ideally (as shown in part 4.1.4).

The hi-fi requirements are harder to fulfill but it is possible to meet up with them. More work must be put on designing the delay-line and error correction in the following output stage and filter. However will the results from the above design show if the concept works or not and give hints about how the hi-fi results should come out.

5.3 Pulse generator

An overview of the hybrid pulse generator is shown below.

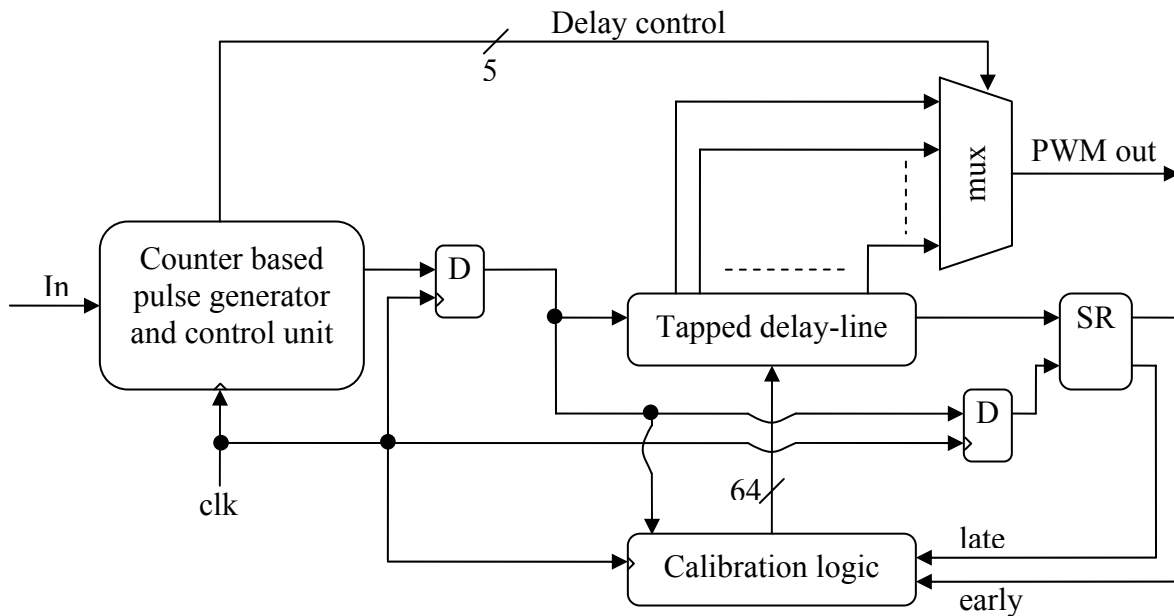


Figure 46. Overview of pulse generator.

The input to the above system is, as mentioned earlier, 12-bits of data from a natural sampled sine wave which arrives uniformly according to f_{pwm} . The counter handles the most significant bits and produces a pulse where the rising edge is fed through tap 1 and the falling edge is delayed by the delay-line by choosing the appropriate delay/tap with the control signal. How much to delay the falling edge is decided by the least significant bits of the input which control the multiplexer at the output. The result is a PWM signal with a resolution according to the input, i.e. 12 bits. See appendix B for schematics and verilog code.

5.3.1 Delay-lines

To be able to use the same calibrator both delay-lines are based upon a 5-bit structure. A 5-bit delay-line requires 32 delay elements.

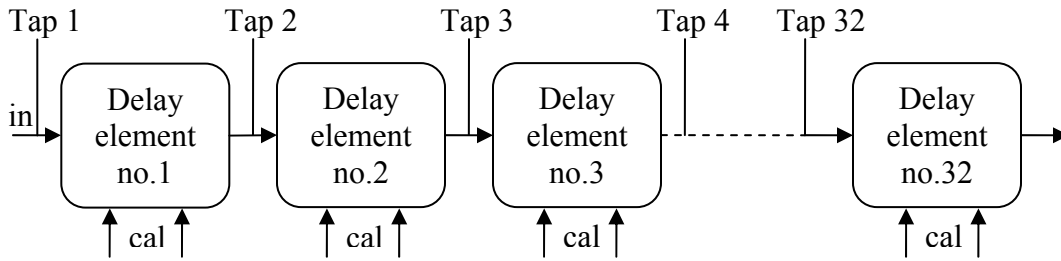


Figure 47. 5-bit delay-line used in design.

The difference between the delay-lines is that in the 104 MHz version the 5-bit delay control signal from the control unit is composing of $x_3x_2x_100$ where $x_3x_2x_1$ are the three least significant bits of the input sample. Since the delay-lines are based upon the same structure it is not possible to use the same delay-element. When a lower system clock is used more delay is needed per element to achieve a total delay of one clock cycle. To increase the delay in each element for the 26 MHz case a new element was constructed by arranging five elements in series thus giving rougher tuning of the delay through the element since all five elements in series get the same calibration signal.

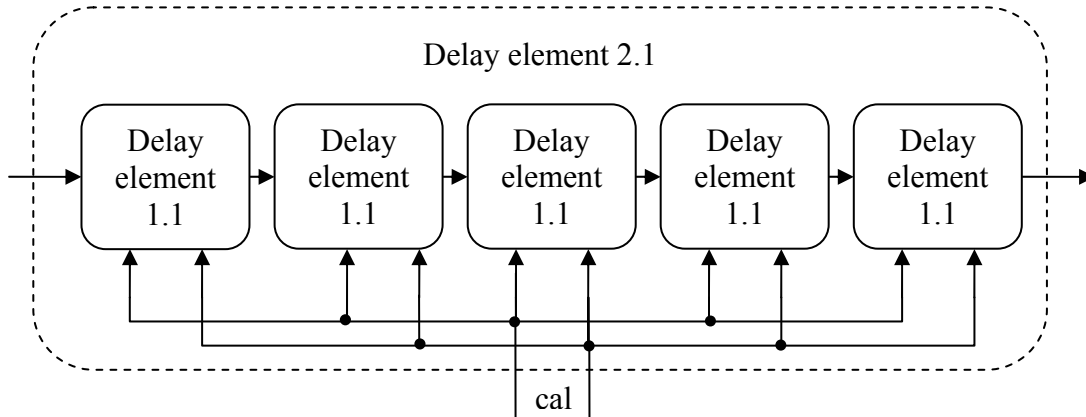
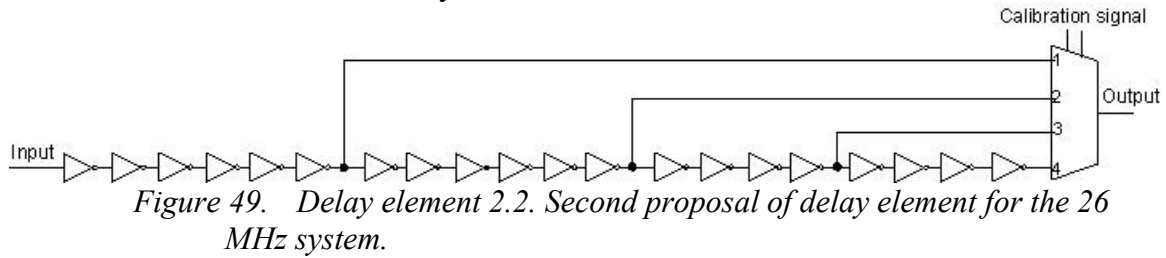


Figure 48. Delay element 2.1 (26 MHz system). Five of delay element 1.1 in series.

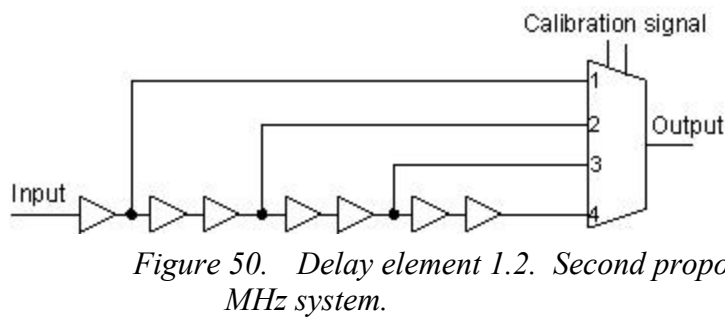
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The below structure was also tried out. It is similar to the 104 MHz design but it uses more inverters which differ widely in size.



The delay of delay element 2.1 and 2.2 are the same.

To have something to compare to for delay element 1.1 the following design was used.



The delay of delay element 1.1 and 1.2 are the same. It uses fewer buffers than delay element 1.1 but they are not minimum sized anymore.

As seen in the design of the delay elements it would be possible to use a larger multiplexer and/or calibration circuit to be able to get a finer delay adjustment. Every extra bit in the calibration signal would double the amount of possible delays.

5.3.2 Calibration method

Since each delay element has four different delays they need to be controlled by two bits. This means a total of 64 bits to control the whole delay-line with. The method to calibrate is simply to increase the delay one step at the time if the delay is too small and vice versa. Which element, of the 32 available, to change was calculated in Matlab by choosing the one that minimizes the maximum error in the taps, based on normal process and environmental conditions. See appendix C for Matlab code.

The principle for which element to calibrate is shown below.

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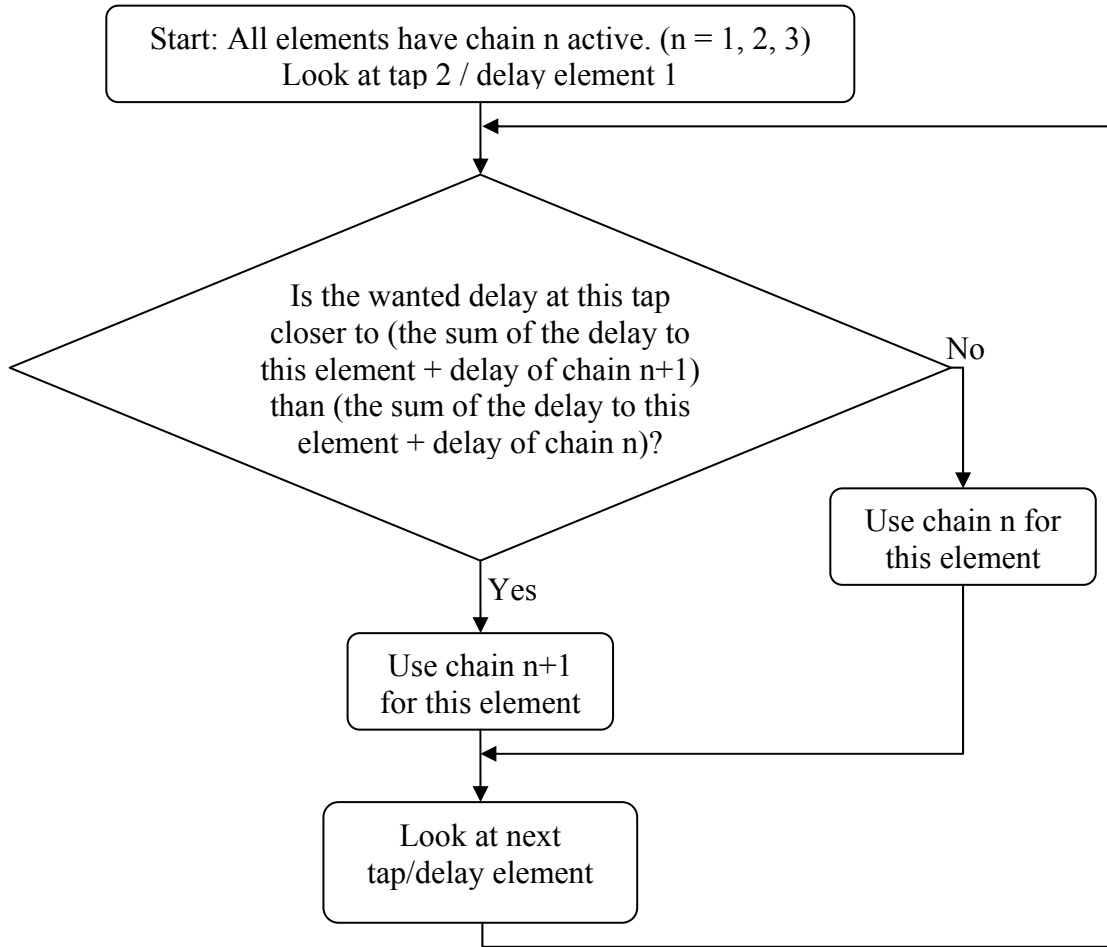


Figure 51. Flowchart showing calibration method.

An example of the delay error at each tap, at nominal conditions, using three of the proposed elements with chain 2 active and 29 with chain 3 active is shown in the figure below.

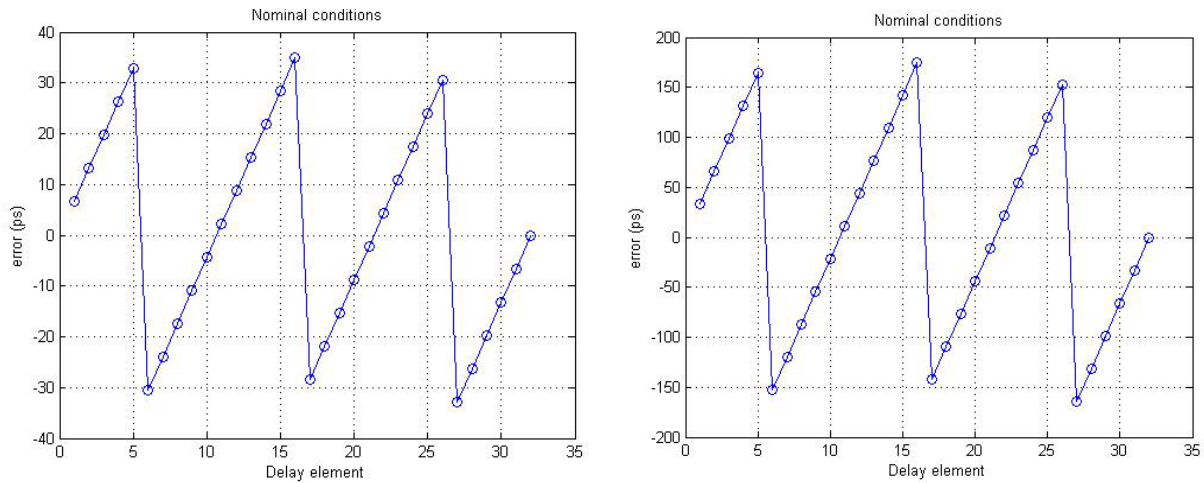


Figure 52. Error at tap 1 – 32 using 3 elements with chain 2 and rest with chain 3. 104 MHz case and 26 MHz case respectively.

This calibration block was programmed in Verilog and the code is presented in appendix B.

5.3.3 Simulation results

To evaluate the calibration method, and the whole pulse generator at this stage, simulations in spectreVerilog were preformed. The input to the pulse generator was a 12-bit, normal quantization, natural sampled 1 kHz sinus signal with an amplitude of 0.5. As this simulation was very time consuming the whole system had to be realized in Verilog, including the delay elements, to speed up the simulation. This should not affect the result much since the possible delays of the delay element is known from earlier simulations.

A fifth order passive Butterworth low-pass filter with a gain of 0.5 and cutoff frequency at 20 kHz was applied at the output to demodulate the PWM-signal. The result is shown below.

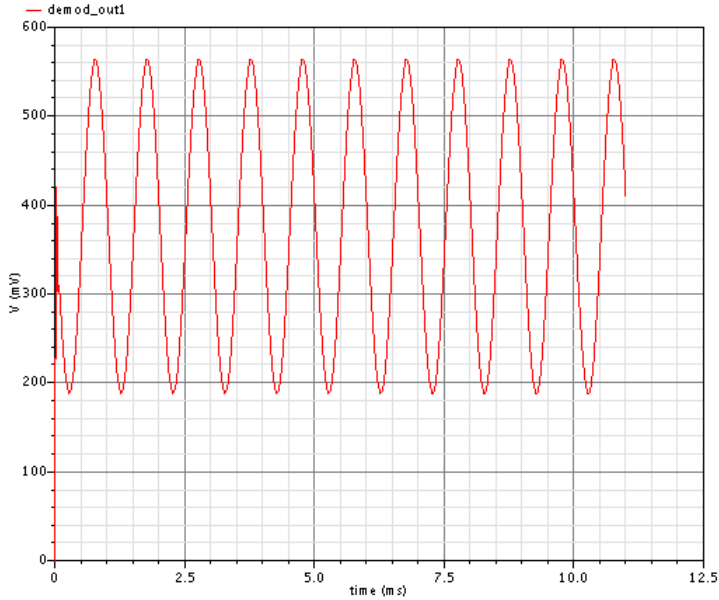


Figure 53. Demodulated output. 1 kHz sine wave.

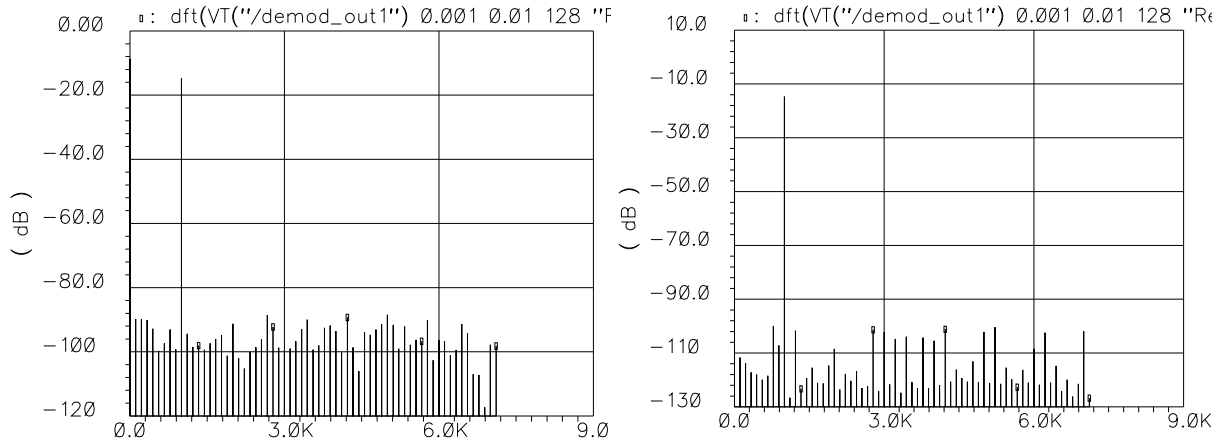


Figure 54. Spectrum of output of the 26 MHz and 104 MHz system.

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The THD calculations of the output signal between 1 ms and 10 ms resulted in approximate 0.07 % (<32 kHz) for the system with 26 MHz clock and approximate 0.02 % for the 104 MHz system. The above result is quite close to the earlier ideal simulations so the calibrator works fine. It is expected to get more harmonics for the 26 MHz system since it uses more bits in the delay-line than the 104 MHz case. By looking at the spectrums it is possible to observe an approximate SNDR of 70 dB in the 26 MHz case and about 80 dB in the 104 MHz case.

The calibrator locks to the preferable delay after less than 50 clock cycles (if it starts at the middle value) and this means that it is locked fast, way before 1 ms which was the start of the THD calculations above. See figure below for simulation result of calibration where the calibrator starts at zero.

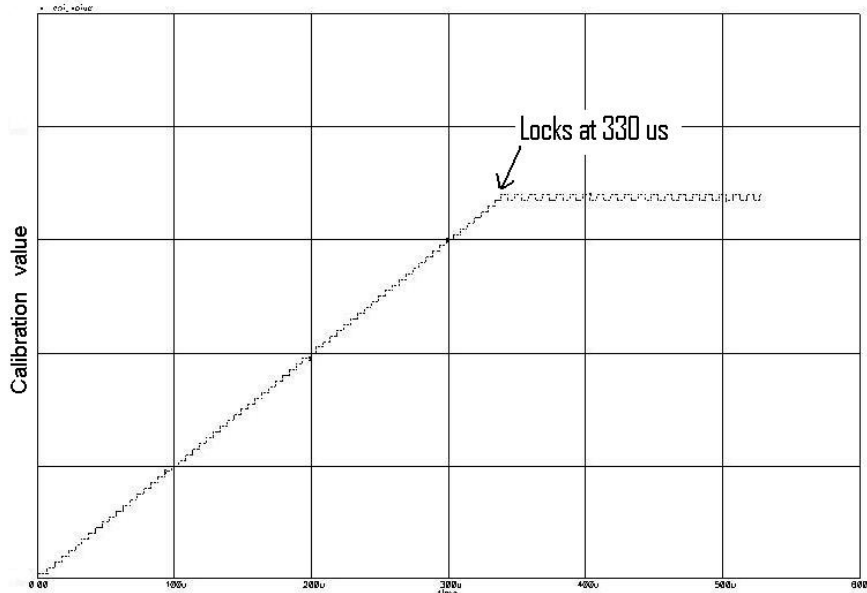


Figure 55. Calibration value for delay-line. Locks after 330 μ s (starts at zero).

The calibrator will alternate between the two calibration signals that gives the delays of the whole delay-line as close to one clock cycle as possible. This means a possible error of up to 100 % of the LSB in the whole delay-line.

6 HDL synthesis and power consumption simulation

As the calibrator and the counter/control are pure digital blocks, described in Verilog, Synopsys Design Compiler was used to perform logic synthesis. The resulting logic was mapped to standard cells used within Infineon and netlists were generated. After importing the netlists into schematic views in Cadence it was possible to simulate power consumption of the two systems. Simulation of system functionality is, as mentioned earlier, very time consuming so this simulation was short but long enough to study the power dissipation. The result is shown below.

f_{clk} (MHz)	Delay element	I_{avg} delay-line active (μA)	I_{avg} digital (μA)	I_{avg} tot (μA)	V_{DD} (V)	Power (μW)	Total cell area (mm^2)
26	2.1	2700 for 38 ns	41	58	1.5	87	0.025
26	2.2	920 for 38 ns	41	54	1.5	81	0.021
104	1.1	278 for 9.6 ns	164	166	1.5	249	0.014
104	1.2	775 for 9.6 ns	164	168	1.5	252	0.014

Table 8. Simulated power dissipation of pulse generator.

The average dynamic (switching) power consumption in CMOS logic circuits is $P = CV^2fa$ where a refers to the switching activity (0 -> 1). As the simulation results show the higher frequency system has about three times higher power consumption. The reason for not being four times higher ($104/26 = 4$) is that more transitions are made within the delay-line in the 26 MHz system since it consists of more buffers. Another conclusion to draw regarding power consumption is that the pulse generator will not affect the total efficiency of the class D amplifier much. A reasonable output power of an amplifier to be used as a speaker phone is about 500 mW and the pulse generator systems dissipates approximate 0.02 % or 0.05 % of that value in comparison.

An example of the system current is shown below.

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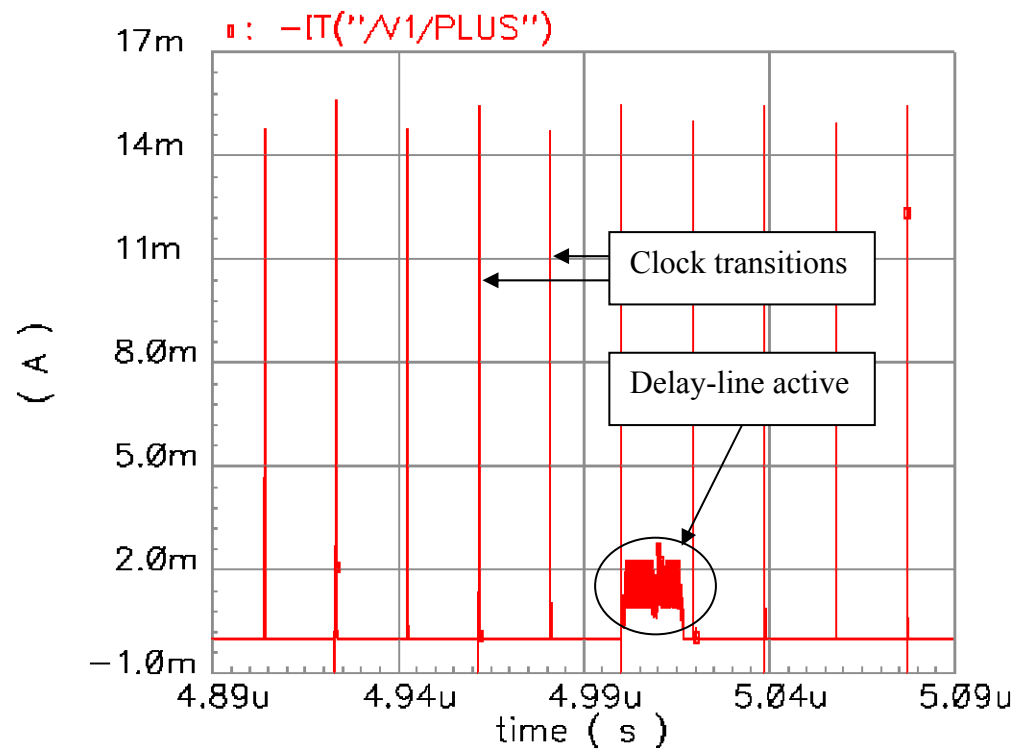


Figure 56. Example of total system current.

7 Discussion

Even though the work from this report shows good results it is only a part of the whole class D amplifier. Of course it is possible to enhance the signal path quality of the above work even more by for example designing delay elements with smaller delay steps but with the consequence of larger area, higher power dissipation or complexity. According to [28] the distortion introduced in the pulse generator is generally smaller compared to that of the output stage.

The non-idealities of the output stage such as ringing, dead-time and finite switching times will affect the quality of the output signal severely. Since the open-loop structure causes zero PSRR, the amplifier will also be very sensitive to power supply perturbations. The question is if it is worth it to put effort on a really good regulated power supply, gate-driver circuitry or other solutions like a feed-forward where one for example may sense the power supply voltage and compensate by changing the timing of the pulses. This would require considerable design effort, and the conclusion may in any case be that it is cheaper and better to use the “classical” analog pulse generation with feedback. This depends to a great extent on the other constraints on the system; for example, what power supply is available. The main drawback of the analog approach is that it requires an analog input signal: where the signal to be amplified only exists in digital form, an additional DAC is required. Also, it becomes cheaper to design digital parts as the process technologies are getting smaller while the analog parts, on the contrary, are getting more expensive because they scale relatively poorly compared to the digital parts. The trend towards system on chip integration of both digital and analog blocks makes it easier to implement relatively complex digital calibration of analog components at rather low cost.

Furthermore as the output low-pass filter is sensitive to load variations the signal transfer and output impedance will be affected when connecting it to a complex impedance of a speaker. This can be solved by a quite complex feedback after the filter but since we have open-loop this will affect the signal quality. An alternative is to use a higher cut-off frequency than the actual frequency band that is used. The sensitivity to load variations will be lower but at the expense of lower attenuation of the high frequencies and therefore more EMI and noise/distortion. Depending on what kind of application the class D amplifier is used in, it may be possible to compensate for the frequency response of the speaker. In products like a speaker phone where a fixed built-in speaker is used the speaker impedance could be measured and compensated for by applying some digital filtering of the input samples.

So if you are about to design an amplifier and the input is a digital sampled signal; what is the best choice: the open-loop digital solution or the solution with a DAC and analog generated PWM with feedback? In the “audiophile” hi-fi-world the answer is analog class D with feedback, at least according to one of the most respected class D designers Bruno Putzeys who puts it: “digital class D: dead end street; analog class D: definitely the future” [26]. But when there is no need for super hi-fi-quality the open-loop digital design is an alternative. Manufacturers like Texas Instruments provide what they call “True Digital Audio Amplifiers” (TDAA) (open-loop, digital), for which there is clearly

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a big market, but it is unusual to see THD lower than 0.1 %. However it is hard to evaluate an amplifier when just looking at the SNR and THD specifications. Tube amplifiers with THD of 1-3 % may be hi-fi for “audiophiles” but not a transistor based amplifier with lower THD.

As further work, it would be interesting to, in the high-level simulations, simulate for example delta-sigma together with dithering or simulate higher orders of delta-sigma quantization. It would also be desirable to back-annotate the measured delays from the simulations of the delay elements back into the Cocentric System Studio simulations, and also to perform listening tests of the results. More than five random simulations of the delay error model should probably be performed to guarantee a correct result. It may also make sense to use a second order Butterworth filter in the simulations, since it is a very common demodulation filter.

It would also be very interesting to complete the design of the whole system, by adding output stage and a sampling process to drive the pulse generator. If a layout of the whole system was done, it would then be possible to fabricate a test chip and measure and listen to how it really sounds. In such a case, pre-compensation techniques or other methods to increase the PSRR and reduce distortion would also be interesting areas to look into.

8 Conclusions

When designing a direct digital pulse width modulator based on the principle described in this report there are several important things to consider:

- **Sampling process:** To avoid nonlinearities the sampling process should be as close to natural sampling as possible.
- **Switching frequency:** The switching frequency needs to be high enough to be able to fulfill the Nyquist sampling criterion and high enough for a simple low-pass filter to attenuate the high-frequency components. To be able to have a high efficiency amplifier the switching frequency must not be too high. Frequencies between 200 kHz and 500 kHz are common.
- **Quantization:** The number of bits a digital pulse generator can handle is important for the signal quality. In low-power circuits a good solution is to use a self-calibrating delay-line to be able to achieve higher resolution of the pulses than a clock cycle. With this in combination with delta-sigma it is possible to get really low distortion and noise.
- **Delay-line design:** Based on the system clock frequency, switching frequency and quantization the number of bits required in the delay-line can be decided. One simple design of the controllable delay elements is to use different chains of buffers to delay the input where the chains are connected to a multiplexer. Area and power consumption decides how accurate delay elements to design.
- **Calibration:** By using calibration of the delay-line one can prevent errors occurring from environmental changes and process variations. The errors left after calibration at each tap are minimized by calibrating the right elements.

A direct digital modulation suits low cost, low area and non “audiophile” hi-fi systems. If higher fidelity is required it is probably a better choice to use an analog system with feedback. Since the work presented in this report is focused on small battery driven devices the open-loop digital approach is a good choice. This is primarily because the digital parts scale down with technology and will therefore not be limiting the design of future systems based on smaller process technologies. The quality of the produced output audio signal would probably qualify for the requirements of today’s portable hi-fi audio devices but as always, you can’t say anything before you’ve listened to it.

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Appendix A – Cocentric System Studio code

Sampling process

```
// Sample Generator for digital PWM

// This model generates samples (natural sampling) from two sine signals
// The value of the out samples corresponds to the duty ratio of the pwm pulse
// 0 < OutData(k) < 1

// (C) 2006: Infineon
//
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// prohibited without the prior written consent of the copyright owner.

prim_model PWM_sample_gen
{
    // Output signal data type.
    type_param T1 = double;
    // Data type.
    type_param T2 = int;
    // Amplitude of the first sine signal.
    param dynamic T1 A1 = 0.5;
    // Frequency of the first sine signal
    param dynamic T2 F1 = 1000;
    // Amplitude of the second sine signal.
    param dynamic T1 A2 = 0.5;
    // Frequency of the second sine signal
    param dynamic T2 F2 = 2500;
    // Start time of sawtooth signal.
    param read_on_reset double t_start = 0.0;
    // Constant 2*pi.
    param const double C_2PI = 8.0*atan(1.0);
    // Output samples
    port out T1 OutData;

    // PWM frequency
    param dynamic T2 f_pwm = 100e3;

    // Phase of two sinus
    double p1,p2;

    main_action
    {
        double p1_left, p2_left;
        double p1_right, p2_right;
        double t_left, t_right;
        t_left = 0;
        t_right = 1.0/f_pwm;
        p1_left = p1;
        p2_left = p2;

        // Phases at start of next cycle
        // pX_right needs to be greater than pX_left
        p1 = p1 + C_2PI*F1*(1.0/f_pwm);
        p1_right = p1;
```

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```

p1 = (p1 > (C_2PI/2)) ? (p1 -= C_2PI) : p1;
p1 = (p1 < (C_2PI/2)) ? (p1 += C_2PI) : p1;
p2 = p2 + C_2PI * F2 * (1.0 / f_pwm);
p2_right = p2;
p2 = (p2 > (C_2PI/2)) ? (p2 -= C_2PI) : p2;
p2 = (p2 < (C_2PI/2)) ? (p2 += C_2PI) : p2;

double t_tol = 1.0 / 1e12; // tolerance of binary search
double y_mid, triangle, p1_mid, p2_mid, t_mid;

// Binary search loop
while (abs(t_left - t_right) > t_tol)
{
    p1_mid = (p1_left + p1_right) / 2;
    p2_mid = (p2_left + p2_right) / 2;
    t_mid = (t_left + t_right) / 2;
    y_mid = A1 * sin(p1_mid) + A2 * sin(p2_mid);
    triangle = 2 * f_pwm * t_mid - 1;

    // 1
    //
    //
    //
    //
    //
    //
    //
    // 0 /
    // -----
    // 0 | 1/f_pwm
    // t_mid
    if (y_mid < triangle)
    {
        t_right = t_mid;
        p1_right = p1_mid;
        p2_right = p2_mid;
    }
    else
    {
        t_left = t_mid;
        p1_left = p1_mid;
        p2_left = p2_mid;
    }
}
t_mid = (t_left + t_right) / 2;
OutData = t_mid * f_pwm;
write(OutData);
}

reset_action
{
    if (type_is_logical(T1))
        ErrorExit ("Logic types are not allowed for parameter T");

    p1 = t_start * C_2PI * F1;
    p2 = t_start * C_2PI * F2;

```

```
}  
  
attributes  
{  
    // ports attributes  
    OutData.port_rate("1");  
}  
}
```

Quantization

// Quantizes incoming data

// (C) 2006: Infineon

//

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// prohibited without the prior written consent of the copyright owner.

prim_model PWM_quantizer

```
{  
    // data type.  
    type_param T1 = double;  
    // data type.  
    type_param T2 = int;  
    // Output samples  
    port out T1 OutData;  
    // Input samples  
    port in T1 InData;  
    // Number of quantization levels of time. No quantization: levels = -1.  
    param dynamic T2 levels = -1;  
  
    main_action  
    {  
        read(InData);  
  
        //quantization of time?  
        if ( levels != -1 ) //yes  
        {  
            OutData = nint(InData*double(levels))/double(levels);  
        }  
        else //no  
            OutData = InData;  
  
        write(OutData);  
    }  
}
```

Pulse generator

```
// PWM pulse train to discrete-time sample conversion
// Receives the duty ratio (0<dr<1) of a pwm pulse and constructs a discrete
// time signal based on the step response from a fifth order butterworth filter.

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// prohibited without the prior written consent of the copyright owner.

prim_model PWM_LPF_arb
{
    // Signal data type.
    type_param T1 = double;
    // Data type 2.
    type_param T2 = int;
    // Cutoff frequency of LP-filter (5th order butterworth)
    param read_on_reset T1 cutoff = 20e3;
    // Constant 2*pi.
    param const double C_2PI = 8.0*atan(1.0);
    // PWM frequency
    param read_on_reset T2 f_pwm = 100e3;
    // Number of cutoff-frequency time constants to calculate over
    param read_on_reset int N_periods = 5;
    // Output sampling rate
    param read_on_reset float f_out = 50000;
    // timescaling, since the filter's cutoff frequency = 1 rad/sec
    param const double time_scale = cutoff*C_2PI/f_pwm;
    // Number of past samples to store (always at least current and previous)
    param const int N_pwm = nint(N_periods*f_pwm/cutoff)+1;

    // Output samples
    port out T1 OutData;
    // Input samples
    port in T1 InData;

    // Current and past PWM pulse widths in ring buffer
    float inputs[N_pwm];
    // Pointer to latest sample in ring buffer
    int index;
    // Current time in current PWM cycle, range 0 - 1
    float pwm_time;

    main_action
    {
        float output = -0.5;
        double t;

        // In calculations, time is relative to a PWM cycle; it is then
        // converted to a "real" time via time_scale

        // Advance time to next sampling instant
        pwm_time += f_pwm / f_out;
        // If we have moved into a new PWM cycle, we need to read more samples
        while (pwm_time >= 1.0)
```


- Direct Digital Pulse Width Modulation for Class D Amplifiers -

```

    {
        index++; index = (index<N_pwm)?index:0;
        read(InData);
        inputs[index] = InData;
        pwm_time -= 1.0;
    }
    int i = index;
    // Start with current PWM cycle

    // Step response from rising edge at start of current PWM cycle
    t = pwm_time*time_scale;
    output += 1 - 1.89442719099993*exp(-t)
    - 2*1.37638192047116*exp(-0.80901699437495*t)*sin(0.58778525229248*t)
    + 2*0.44721359549996*exp(-0.30901699437495*t)*cos(0.95105651629515*t);
    if (pwm_time > inputs[index])
    {
        // Step response from falling edge within current PWM cycle
        t = (pwm_time-inputs[index])*time_scale;
        output -= 1 - 1.89442719099993*exp(-t)
        - 2*1.37638192047116*exp(-0.80901699437495*t)*sin(0.58778525229248*t)
        + 2*0.44721359549996*exp(-0.30901699437495*t)*cos(0.95105651629515*t);
    }

    // Move to next previous sample
    i--; i = (i<0)?(N_pwm-1):i;
    int j = 1;
    while (i != index)
    {
        // Step response from rising edge at start of past PWM cycle
        t = (pwm_time+j)*time_scale;
        output += 1 - 1.89442719099993*exp(-t)
        - 2*1.37638192047116*exp(-0.80901699437495*t)*sin(0.58778525229248*t)
        + 2*0.44721359549996*exp(-0.30901699437495*t)*cos(0.95105651629515*t);
        // Step response from falling edge within past PWM cycle
        t = (pwm_time-inputs[i]+j)*time_scale;
        output -= 1 - 1.89442719099993*exp(-t)
        - 2*1.37638192047116*exp(-0.80901699437495*t)*sin(0.58778525229248*t)
        + 2*0.44721359549996*exp(-0.30901699437495*t)*cos(0.95105651629515*t);

        j++;
        i--; i = (i<0)?(N_pwm-1):i;
    }
    OutData = output;
    write(OutData);
}

reset_action
{
    // See to it that index wraps to zero on first sample
    index = N_pwm-1;
    // See to it that we just become 1.0 on first sample
    pwm_time = 1.0 - f_pwm / f_out;
    int i;
    for (i=0;i<N_pwm;i++) inputs[i] = 0.0;
}
}

```

Error with calibration

```
// Adds the error of each delay element that is used.
// The error is a random value which is generated at the start of the simulation.

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prim_model PWM_error_adder_cal
{
    // data type.
    type_param T1 = double;
    // data type.
    type_param T2 = int;
    // data type.
    type_param T3 = bit_vector(4,false);
    // Output samples
    port out T1 OutData;
    // Input samples (binary)
    port in T3 InData;
    // Input random value
    port in T1 randIn;
    // Number of bits used in delay line
    param read_on_reset T2 delaybits = 2;
    // Total number of bits used in pulse generator ( log2(levels) )
    param read_on_reset T2 totalbits = 4;

    int got_rand = 0; // to see if random errors has been generated and saved
    double rand[nint(pow(2,delaybits))]; // vector to save the errors in. 1024
                                         //should be enough

    double temp = 0;

    main_action
    {
        // Get random delay element errors
        if (got_rand == 0)
        {
            got_rand = 1;
            for (int i = 0; i < nint(pow(2,delaybits)); i++)
            {
                read(randIn);
                rand[i] = randIn;
            }
        }

        double sum = 0; // The decimal value with error
        int cnt = 0; // Number of delays active

        read(InData);

        // Convert to decimal and count number of delays
        for (int i = delaybits; i<totalbits; i++)
        {
            if ( InData[i] == 1 )
```

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```
        {
            sum = sum + double(1)/pow(2,totalbits-i);
        }
    }

    double delay_line_tot = 0;
    double delay_line[nint(pow(2,delaybits))];

    // Add delay line
    for (int i = 0; i<pow(2,delaybits); i++)
    {
        delay_line[i] = double(1)/pow(2,totalbits) + rand[i];
        delay_line_tot = delay_line_tot + delay_line[i];
    }

    // Calibration
    for (int i = 0; i<pow(2,delaybits); i++)
    {
        delay_line[i] = ((double(1)/pow(2,totalbits-
            delaybits))/delay_line_tot)*delay_line[i];
    }

    temp = ((double(1)/pow(2,totalbits-delaybits))/delay_line_tot); //test

    for (int i = 0; i<delaybits; i++)
    {
        cnt = cnt + InData[i]*pow(2,i);
    }

    for (int i = 0; i<cnt; i++)
    {
        sum = sum + delay_line[i];
    }

    OutData = sum;

    write(OutData);
}
}
```

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Appendix B – Cadence schematics and HDL

Important schematics

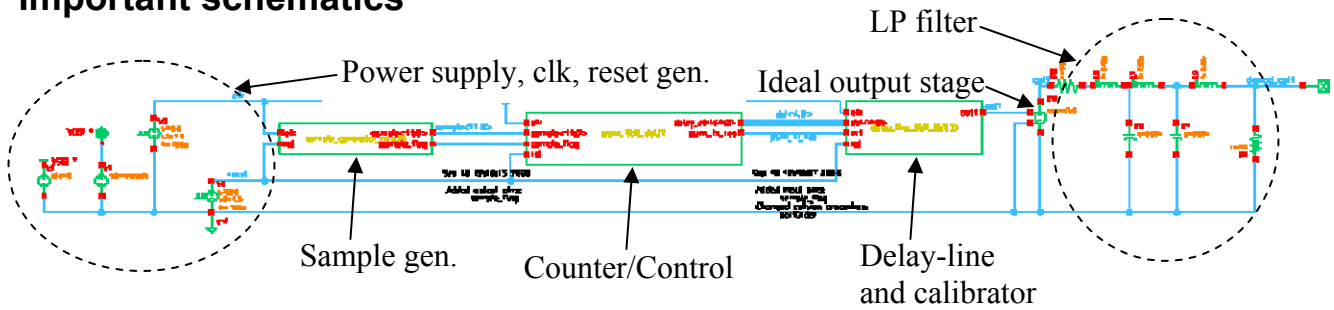


Figure B-1. Top-level schematic.

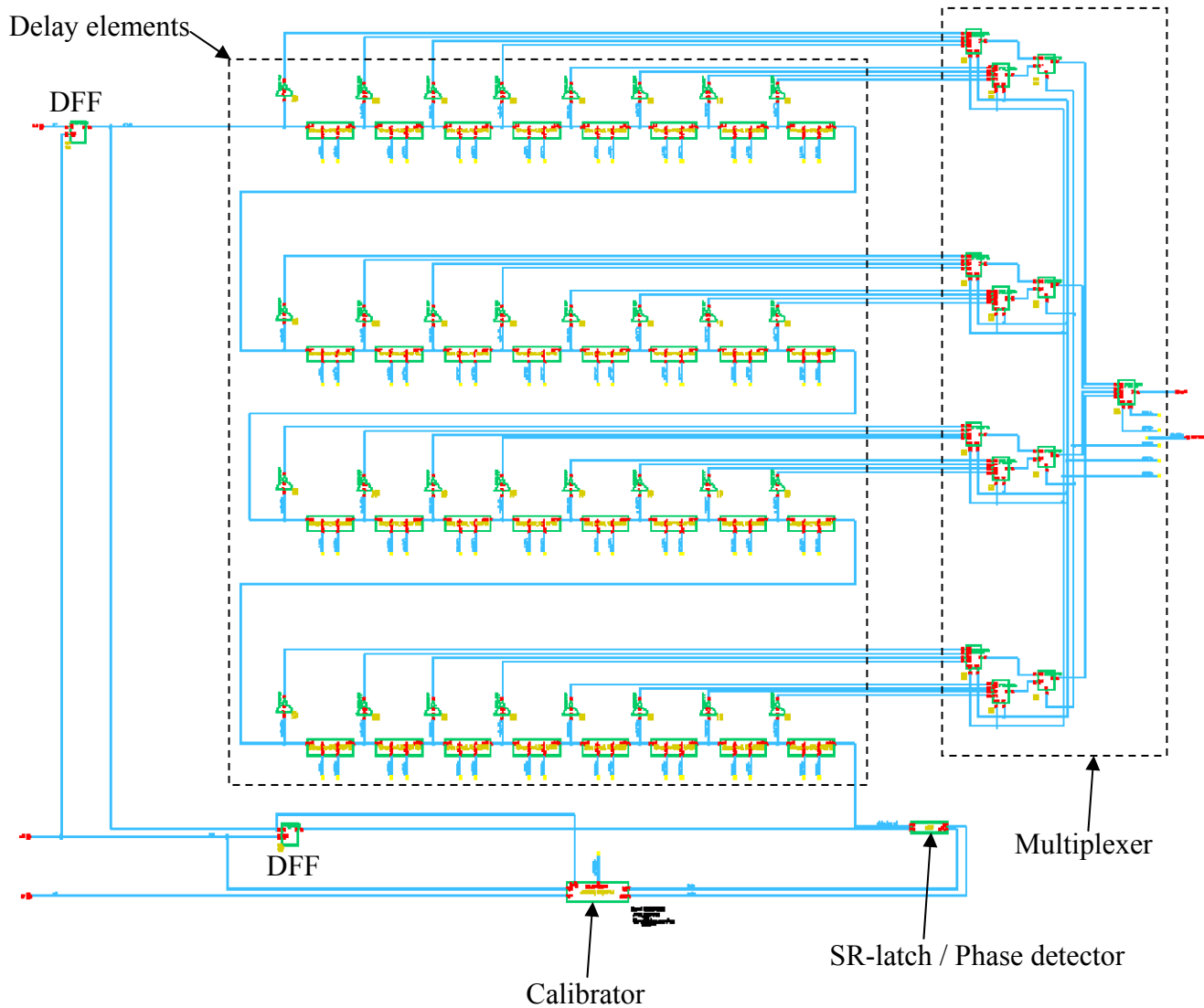


Figure B-2. Delay-line with calibrator.

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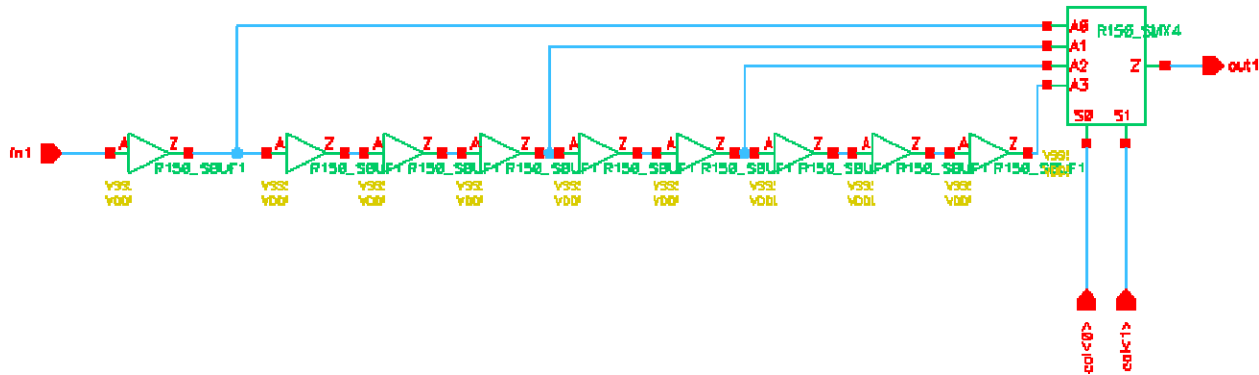


Figure B-3. Delay element 1.1.

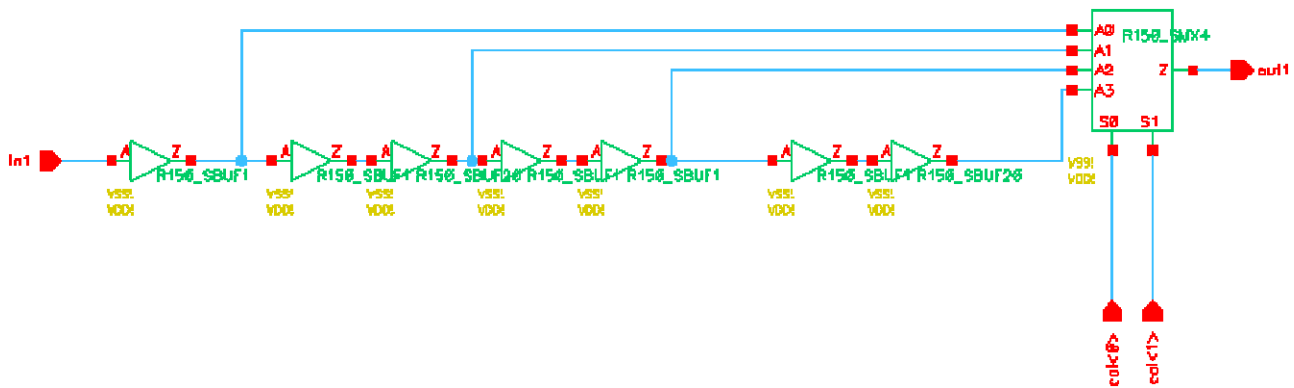


Figure B-4. Delay element 1.2.

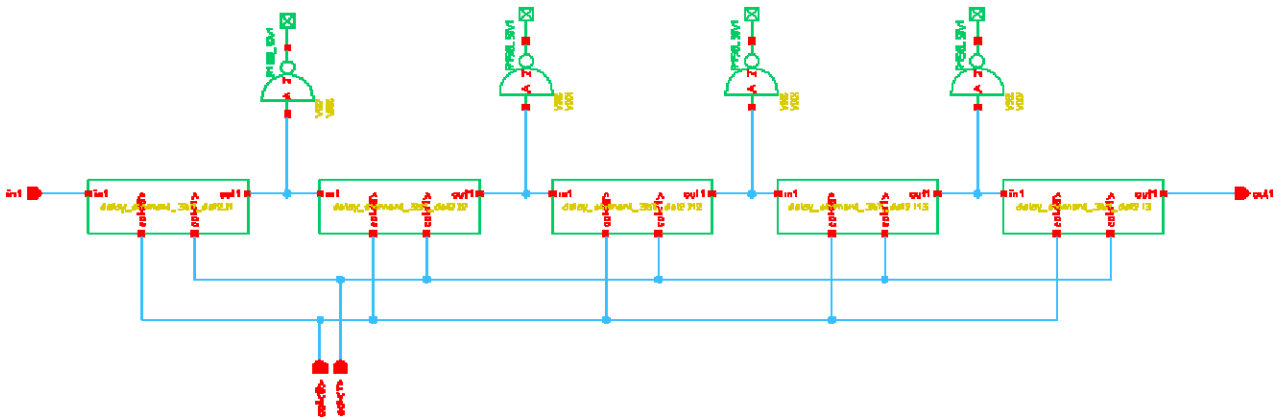


Figure B-5. Delay element 2.1.

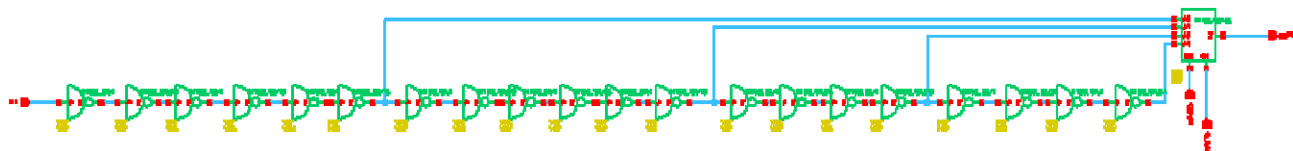


Figure B-6. Delay element 2.2.

Important verilog code

Sample generator

```
// Verilog HDL for "ownlib_ana_starkste", "sample_generator" "verilog"

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//
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// prohibited without the prior written consent of the copyright owner.

`timescale 1 ns / 100 ps

module sample_generator_new(clk,rst,sample,sample_flag);

    input clk;
    input rst;

    output sample_flag; //to indicate a new sample
    reg sample_flag;
    output [11:0] sample;
    reg [11:0] sample;

    integer mem_cnt; //counting the samples in mem
    reg [11:0] mem[0:199];

    initial

//read binary data from file to mem
$readmemb("/home/COSIC/cosic_ana/dss/dss.common.default/units/main/cdb/ownlib_ana_stark
ste/sample_generator_5bit_del/verilog/sinus.data", mem);

    always @ (posedge rst) begin
        sample <= 12'b000001100101;
        mem_cnt = 0;
    end

    //f_pwm = 200

    always begin
        #10 sample <= mem[mem_cnt];
        mem_cnt <= mem_cnt + 1;
        sample_flag <= 1'd1;
        #10 sample_flag <= 1'd0;
        if (mem_cnt == 200) //kanske 199
            mem_cnt = 0;
        #4980;
    end

endmodule
```

Counter/control 26 MHz system

```
// Verilog HDL for "ownlib_ana_starkste", "PWM_modulator" "verilog"

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//
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module pwm_5bit_del(clk,rst,sample,sample_flag,pwm_hi_res,delay_ctrl);

    input clk;
    input rst;
    input [11:0] sample;
    input sample_flag;
    output pwm_hi_res;
    output [4:0] delay_ctrl;

    reg          pwm_hi_res;
    reg [4:0]     delay_ctrl;
    reg [6:0]     cnt;

    always @ (posedge sample_flag) begin
        cnt <= 10'd0;
        delay_ctrl <= 5'd0;
    end

    always @ (posedge clk or posedged rst)
    if (rst) begin
        pwm_hi_res <= 1'b0;
        delay_ctrl <= 5'd0;
        cnt <= 7'd0;
    end
    else begin
        if (cnt >= 7'd2)
            delay_ctrl <= sample[4:0];
        else
            delay_ctrl <= 5'd0;
        if (cnt < sample[11:5])
            pwm_hi_res <= 1'b1;
        else begin
            pwm_hi_res <= 1'b0;
        end
        cnt <= cnt + 7'd1;
    end

endmodule
```


Counter/control 104 MHz system

```
// Verilog HDL for "ownlib_ana_starkste", "PWM_modulator" "verilog"

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module pwm_3bit_del(clk,rst,sample,sample_flag,pwm_hi_res,delay_ctrl);

    input clk;
    input rst;
    input [11:0] sample;
    input sample_flag;
    output pwm_hi_res;
    output [4:0] delay_ctrl;

    reg          pwm_hi_res;
    reg [4:0]     delay_ctrl; //sould be 3 bits if 104 MHz and 5 bits if 40 MHz
    reg [8:0]     cnt;

    always @ (posedge sample_flag) begin
        cnt <= 9'd0;
        delay_ctrl <= 5'd0;
    end

    always @ (posedge clk or posedge rst)
        if (rst) begin
            pwm_hi_res <= 1'b0;
            delay_ctrl <= 5'd0;
            cnt <= 9'd0;
        end
        else begin
            if (cnt >= 9'd2)
                delay_ctrl <= {sample[2:0],2'b00};
            else
                delay_ctrl <= 5'd0;
            if (cnt < sample[11:3])
                pwm_hi_res <= 1'b1;
            else begin
                pwm_hi_res <= 1'b0;
            end
            cnt <= cnt + 9'd1;
        end
    end

endmodule
```

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Appendix C – Matlab code

Important Matlab code

Calibration order calculation

```
% Program that calculates in which order to calibrate
% the delay elements in the delay-line
%
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%
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% prohibited without the prior written consent of the copyright owner.

% Delays (ps) in normal conditions of an element
del1 = 5*120;
del2 = 5*220;
del3 = 5*290;
del4 = 5*380;
del = [del1 del2 del3 del4];

% Number of elements
elements = 32;

% Matrix to save the order
cal_order = zeros(elements);
cal_order_bits = zeros(elements,2*elements);

% Error variable for plot
error = zeros(1,elements);
max_abs_error = zeros(1,elements);

d = 2 % d = 1-3 for each pair of delays
for i = 1:elements %number of elements with a certain delay active
    total_del = i*del(d+1) + (elements - i)*del(d);
    wanted_stage_del = total_del/elements;
    for j = 1:elements %at a certain tap
        del_so_far = sum(cal_order,2);
        if (abs(del(d)+del_so_far(i) - j*wanted_stage_del) > abs(del(d+1)+del_so_far(i)
            - j*wanted_stage_del))
            cal_order(i,j) = del(d+1);
        else
            cal_order(i,j) = del(d);
        end
        error(j) = j*wanted_stage_del - sum(cal_order(i,:),2);
    end
    plot(1:elements,error,'-o');
    title('Nominal conditions');
    xlabel('Delay element');
    ylabel('error (ps)');
    grid on;
    %hold on;
    max_abs_error = max([max_abs_error;abs(error)]);
    pause;
```

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```
end

%plot(1:elements,max_abs_error,'*b');
%hold on;

cal_order
max(error)

% För att kunna föra in i verilog
for i = 1:elements
    for j = 1:elements
        switch cal_order(i,j)
            case del1
                cal_order_bits(i,2*j-1) = 0;
                cal_order_bits(i,2*j) = 0;
            case del2
                cal_order_bits(i,2*j-1) = 1;
                cal_order_bits(i,2*j) = 0;
            case del3
                cal_order_bits(i,2*j-1) = 0;
                cal_order_bits(i,2*j) = 1;
            case del4
                cal_order_bits(i,2*j-1) = 1;
                cal_order_bits(i,2*j) = 1;
        end
    end
end
```

Appendix D – Definitions

$$THD = \frac{\sum \text{Harmonic powers}}{\text{power of fundamental}} = \frac{\sum_{k=2}^{k_{\max}} P_k}{P_1} = \frac{\sqrt{\sum_{k=2}^{k_{\max}} A_k^2}}{A_1}$$

$$THD_{\%} = \frac{THD}{100} \quad THD_{dB} = 10 \log THD$$

$$THD + N = \frac{\sum (\text{Harmonic powers}) + \text{Noise power}}{\text{power of fundamental}} = \frac{\sqrt{\int_0^{f_{\max}} (X(f) - fund)^2 df}}{A_1}$$

$$THD + N_{\%} = \frac{THD + N}{100} \quad THD + N_{dB} = 10 \log THD + N$$

$$SNR = \frac{\text{Power of fundamental}}{\text{Power of noise}} = \frac{P_{fund}}{P_{noise}} = \frac{A_{fund}}{\sqrt{\int_0^{f_{\max}} (X(f) - fund - harmonics)^2 df}}$$

$$SNR_{dB} = 10 \log SNR$$

$$SNDR = \frac{\text{Power of fundamental}}{\text{Power of noise and distortion}} = \frac{P_{fund}}{P_{noise+dist}} = \frac{1}{THD + N}$$

$$SNDR_{dB} = 10 \log SNDR$$

$$PSRR_{dB} = 20 \log \left(\frac{\Delta V_{\text{supply}}}{\Delta V_{\text{out}}} \right)$$

P – Power

A – Amplitude

k_{\max} – Depends on how many harmonics within the bandwidth

$X(f)$ – Signal in frequency domain

f_{\max} – Upper bandwidth limit

ΔV_{supply} – Change in supply voltage

ΔV_{out} – Resulting change on output voltage

På svenska

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