Lab 11
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- Datapath Verilog file (10pt)

```
module dataPath( input clk,input reset,input[1:0] aluControl,input enaALU,input[2:0] SR1,input[2:0] SR2,
input[2:0] DR,input regWE,input[1:0] selPC,input enaMARM,input selMAR,input selEAB1,
input[1:0] selEAB2,input enaPC,input ldPC,input ldIR,input ldMAR,input ldMDR,input selMDR,
input memWE,input flagWE,input enaMDR,output N,output Z,output P,output[15:0] IR);

wire[15:0] Ra,  Rb,  aluOut,  Buss,  eabOut,  MARMuxOut,  mdrOut,  PC;


ALU alu (Ra,  Rb,  IR[5:0],  aluControl,  aluOut); //ALU(input[15:0] Ra,Rb,input[5:0] IR,input[1:0] aluContr
ts_driver EnaALU (aluOut,  Buss,  enaALU);


IR ir (IR,  clk,  Buss,  reset,  ldIR); //IR(output[15:0] IR,  input clk,  input[15:0] Buss,  input reset,


MARMux marmx (IR[7:0],  selMAR,  eabOut,  MARMuxOut); //module MARMux(input[7:0] IR,input selMAR,input[15:0]
ts_driver EnaMARM (MARMuxOut,  Buss,  enaMARM);


Memory memory (mdrOut,  Buss,  clk,  reset,  ldMAR,  ldMDR,  selMDR,  memWE); //Memory(mdrOut, Buss, clk, re
ts_driver EnaMDR (mdrOut,  Buss,  enaMDR);

NZP nzp (clk,  reset,  flagWE,  Buss,  N,  Z,  P); //module NZP(input clk,reset,flagWE,output[15:0] Buss,out


PC pc (Buss,  eabOut,  selPC,  ldPC,  clk,  reset,  PC); //PC(input[15:0] Buss, eabOut,input[1:0] selPC,inpu
ts_driver EnaPC (PC,  Buss,  enaPC);


RegFile regfile(Buss,  DR,  SR1,  SR2,  regWE,  clk,  reset,  Rb,  Ra); //module RegFile(input[15:0] Buss,in

EAB eab (PC,  Ra,  IR,  selEAB2,  selEAB1,  eabOut); //EAB(input[15:0] PC, Ra,input[10:0] IR,input[1:0] selE

endmodule
```

Procedure (30pts possible)

- Master TCL file (2pt)

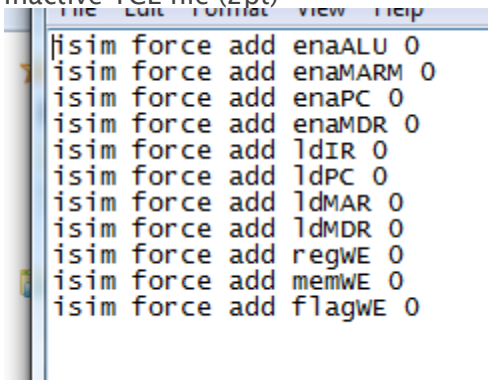
```
source wave.tcl

isim force add clk 0 -time 0 -value 1 -time 5ns -repeat 10ns
isim force add reset 1 -time 0 -value 0 -time 8ns
#run 12ns
run 10ns

#Use the following format for the rest of your TCL file

source fetch00.tcl
source fetch1.tcl
source fetch2.tcl

source and1.tcl

source fetch0.tcl
source fetch1.tcl
source fetch2.tcl

source add1.tcl

source fetch0.tcl
source fetch1.tcl
source fetch2.tcl

source not.tcl

source fetch0.tcl
source fetch1.tcl
source fetch2.tcl

source br1.tcl

source fetch0.tcl
source fetch1.tcl
source fetch2.tcl

source jsr0.tcl
source jsr1.tcl

source fetch0.tcl
source fetch1.tcl
source fetch2.tcl

source ld0.tcl
source ld1.tcl
source ld2a.tcl

source fetch0.tcl
source fetch1.tcl
source fetch2.tcl


source ld0.tcl
source ld1.tcl
source ld2b.tcl

source fetch0.tcl
source fetch1.tcl
source fetch2.tcl

source add_b.tcl

source fetch0.tcl
source fetch1.tcl
source fetch2.tcl

source st0.tcl
source st1.tcl
source st2.tcl

source fetch0.tcl
source fetch1.tcl
source fetch2.tcl

source jmp.tcl

source fetch0.tcl
source fetch1.tcl
source fetch2.tcl

source br_b.tcl

source fetch0.tcl
```

- Wave TCL file (2pt)

File Edit Format View Help

```
wave add clk

wave add reset
wave add Buss -radix hex

#add signals to view the PC and PC control
wave add selPC
wave add enaPC
wave add ldPC
wave add PC -radix hex

#add signals to view the IR and IR control
wave add ldIR
wave add IR -radix hex

#add signals to view the EAB control
wave add selEAB1
wave add selEAB2
wave add eabOut -radix hex

#add signals to view the MARMux control
wave add selMAR
wave add enaMARM
wave add MARMuxOut -radix hex

#add signals to view Register File control
wave add DR
wave add SR1
wave add SR2
wave add regWE

#add signals to view the Registers in the Register File
wave add /regfile/regOut0 -radix hex
wave add /regfile/regOut1 -radix hex
wave add /regfile/regOut2 -radix hex
wave add /regfile/regOut3 -radix hex
wave add /regfile/regOut4 -radix hex
wave add /regfile/regOut5 -radix hex
wave add /regfile/regOut6 -radix hex
wave add /regfile/regOut7 -radix hex
wave add Ra -radix hex
wave add Rb -radix hex

#add signals to view the ALU control
wave add aluControl
wave add enaALU
wave add aluOut -radix hex

#view the condition flags
wave add N
wave add Z
wave add P
wave add flagWE

#add signals to view the Memory Registers and the Memory control
wave add ldMAR
wave add /memory/MARReg -radix hex
wave add ldMDR
wave add enaMDR
wave add selMDR
wave add  mdrOut -radix hex
wave add /memory/memOut -radix hex
wave add memWE
```

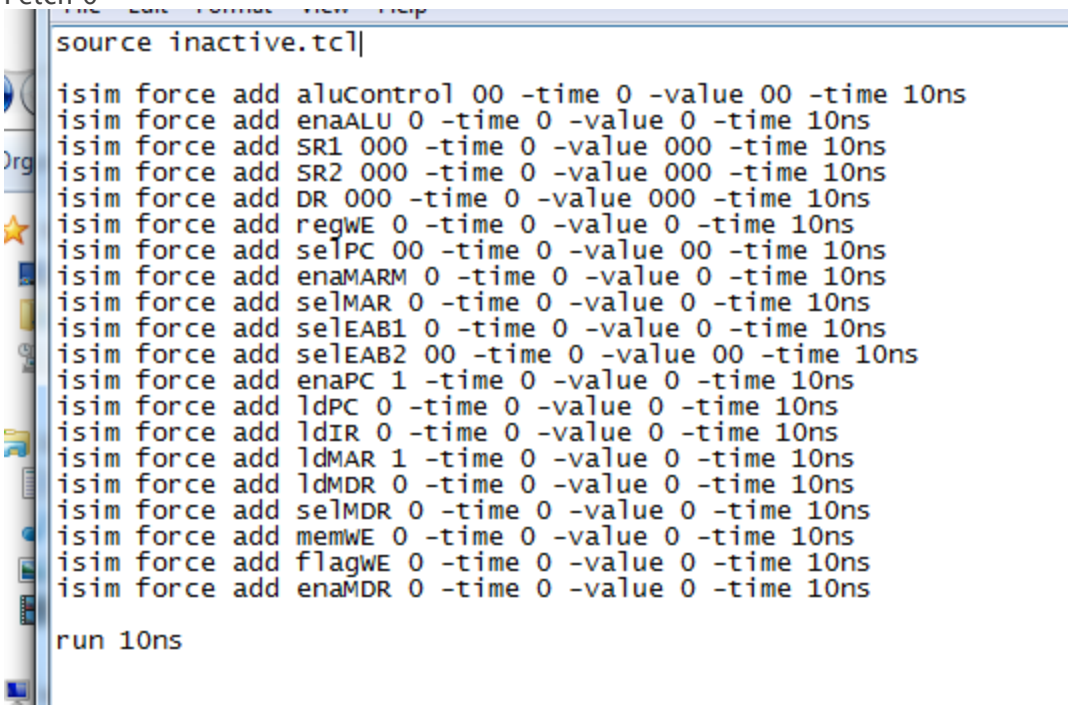
- Inactive TCL file (2pt)



```
isim force add enaALU 0
isim force add enaMARM 0
isim force add enaPC 0
isim force add enaMDR 0
isim force add ldIR 0
isim force add ldPC 0
isim force add ldMAR 0
isim force add ldMDR 0
isim force add regWE 0
isim force add memWE 0
isim force add flagWE 0
```

- Fetch TCL file (2pt)

Fetch 0



```
source inactive.tcl

isim force add aluControl 00 -time 0 -value 00 -time 10ns
isim force add enaALU 0 -time 0 -value 0 -time 10ns
isim force add SR1 000 -time 0 -value 000 -time 10ns
isim force add SR2 000 -time 0 -value 000 -time 10ns
isim force add DR 000 -time 0 -value 000 -time 10ns
isim force add regWE 0 -time 0 -value 0 -time 10ns
isim force add selPC 00 -time 0 -value 00 -time 10ns
isim force add enaMARM 0 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
isim force add selEAB1 0 -time 0 -value 0 -time 10ns
isim force add selEAB2 00 -time 0 -value 00 -time 10ns
isim force add enaPC 1 -time 0 -value 0 -time 10ns
isim force add ldPC 0 -time 0 -value 0 -time 10ns
isim force add ldIR 0 -time 0 -value 0 -time 10ns
isim force add ldMAR 1 -time 0 -value 0 -time 10ns
isim force add ldMDR 0 -time 0 -value 0 -time 10ns
isim force add selMDR 0 -time 0 -value 0 -time 10ns
isim force add memWE 0 -time 0 -value 0 -time 10ns
isim force add flagWE 0 -time 0 -value 0 -time 10ns
isim force add enaMDR 0 -time 0 -value 0 -time 10ns

run 10ns
```

Fetch 1

```
source inactive.tcl

isim force add aluControl 00 -time 0 -value 00 -time 10ns
isim force add enaALU 0 -time 0 -value 0 -time 10ns
isim force add SR1 000 -time 0 -value 000 -time 10ns
isim force add SR2 000 -time 0 -value 000 -time 10ns
isim force add DR 000 -time 0 -value 000 -time 10ns
isim force add regWE 0 -time 0 -value 0 -time 10ns
isim force add selPC 00 -time 0 -value 00 -time 10ns
isim force add enaMARM 0 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
isim force add selEAB1 0 -time 0 -value 0 -time 10ns
isim force add selEAB2 00 -time 0 -value 00 -time 10ns
isim force add enaPC 0 -time 0 -value 0 -time 10ns
isim force add ldPC 1 -time 0 -value 0 -time 10ns
isim force add ldIR 0 -time 0 -value 0 -time 10ns
isim force add ldMAR 0 -time 0 -value 0 -time 10ns
isim force add ldMDR 1 -time 0 -value 0 -time 10ns
isim force add selMDR 1 -time 0 -value 0 -time 10ns
isim force add memWE 0 -time 0 -value 0 -time 10ns
isim force add flagWE 0 -time 0 -value 0 -time 10ns
isim force add enaMDR 0 -time 0 -value 0 -time 10ns

run 10 ns
```

Fetch 2

```
source inactive.tcl

isim force add aluControl 00 -time 0 -value 00 -time 10ns
isim force add enaALU 0 -time 0 -value 0 -time 10ns
isim force add SR1 000 -time 0 -value 000 -time 10ns
isim force add SR2 000 -time 0 -value 000 -time 10ns
isim force add DR 000 -time 0 -value 000 -time 10ns
isim force add regWE 0 -time 0 -value 0 -time 10ns
isim force add selPC 00 -time 0 -value 00 -time 10ns
isim force add enaMARM 0 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
isim force add selEAB1 0 -time 0 -value 0 -time 10ns
isim force add selEAB2 00 -time 0 -value 00 -time 10ns
isim force add enaPC 0 -time 0 -value 0 -time 10ns
isim force add ldPC 0 -time 0 -value 0 -time 10ns
isim force add ldIR 1 -time 0 -value 0 -time 10ns
isim force add ldMAR 0 -time 0 -value 0 -time 10ns
isim force add ldMDR 0 -time 0 -value 0 -time 10ns
isim force add selMDR 0 -time 0 -value 0 -time 10ns
isim force add memWE 0 -time 0 -value 0 -time 10ns
isim force add flagWE 0 -time 0 -value 0 -time 10ns
isim force add enaMDR 1 -time 0 -value 0 -time 10ns

run 10ns
```

- All instruction TCL files (12pt)

AND

source inactive.tcl

isim force add aluControl 10 -time 0 -value 00 -time 10ns
isim force add enaALU 1 -time 0 -value 0 -time 10ns
isim force add SR1 000 -time 0 -value 000 -time 10ns
isim force add SR2 000 -time 0 -value 000 -time 10ns
isim force add DR 000 -time 0 -value 000 -time 10ns
isim force add regWE 1 -time 0 -value 0 -time 10ns
isim force add selPC 00 -time 0 -value 00 -time 10ns
isim force add enaMARM 0 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
isim force add selEAB1 0 -time 0 -value 0 -time 10ns
isim force add selEAB2 00 -time 0 -value 00 -time 10ns
isim force add enaPC 0 -time 0 -value 0 -time 10ns
isim force add ldPC 0 -time 0 -value 0 -time 10ns
isim force add ldIR 0 -time 0 -value 0 -time 10ns
isim force add ldMAR 0 -time 0 -value 0 -time 10ns
isim force add ldMDR 0 -time 0 -value 0 -time 10ns
isim force add selMDR 0 -time 0 -value 0 -time 10ns
isim force add memWE 0 -time 0 -value 0 -time 10ns
isim force add flagWE 1 -time 0 -value 0 -time 10ns
isim force add enaMDR 0 -time 0 -value 0 -time 10ns

run 10ns

BR
source inactive.tcl

isim force add aluControl 00 -time 0 -value 00 -time 10ns
isim force add enaALU 0 -time 0 -value 0 -time 10ns
isim force add SR1 000 -time 0 -value 000 -time 10ns
isim force add SR2 000 -time 0 -value 000 -time 10ns
isim force add DR 000 -time 0 -value 000 -time 10ns
isim force add regWE 0 -time 0 -value 0 -time 10ns
isim force add selPC 01 -time 0 -value 00 -time 10ns
isim force add enaMARM 0 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
isim force add selEAB1 0 -time 0 -value 0 -time 10ns
isim force add selEAB2 10 -time 0 -value 00 -time 10ns
isim force add enaPC 0 -time 0 -value 0 -time 10ns
isim force add ldPC 1 -time 0 -value 0 -time 10ns
isim force add ldIR 0 -time 0 -value 0 -time 10ns
isim force add ldMAR 0 -time 0 -value 0 -time 10ns
isim force add ldMDR 0 -time 0 -value 0 -time 10ns
isim force add selMDR 0 -time 0 -value 0 -time 10ns

```
isim force add memWE 0 -time 0 -value 0 -time 10ns
isim force add flagWE 0 -time 0 -value 0 -time 10ns
isim force add enaMDR 0 -time 0 -value 0 -time 10ns

run 10ns

JUMP

source inactive.tcl

isim force add aluControl 00 -time 0 -value 00 -time 10ns
isim force add enaALU 0 -time 0 -value 0 -time 10ns
isim force add SR1 111 -time 0 -value 000 -time 10ns
isim force add SR2 000 -time 0 -value 000 -time 10ns
isim force add DR 000 -time 0 -value 000 -time 10ns
isim force add regWE 0 -time 0 -value 0 -time 10ns
isim force add selPC 01 -time 0 -value 00 -time 10ns
isim force add enaMARM 0 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
isim force add selEAB1 1 -time 0 -value 0 -time 10ns
isim force add selEAB2 00 -time 0 -value 00 -time 10ns
isim force add enaPC 0 -time 0 -value 0 -time 10ns
isim force add ldPC 1 -time 0 -value 0 -time 10ns
isim force add ldIR 0 -time 0 -value 0 -time 10ns
isim force add ldMAR 0 -time 0 -value 0 -time 10ns
isim force add ldMDR 0 -time 0 -value 0 -time 10ns
isim force add selMDR 0 -time 0 -value 0 -time 10ns
isim force add memWE 0 -time 0 -value 0 -time 10ns
isim force add flagWE 0 -time 0 -value 0 -time 10ns
isim force add enaMDR 0 -time 0 -value 0 -time 10ns

run 10ns

ST0

source inactive.tcl

isim force add aluControl 00 -time 0 -value 00 -time 10ns
isim force add enaALU 0 -time 0 -value 0 -time 10ns
isim force add SR1 000 -time 0 -value 000 -time 10ns
isim force add SR2 000 -time 0 -value 000 -time 10ns
isim force add DR 111 -time 0 -value 000 -time 10ns
isim force add regWE 1 -time 0 -value 0 -time 10ns
isim force add selPC 00 -time 0 -value 00 -time 10ns
isim force add enaMARM 0 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
isim force add selEAB1 0 -time 0 -value 0 -time 10ns
isim force add selEAB2 00 -time 0 -value 00 -time 10ns
```

```
isim force add enaPC 1 -time 0 -value 0 -time 10ns
isim force add ldPC 0 -time 0 -value 0 -time 10ns
isim force add ldIR 0 -time 0 -value 0 -time 10ns
isim force add ldMAR 0 -time 0 -value 0 -time 10ns
isim force add ldMDR 0 -time 0 -value 0 -time 10ns
isim force add selMDR 0 -time 0 -value 0 -time 10ns
isim force add memWE 0 -time 0 -value 0 -time 10ns
isim force add flagWE 0 -time 0 -value 0 -time 10ns
isim force add enaMDR 0 -time 0 -value 0 -time 10ns

run 10ns

ST1

source inactive.tcl

isim force add aluControl 00 -time 0 -value 00 -time 10ns
isim force add enaALU 0 -time 0 -value 0 -time 10ns
isim force add SR1 000 -time 0 -value 000 -time 10ns
isim force add SR2 000 -time 0 -value 000 -time 10ns
isim force add DR 111 -time 0 -value 000 -time 10ns
isim force add regWE 1 -time 0 -value 0 -time 10ns
isim force add selPC 00 -time 0 -value 00 -time 10ns
isim force add enaMARM 0 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
isim force add selEAB1 0 -time 0 -value 0 -time 10ns
isim force add selEAB2 00 -time 0 -value 00 -time 10ns
isim force add enaPC 1 -time 0 -value 0 -time 10ns
isim force add ldPC 0 -time 0 -value 0 -time 10ns
isim force add ldIR 0 -time 0 -value 0 -time 10ns
isim force add ldMAR 0 -time 0 -value 0 -time 10ns
isim force add ldMDR 0 -time 0 -value 0 -time 10ns
isim force add selMDR 0 -time 0 -value 0 -time 10ns
isim force add memWE 0 -time 0 -value 0 -time 10ns
isim force add flagWE 0 -time 0 -value 0 -time 10ns
isim force add enaMDR 0 -time 0 -value 0 -time 10ns

run 10ns

ST2

source inactive.tcl

isim force add aluControl 00 -time 0 -value 00 -time 10ns
isim force add enaALU 0 -time 0 -value 0 -time 10ns
isim force add SR1 000 -time 0 -value 000 -time 10ns
isim force add SR2 000 -time 0 -value 000 -time 10ns
isim force add DR 000 -time 0 -value 000 -time 10ns
```

```
isim force add regWE 0 -time 0 -value 0 -time 10ns
isim force add selPC 00 -time 0 -value 00 -time 10ns
isim force add enaMARM 0 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
isim force add selEAB1 0 -time 0 -value 0 -time 10ns
isim force add selEAB2 00 -time 0 -value 00 -time 10ns
isim force add enaPC 0 -time 0 -value 0 -time 10ns
isim force add ldPC 0 -time 0 -value 0 -time 10ns
isim force add ldIR 0 -time 0 -value 0 -time 10ns
isim force add ldMAR 0 -time 0 -value 0 -time 10ns
isim force add ldMDR 0 -time 0 -value 0 -time 10ns
isim force add selMDR 0 -time 0 -value 0 -time 10ns
isim force add memWE 1 -time 0 -value 0 -time 10ns
isim force add flagWE 0 -time 0 -value 0 -time 10ns
isim force add enaMDR 0 -time 0 -value 0 -time 10ns

run 10ns

ADD

source inactive.tcl

isim force add aluControl 01 -time 0 -value 00 -time 10ns
isim force add enaALU 1 -time 0 -value 0 -time 10ns
isim force add SR1 010 -time 0 -value 000 -time 10ns
isim force add SR2 001 -time 0 -value 000 -time 10ns
isim force add DR 110 -time 0 -value 000 -time 10ns
isim force add regWE 1 -time 0 -value 0 -time 10ns
isim force add selPC 00 -time 0 -value 00 -time 10ns
isim force add enaMARM 0 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
isim force add selEAB1 0 -time 0 -value 0 -time 10ns
isim force add selEAB2 00 -time 0 -value 00 -time 10ns
isim force add enaPC 0 -time 0 -value 0 -time 10ns
isim force add ldPC 0 -time 0 -value 0 -time 10ns
isim force add ldIR 0 -time 0 -value 0 -time 10ns
isim force add ldMAR 0 -time 0 -value 0 -time 10ns
isim force add ldMDR 0 -time 0 -value 0 -time 10ns
isim force add selMDR 0 -time 0 -value 0 -time 10ns
isim force add memWE 0 -time 0 -value 0 -time 10ns
isim force add flagWE 1 -time 0 -value 0 -time 10ns
isim force add enaMDR 0 -time 0 -value 0 -time 10ns

run 10ns

JSR 0
source inactive.tcl
```

```
isim force add aluControl 00 -time 0 -value 00 -time 10ns
isim force add enaALU 0 -time 0 -value 0 -time 10ns
isim force add SR1 000 -time 0 -value 000 -time 10ns
isim force add SR2 000 -time 0 -value 000 -time 10ns
isim force add DR 111 -time 0 -value 000 -time 10ns
isim force add regWE 1 -time 0 -value 0 -time 10ns
isim force add selPC 00 -time 0 -value 00 -time 10ns
isim force add enaMARM 0 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
isim force add selEAB1 0 -time 0 -value 0 -time 10ns
isim force add selEAB2 00 -time 0 -value 00 -time 10ns
isim force add enaPC 1 -time 0 -value 0 -time 10ns
isim force add ldPC 0 -time 0 -value 0 -time 10ns
isim force add ldIR 0 -time 0 -value 0 -time 10ns
isim force add ldMAR 0 -time 0 -value 0 -time 10ns
isim force add ldMDR 0 -time 0 -value 0 -time 10ns
isim force add selMDR 0 -time 0 -value 0 -time 10ns
isim force add memWE 0 -time 0 -value 0 -time 10ns
isim force add flagWE 0 -time 0 -value 0 -time 10ns
isim force add enaMDR 0 -time 0 -value 0 -time 10ns

run 10ns

JSR 1

source inactive.tcl

isim force add aluControl 00 -time 0 -value 00 -time 10ns
isim force add enaALU 0 -time 0 -value 0 -time 10ns
isim force add SR1 000 -time 0 -value 000 -time 10ns
isim force add SR2 000 -time 0 -value 000 -time 10ns
isim force add DR 000 -time 0 -value 000 -time 10ns
isim force add regWE 0 -time 0 -value 0 -time 10ns
isim force add selPC 01 -time 0 -value 00 -time 10ns
isim force add enaMARM 0 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
isim force add selEAB1 0 -time 0 -value 0 -time 10ns
isim force add selEAB2 11 -time 0 -value 00 -time 10ns
isim force add enaPC 0 -time 0 -value 0 -time 10ns
isim force add ldPC 1 -time 0 -value 0 -time 10ns
isim force add ldIR 0 -time 0 -value 0 -time 10ns
isim force add ldMAR 0 -time 0 -value 0 -time 10ns
isim force add ldMDR 0 -time 0 -value 0 -time 10ns
isim force add selMDR 0 -time 0 -value 0 -time 10ns
isim force add memWE 0 -time 0 -value 0 -time 10ns
isim force add flagWE 0 -time 0 -value 0 -time 10ns
isim force add enaMDR 0 -time 0 -value 0 -time 10ns
```

run 10ns

LD 0

source inactive.tcl

```
isim force add aluControl 00 -time 0 -value 00 -time 10ns
isim force add enaALU 0 -time 0 -value 0 -time 10ns
isim force add SR1 000 -time 0 -value 000 -time 10ns
isim force add SR2 000 -time 0 -value 000 -time 10ns
isim force add DR 000 -time 0 -value 000 -time 10ns
isim force add regWE 0 -time 0 -value 0 -time 10ns
isim force add selPC 00 -time 0 -value 00 -time 10ns
isim force add enaMARM 1 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
isim force add selEAB1 0 -time 0 -value 0 -time 10ns
isim force add selEAB2 10 -time 0 -value 00 -time 10ns
isim force add enaPC 0 -time 0 -value 0 -time 10ns
isim force add ldPC 0 -time 0 -value 0 -time 10ns
isim force add ldIR 0 -time 0 -value 0 -time 10ns
isim force add ldMAR 1 -time 0 -value 0 -time 10ns
isim force add ldMDR 0 -time 0 -value 0 -time 10ns
isim force add selMDR 0 -time 0 -value 0 -time 10ns
isim force add memWE 0 -time 0 -value 0 -time 10ns
isim force add flagWE 0 -time 0 -value 0 -time 10ns
isim force add enaMDR 0 -time 0 -value 0 -time 10ns
```

run 10ns

LD 1

source inactive.tcl

```
isim force add aluControl 00 -time 0 -value 00 -time 10ns
isim force add enaALU 0 -time 0 -value 0 -time 10ns
isim force add SR1 000 -time 0 -value 000 -time 10ns
isim force add SR2 000 -time 0 -value 000 -time 10ns
isim force add DR 000 -time 0 -value 000 -time 10ns
isim force add regWE 0 -time 0 -value 0 -time 10ns
isim force add selPC 00 -time 0 -value 00 -time 10ns
isim force add enaMARM 0 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
isim force add selEAB1 0 -time 0 -value 0 -time 10ns
isim force add selEAB2 00 -time 0 -value 00 -time 10ns
isim force add enaPC 0 -time 0 -value 0 -time 10ns
isim force add ldPC 0 -time 0 -value 0 -time 10ns
isim force add ldIR 0 -time 0 -value 0 -time 10ns
isim force add ldMAR 0 -time 0 -value 0 -time 10ns
```

```
isim force add ldMDR 1 -time 0 -value 0 -time 10ns
isim force add selMDR 1 -time 0 -value 0 -time 10ns
isim force add memWE 0 -time 0 -value 0 -time 10ns
isim force add flagWE 0 -time 0 -value 0 -time 10ns
isim force add enaMDR 0 -time 0 -value 0 -time 10ns

run 10ns
```

LD 2

```
source inactive.tcl

isim force add aluControl 00 -time 0 -value 00 -time 10ns
isim force add enaALU 0 -time 0 -value 0 -time 10ns
isim force add SR1 000 -time 0 -value 000 -time 10ns
isim force add SR2 000 -time 0 -value 000 -time 10ns
isim force add DR 010 -time 0 -value 000 -time 10ns
isim force add regWE 1 -time 0 -value 0 -time 10ns
isim force add selPC 00 -time 0 -value 00 -time 10ns
isim force add enaMARM 0 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
isim force add selEAB1 0 -time 0 -value 0 -time 10ns
isim force add selEAB2 00 -time 0 -value 00 -time 10ns
isim force add enaPC 0 -time 0 -value 0 -time 10ns
isim force add ldPC 0 -time 0 -value 0 -time 10ns
isim force add ldIR 0 -time 0 -value 0 -time 10ns
isim force add ldMAR 0 -time 0 -value 0 -time 10ns
isim force add ldMDR 0 -time 0 -value 0 -time 10ns
isim force add selMDR 0 -time 0 -value 0 -time 10ns
isim force add memWE 0 -time 0 -value 0 -time 10ns
isim force add flagWE 0 -time 0 -value 0 -time 10ns
isim force add enaMDR 1 -time 0 -value 0 -time 10ns

run 10ns
```

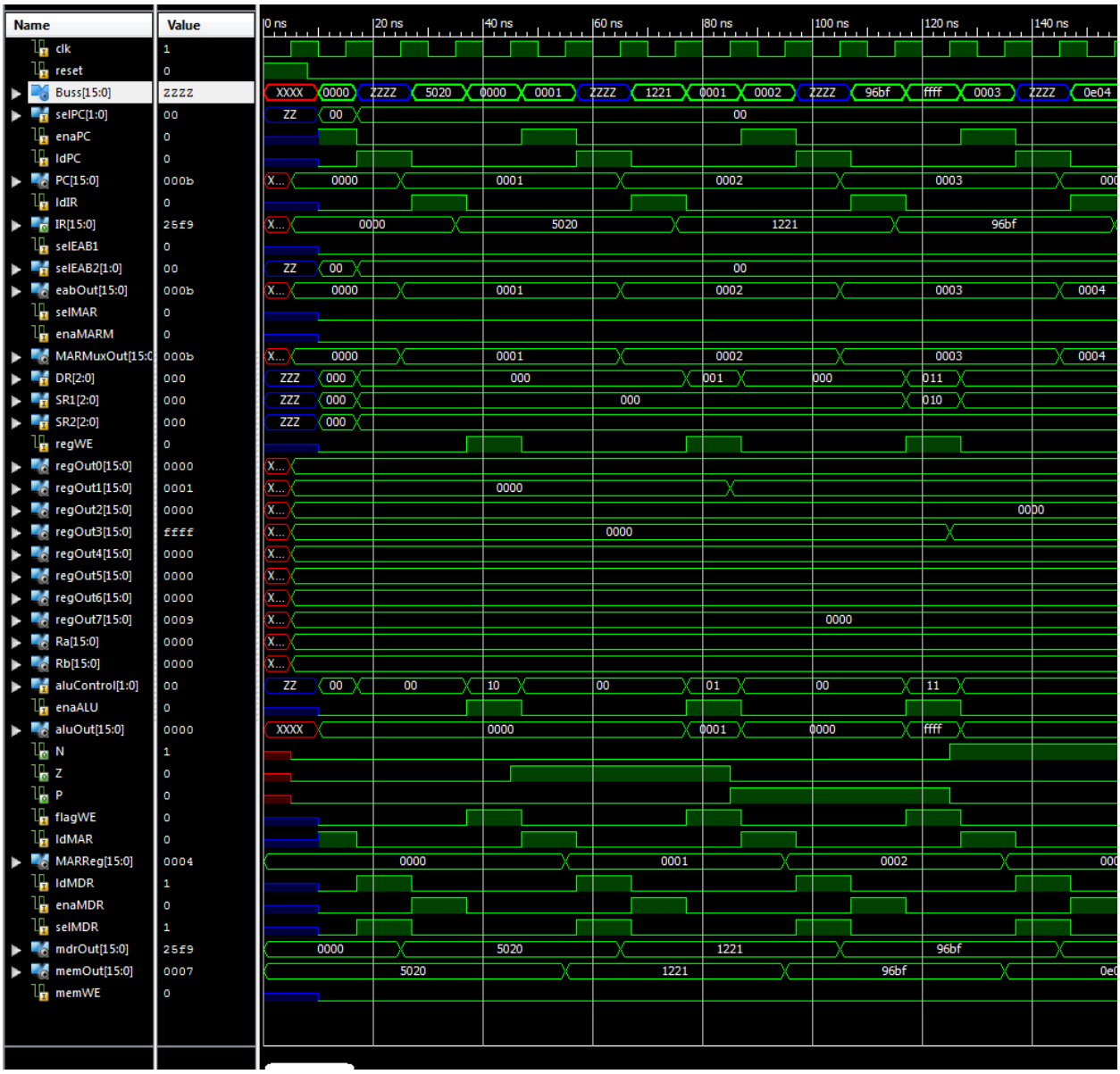
NOT

```
source inactive.tcl

isim force add aluControl 11 -time 0 -value 00 -time 10ns
isim force add enaALU 1 -time 0 -value 0 -time 10ns
isim force add SR1 010 -time 0 -value 000 -time 10ns
isim force add SR2 000 -time 0 -value 000 -time 10ns
isim force add DR 011 -time 0 -value 000 -time 10ns
isim force add regWE 1 -time 0 -value 0 -time 10ns
isim force add selPC 00 -time 0 -value 00 -time 10ns
isim force add enaMARM 0 -time 0 -value 0 -time 10ns
isim force add selMAR 0 -time 0 -value 0 -time 10ns
```

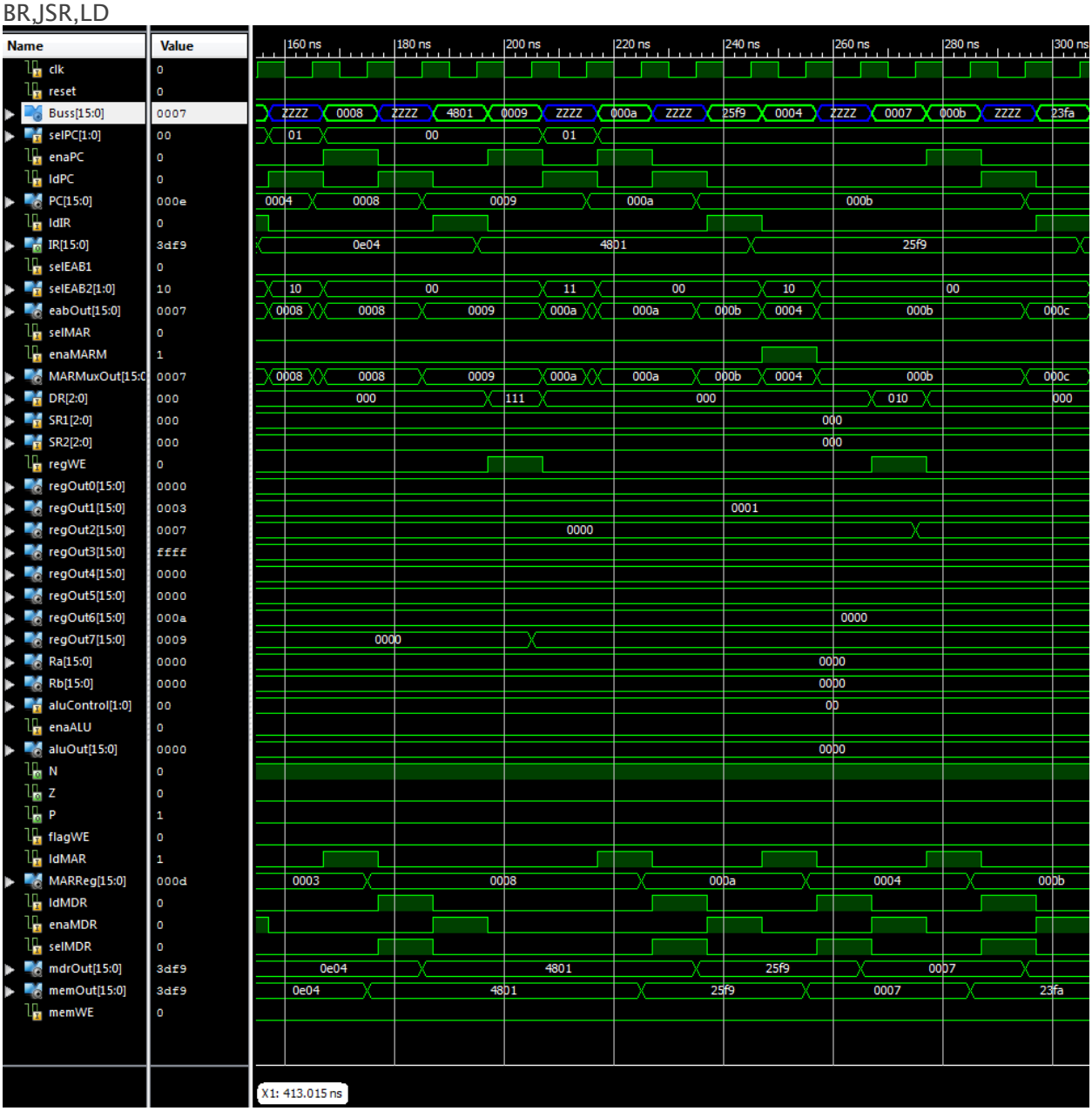
```
isim force add selEAB1 0 -time 0 -value 0 -time 10ns
isim force add selEAB2 00 -time 0 -value 00 -time 10ns
isim force add enaPC 0 -time 0 -value 0 -time 10ns
isim force add ldPC 0 -time 0 -value 0 -time 10ns
isim force add ldIR 0 -time 0 -value 0 -time 10ns
isim force add ldMAR 0 -time 0 -value 0 -time 10ns
isim force add ldMDR 0 -time 0 -value 0 -time 10ns
isim force add selMDR 0 -time 0 -value 0 -time 10ns
isim force add memWE 0 -time 0 -value 0 -time 10ns
isim force add flagWE 1 -time 0 -value 0 -time 10ns
isim force add enaMDR 0 -time 0 -value 0 -time 10ns

run 10ns
```

- Full Simulation waveform (10pt)

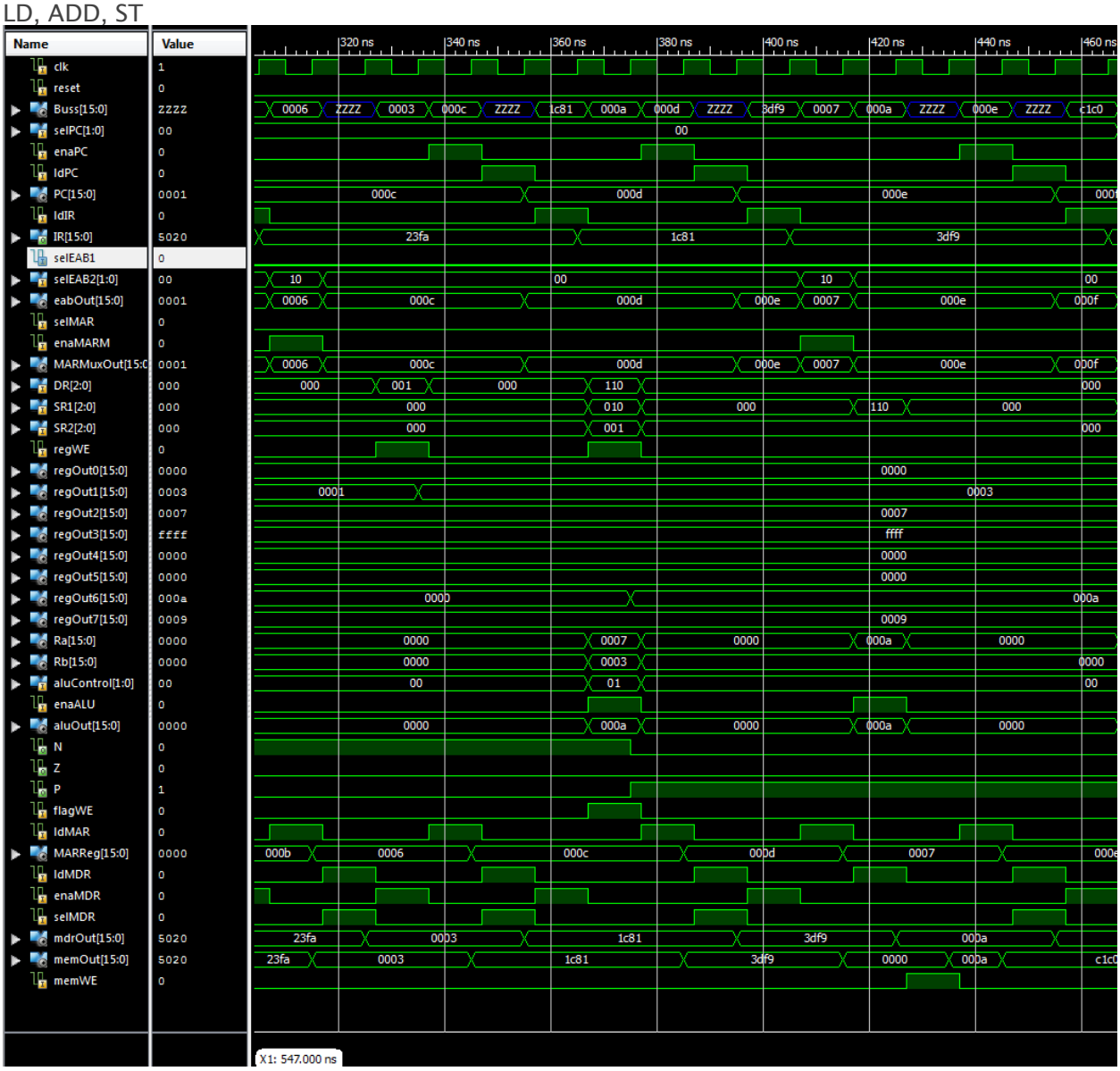
AND, ADD, NOT


Name
Value
clk
reset
Buss[15:0]
selPC[1:0]
enaPC
ldPC
PC[15:0]
ldIR
IR[15:0]
selEAB1
selEAB2[1:0]
eabOut[15:0]
selMAR
enaMARM
MARMuxOut[15:0]
DR[2:0]
SR1[2:0]
SR2[2:0]
regWE
regOut0[15:0]
regOut1[15:0]
regOut2[15:0]
regOut3[15:0]
regOut4[15:0]
regOut5[15:0]
regOut6[15:0]
regOut7[15:0]
Ra[15:0]
Rb[15:0]
aluControl[1:0]
enaALU
aluOut[15:0]
N
Z
P
flagWE
ldMAR
MARReg[15:0]
ldMDR
enaMDR
selMDR
mdrOut[15:0]
memOut[15:0]
memWE
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
140 ns

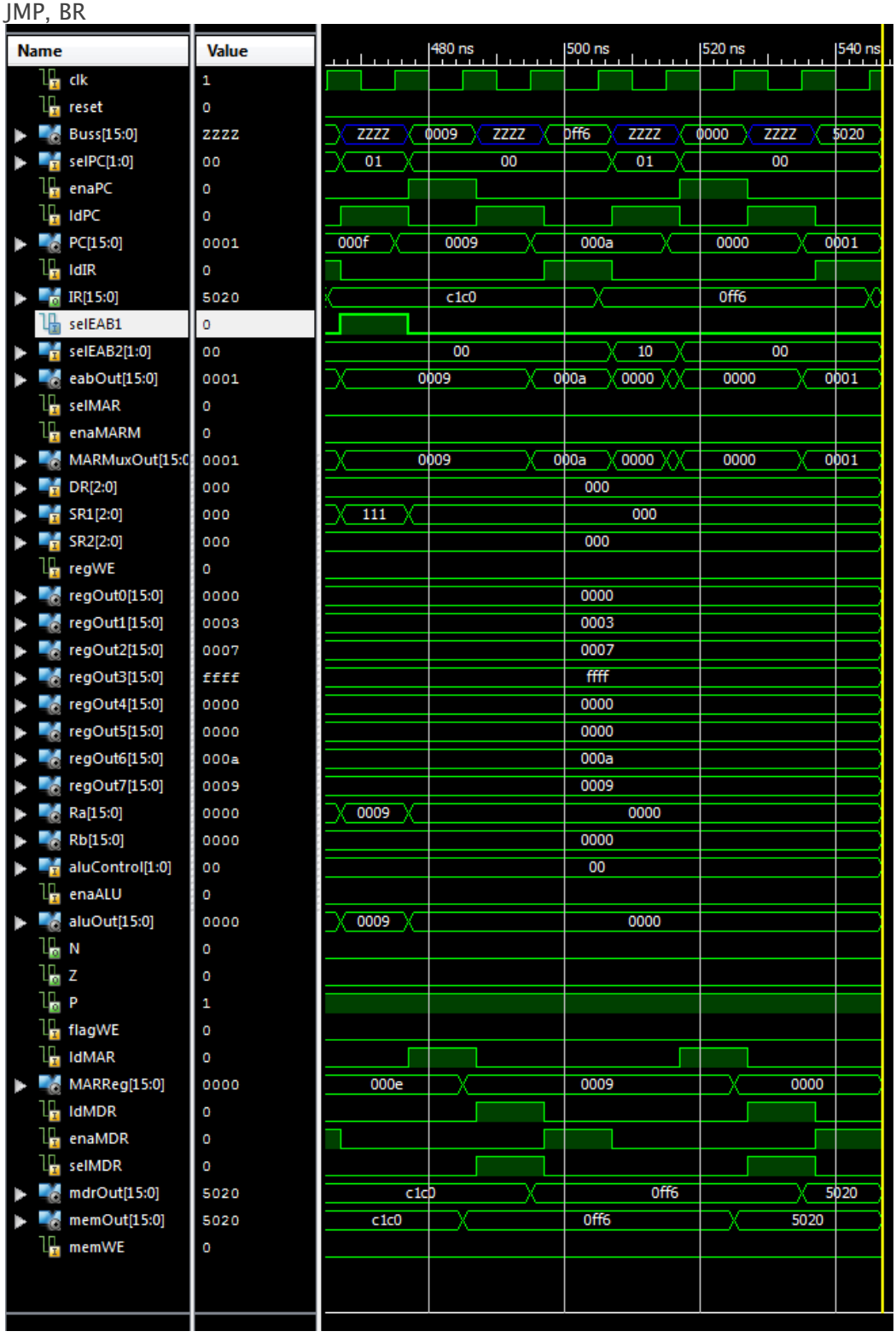
BR,JSR,LD


Name
Value
clk 0
reset 0
Buss[15:0] 0007
selPC[1:0] 00
enaPC 0
ldPC 0
PC[15:0] 000e
ldIR 0
IR[15:0] 3df9
selEAB1 0
selEAB2[1:0] 10
eabOut[15:0] 0007
selMAR 0
enaMARM 1
MARMuxOut[15:0] 0007
DR[2:0] 000
SR1[2:0] 000
SR2[2:0] 000
regWE 0
regOut0[15:0] 0000
regOut1[15:0] 0003
regOut2[15:0] 0007
regOut3[15:0] ffff
regOut4[15:0] 0000
regOut5[15:0] 0000
regOut6[15:0] 000a
regOut7[15:0] 0009
Ra[15:0] 0000
Rb[15:0] 0000
aluControl[1:0] 00
enaALU 0
aluOut[15:0] 0000
N 0
Z 0
P 1
flagWE 0
ldMAR 1
MARReg[15:0] 000d
ldMDR 0
enaMDR 0
selMDR 0
mdrOut[15:0] 3df9
memOut[15:0] 3df9
memWE 0
160 ns
180 ns
200 ns
220 ns
240 ns
260 ns
280 ns
300 ns
X1: 413.015 ns

LD, ADD, ST


Name
Value
clk 1
reset 0
Buss[15:0] zzzz
selPC[1:0] 00
enaPC 0
ldPC 0
PC[15:0] 0001
ldIR 0
IR[15:0] 5020
selEAB1 0
selEAB2[1:0] 00
eabOut[15:0] 0001
selMAR 0
enaMARM 0
MARMuxOut[15:0] 0001
DR[2:0] 000
SR1[2:0] 000
SR2[2:0] 000
regWE 0
regOut0[15:0] 0000
regOut1[15:0] 0003
regOut2[15:0] 0007
regOut3[15:0] ffff
regOut4[15:0] 0000
regOut5[15:0] 0000
regOut6[15:0] 000a
regOut7[15:0] 0009
Ra[15:0] 0000
Rb[15:0] 0000
aluControl[1:0] 00
enaALU 0
aluOut[15:0] 0000
N 0
Z 0
P 1
flagWE 0
ldMAR 0
MARReg[15:0] 0000
ldMDR 0
enaMDR 0
selMDR 0
mdrOut[15:0] 5020
memOut[15:0] 5020
memWE 0
320 ns
340 ns
360 ns
380 ns
400 ns
420 ns
440 ns
460 ns
X1: 547.000 ns

JMP, BR


Name
Value
480 ns
500 ns
520 ns
540 ns
clk 1
reset 0
Buss[15:0] zzzz
selPC[1:0] 00
enaPC 0
ldPC 0
PC[15:0] 0001
ldIR 0
IR[15:0] 5020
selEAB1 0
selEAB2[1:0] 00
eabOut[15:0] 0001
selMAR 0
enaMARM 0
MARMuxOut[15:0] 0001
DR[2:0] 000
SR1[2:0] 000
SR2[2:0] 000
regWE 0
regOut0[15:0] 0000
regOut1[15:0] 0003
regOut2[15:0] 0007
regOut3[15:0] ffff
regOut4[15:0] 0000
regOut5[15:0] 0000
regOut6[15:0] 000a
regOut7[15:0] 0009
Ra[15:0] 0000
Rb[15:0] 0000
aluControl[1:0] 00
enaALU 0
aluOut[15:0] 0000
N 0
Z 0
P 1
flagWE 0
ldMAR 0
MARReg[15:0] 0000
ldMDR 0
enaMDR 0
selMDR 0
mdrOut[15:0] 5020
memOut[15:0] 5020
memWE 0
ZZZZ 0009 ZZZZ 0ff6 ZZZZ 0000 ZZZZ 5020
01 00 01 00
000f 0009 000a 0000 0001
c1c0 0ff6
00 10 00
0009 000a 0000 0000 0001
0009 000a 0000 0000 0001
000
111 000
000
0000
0003
0007
ffff
0000
0000
000a
0009
0009 0000
0000
00
0009 0000
000e 0009 0000
c1c0 0ff6 5020
c1c0 0ff6 5020

Anomalies (bugs, problems, and suggestions)(5pts possible)

Hard lab but very educative.. TAs are very helpful