Lab #6 - Oscilloscope/Logic Analyzer

Isai Mercado Oliveros

Oct 15, 2014

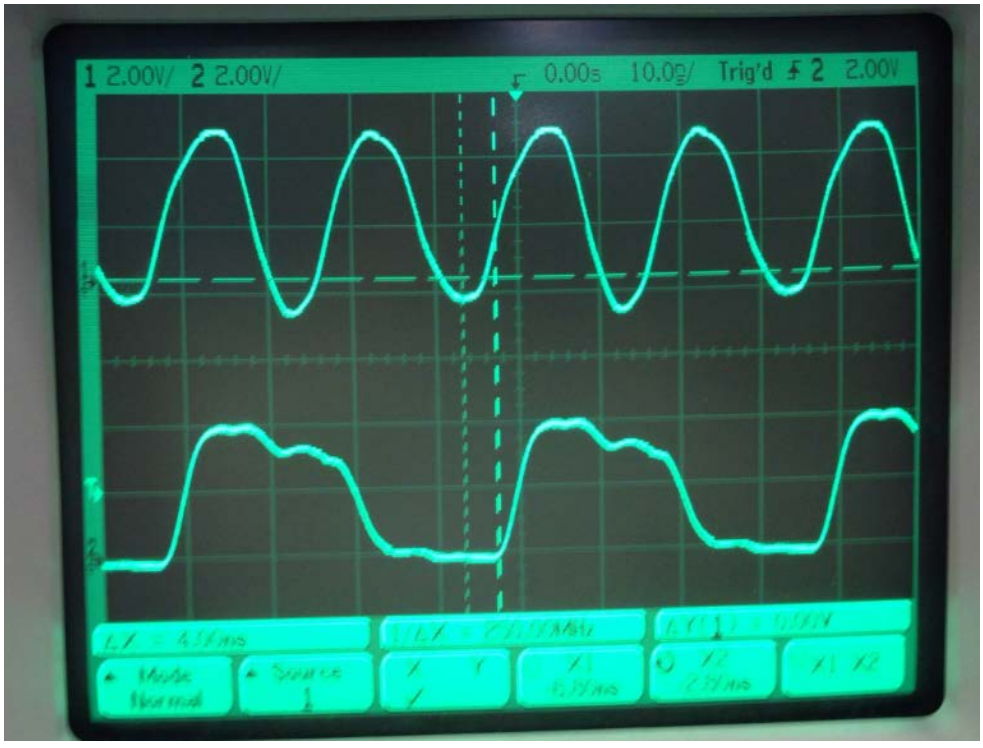
Toggle circuit Verilog code

```
//
//////////////////////////////////////////////////////////////////////////////////
module Toogle(GCLK, CLR, Qout, Clk_out);
    input GCLK, CLR;
    output Qout, Clk_out;
    wire n;

//FF_DC(q, clk, clr, d); input clk, clr, d; output reg q;
    FF_DC hi (Qout,GCLK,CLR,n);
    not(n,Qout);
    buf(Clk_out,GCLK);

endmodule
```

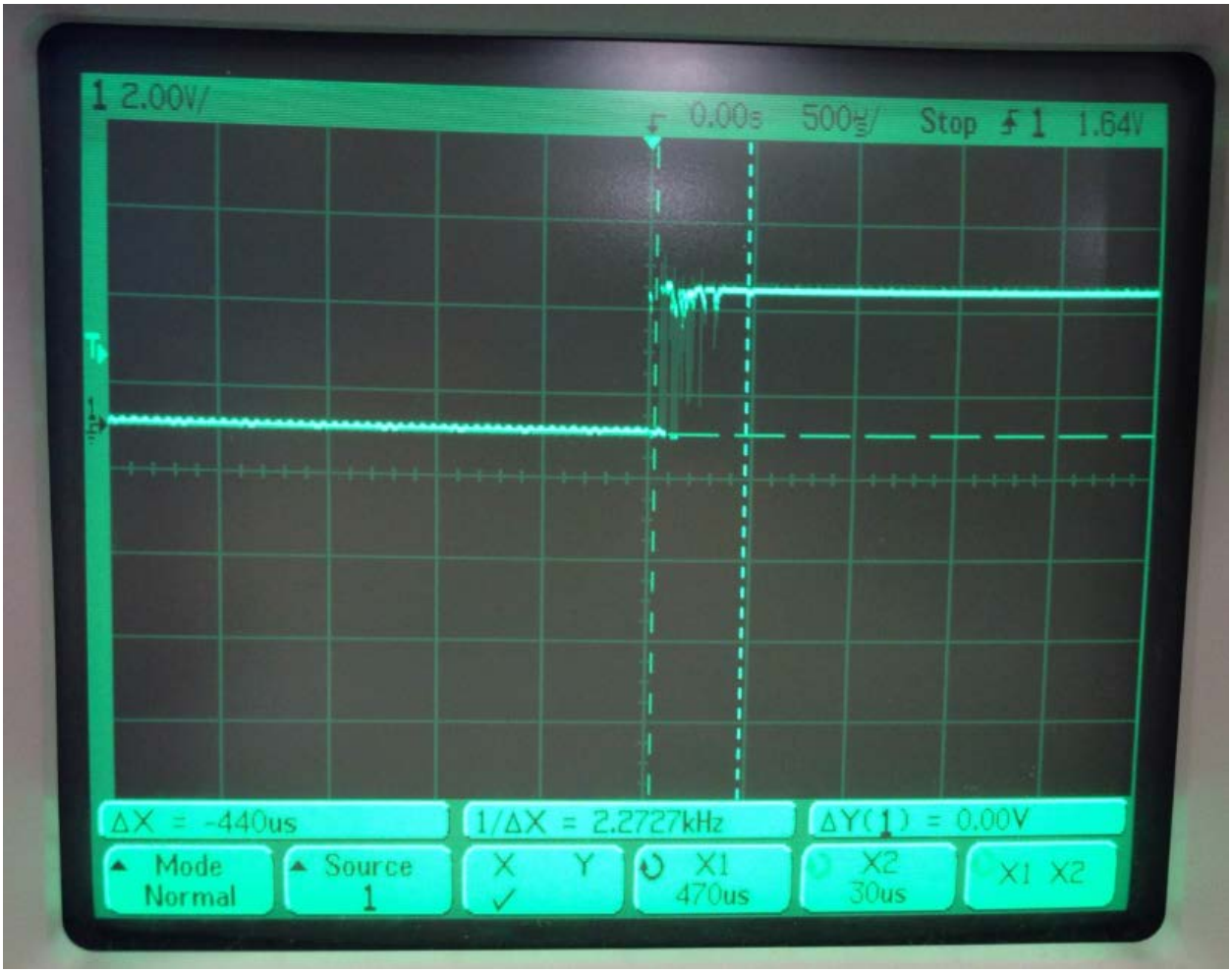
Toggle circuit screen capture



Toggle circuit question and answer (Why is wave not square?)

Because Analogous signals are never a square

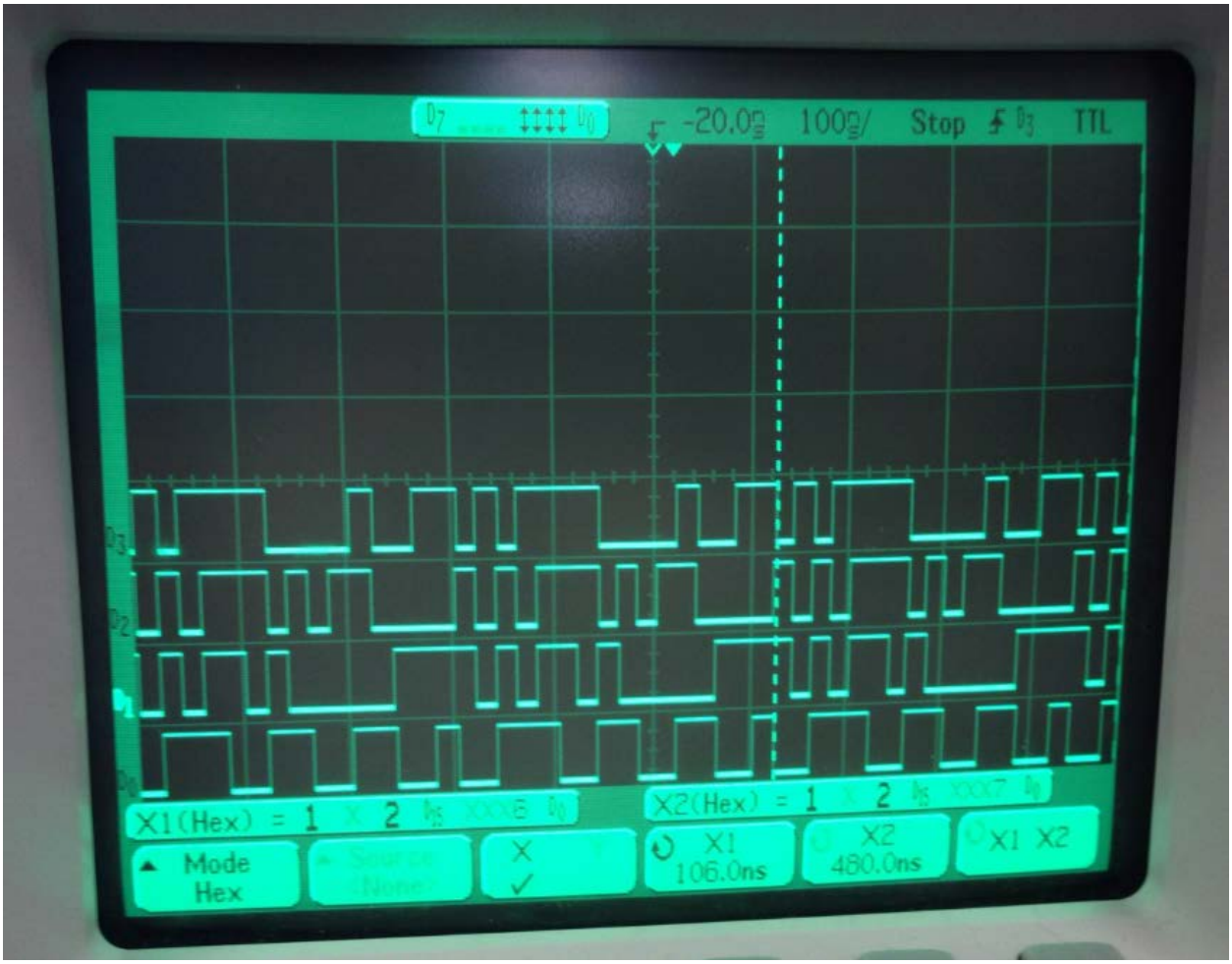
Bounce circuit screen capture



Bounce circuit settling time

440 us

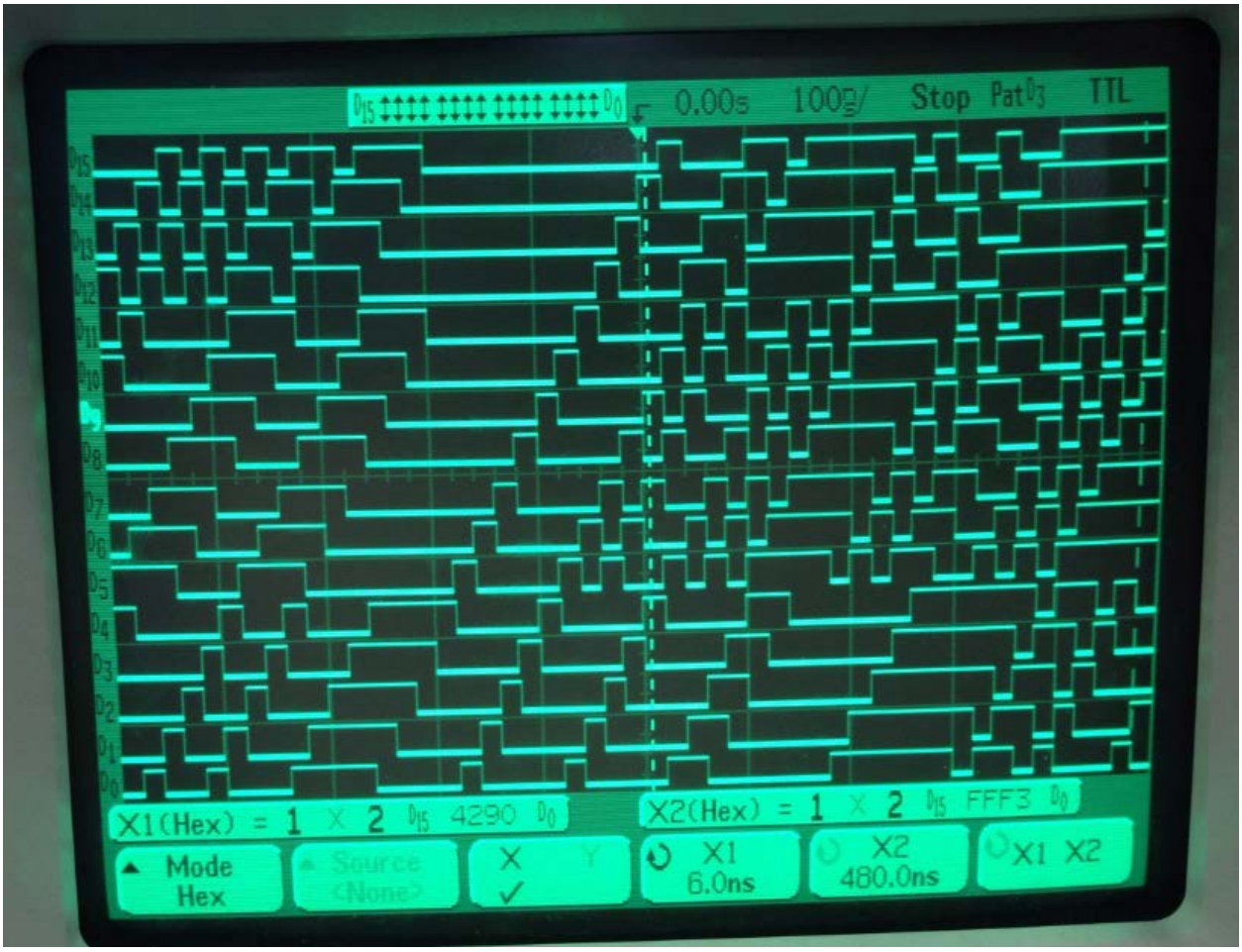
4-bit Shifter screen capture



4-bit Shifter pattern of values

0,4,D,1,2,A,B,6,8,7,9,F,E,C,3,5,0

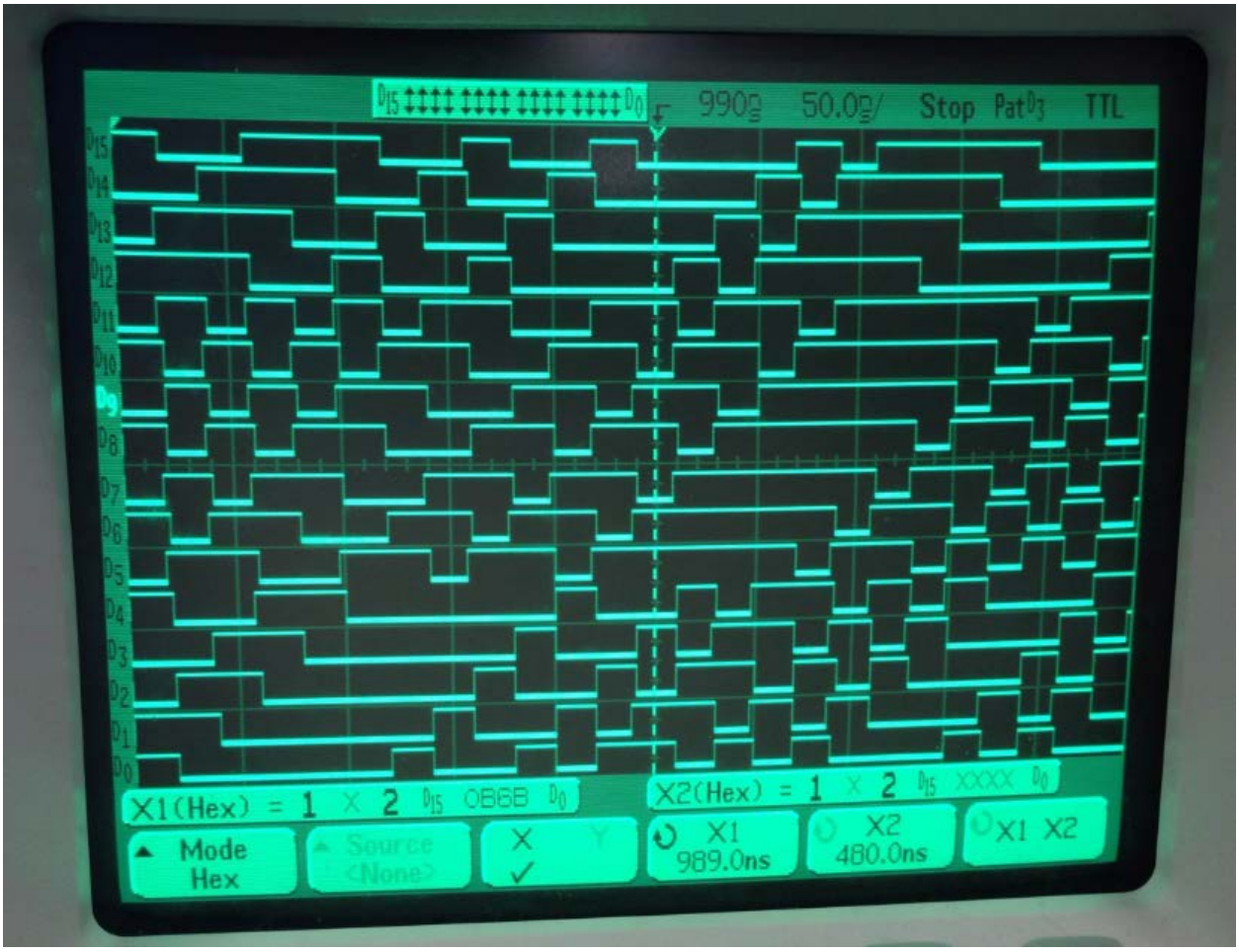
16-bit Shifter screen capture (start at 4290 Hex)



16-bit Shifter four values (start at 4290 Hex)

4290,8521,1A43, 34A6, 694C

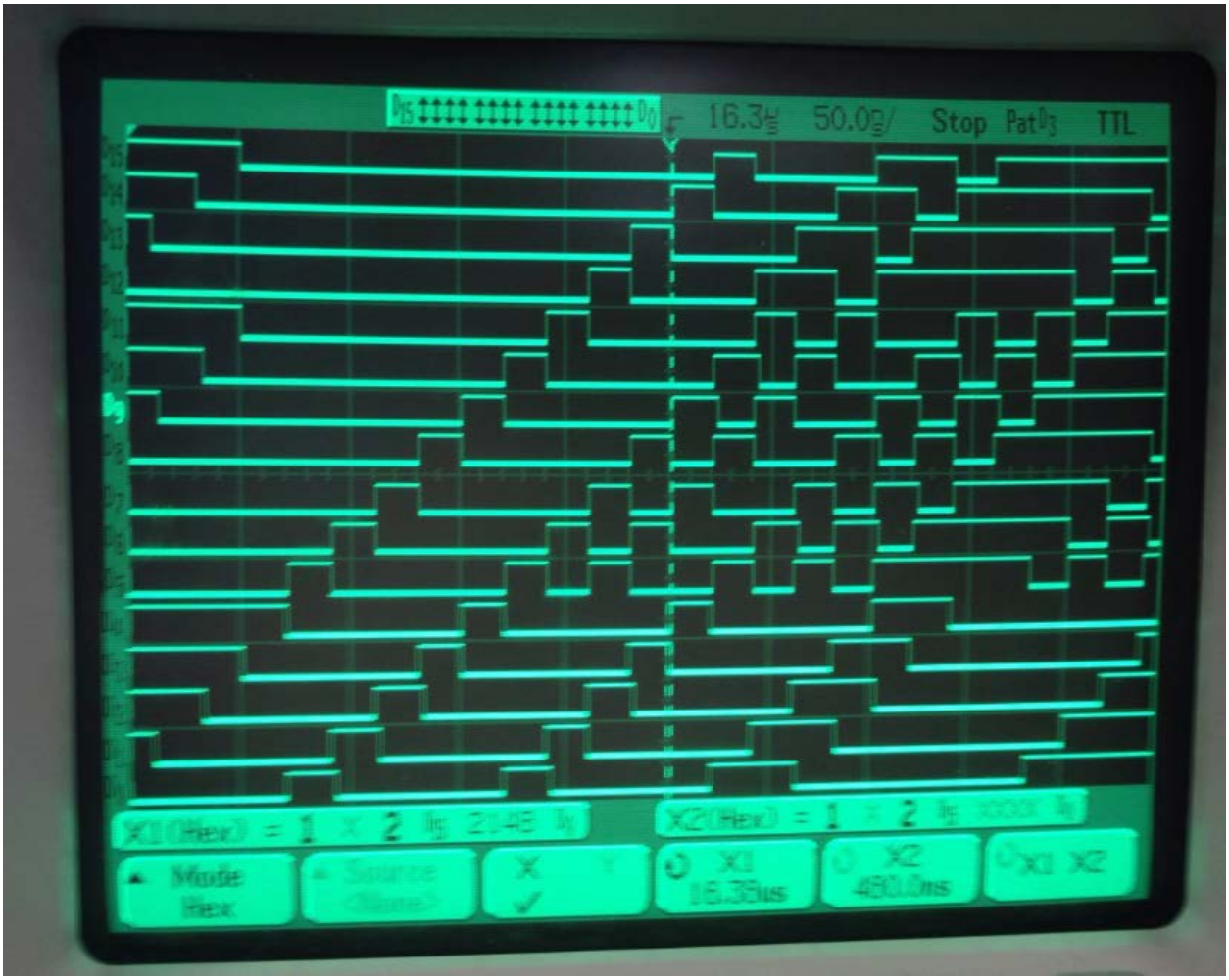
16-bit Shifter screen capture (990ns after triggered pattern)



16-bit Shifter value (990ns after triggered pattern)

0B6B

16-bit Shifter screen capture (16.38us after triggered pattern)



16-bit Shifter value (16.38us after triggered pattern)

4290

16-bit Shifter total number of values in repeating pattern

819

Anomalies (bugs, problems, and suggestions)

The lab is hard because using the oscilloscope is hard, but other than that it is pretty straight forward.