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Reconfigurable & embedded Digital Systems

Description d'éléments mémoire en VHDL

CONCEPTION DE SYSTÈMES NUMÉRIQUES (CSN)

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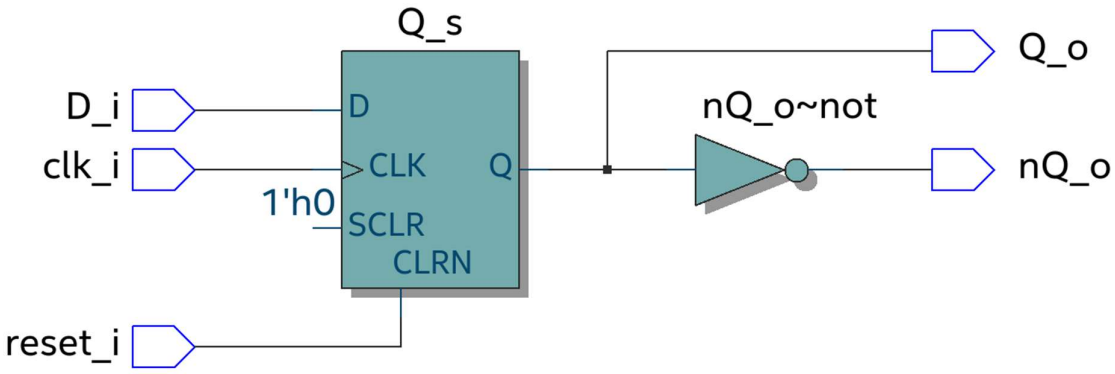
Salle : A09
Classe : CSN

Dff_ar

Vues RTL

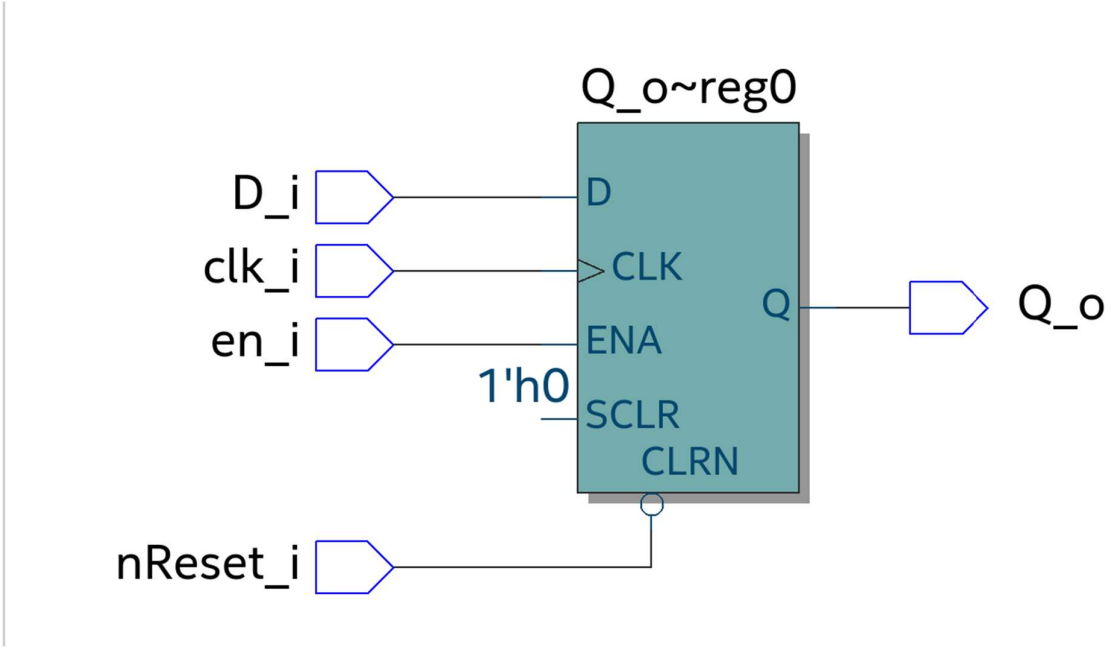


Log simulation

```
# vsim -voptargs=""+acc"" work.dff_ar_tb
# Start time: 16:32:40 on Nov 07,2019
# ** Note: (vsim-3812) Design is being optimized...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.dff_ar_tb(test_bench)#1
# Loading work.dff_ar(comport)#1
VSIM 26> run -all
# ** Note: >> Debut de la simulation
#    Time: 0 ns  Iteration: 0  Instance: /dff_ar_tb
# ** Note: >>Nombre d'erreur détectée = 0
#    Time: 552 ns  Iteration: 0  Instance: /dff_ar_tb
# ** Note: >>Fin de la simulation
#    Time: 552 ns  Iteration: 0  Instance: /dff_ar_tb
```

Dff_en

Vues RTL

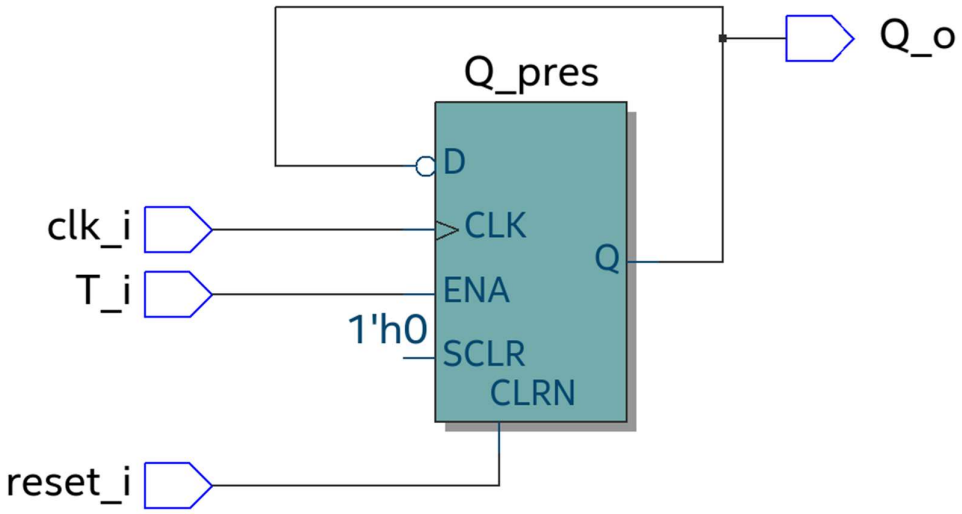


Log simulation

```
# Start time: 16:39:29 on Nov 07,2019
# ** Note: (vsim-3812) Design is being optimized...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.dff_en_tb(test_bench)#1
# Loading work.dff_en(comport)#1
VSIM 31> run -all
# ** Note: >> Debut de la simulation
#    Time: 0 ns  Iteration: 0  Instance: /dff_en_tb
# ** Note: >>Nombre d'erreur détectée = 0
#    Time: 652 ns  Iteration: 0  Instance: /dff_en_tb
# ** Note: >>Fin de la simulation
#    Time: 652 ns  Iteration: 0  Instance: /dff_en_tb
```

Flipflop_t

Vues RTL



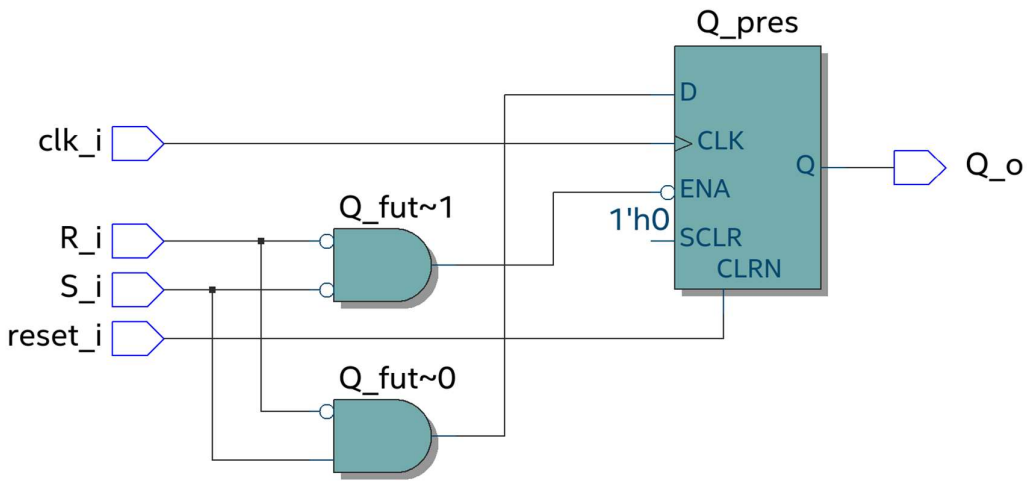
Log simulation

```
# vsim -voptargs=""+acc"" work.flipflop_t_tb
# Start time: 17:52:47 on Nov 07,2019
# ** Note: (vsim-3813) Design is being optimized due to module recompilation...
# Loading std.standard
# Loading std.textio(body)
# Loading ieee.std_logic_1164(body)
# Loading work.flipflop_t_tb(test_bench)#1
# Loading work.flipflop_t(comport)#1
VSIM 70> run -all
# ** Note: >> Debut de la simulation
#    Time: 0 ns  Iteration: 0  Instance: /flipflop_t_tb
# ** Note: >>Nombre d'erreur détectée = 0
#    Time: 652 ns  Iteration: 0  Instance: /flipflop_t_tb
# ** Note: >>Fin de la simulation
#    Time: 652 ns  Iteration: 0  Instance: /flipflop_t_tb

VSIM 71>
```

Flipflop_rs

Vues RTL



Date : le 9 novembre 2019

Nom de l'étudiant : Spinelli Isaia