```
// SPDX-License-Identifier: GPL-2.0+
/*
 * Copyright (C) 2012 Altera <www.altera.com>
 */

#include <dt-bindings/reset/altr,rst-mgr.h>

/ {
    #address-cells = <1>;
    #size-cells = <1>;

    aliases {
        serial0 = &uart0;
        serial1 = &uart1;
        timer0 = &timer0;
        timer1 = &timer1;
        timer2 = &timer2;
        timer3 = &timer3;
    };

    cpus {
        #address-cells = <1>;
        #size-cells = <0>;
        enable-method = "altr,socfpga-smp";

        cpu0: cpu@0 {
            compatible = "arm,cortex-a9";
            device_type = "cpu";
            reg = <0>;
            next-level-cache = <&L2>;
        };
        cpu1: cpu@1 {
            compatible = "arm,cortex-a9";
            device_type = "cpu";
            reg = <1>;
            next-level-cache = <&L2>;
        };
    };

    pmu: pmu@ff111000 {
        compatible = "arm,cortex-a9-pmu";
        interrupt-parent = <&intc>;
        interrupts = <0 176 4>, <0 177 4>;
        interrupt-affinity = <&cpu0>, <&cpu1>;
        reg = <0xff111000 0x1000>,
              <0xff113000 0x1000>;
    };

    intc: intc@fffed000 {
        compatible = "arm,cortex-a9-gic";
        #interrupt-cells = <3>;
        interrupt-controller;
        reg = <0xfffed000 0x1000>,
              <0xfffec100 0x100>;
    };

    soc {
        #address-cells = <1>;
        #size-cells = <1>;
        compatible = "simple-bus";
        device_type = "soc";
        interrupt-parent = <&intc>;
        ranges;

        amba {
            compatible = "simple-bus";
            #address-cells = <1>;
            #size-cells = <1>;
            ranges;
```

```
70
71              pdma: pdma@ffe01000 {
72                  compatible = "arm,pl330", "arm,primecell";
73                  reg = <0xffe01000 0x1000>;
74                  interrupts = <0 104 4>,
75                               <0 105 4>,
76                               <0 106 4>,
77                               <0 107 4>,
78                               <0 108 4>,
79                               <0 109 4>,
80                               <0 110 4>,
81                               <0 111 4>;
82                  #dma-cells = <1>;
83                  #dma-channels = <8>;
84                  #dma-requests = <32>;
85                  clocks = <&l4_main_clk>;
86                  clock-names = "apb_pclk";
87                  resets = <&rst DMA_RESET>;
88                  reset-names = "dma";
89              };
90          };
91
92          base_fpga_region {
93              compatible = "fpga-region";
94              fpga-mgr = <&fpgamgr0>;
95
96              #address-cells = <0x1>;
97              #size-cells = <0x1>;
98          };
99
100         can0: can@ffc00000 {
101             compatible = "bosch,d_can";
102             reg = <0xffc00000 0x1000>;
103             interrupts = <0 131 4>, <0 132 4>, <0 133 4>, <0 134 4>;
104             clocks = <&can0_clk>;
105             resets = <&rst CAN0_RESET>;
106             status = "disabled";
107         };
108
109         can1: can@ffc01000 {
110             compatible = "bosch,d_can";
111             reg = <0xffc01000 0x1000>;
112             interrupts = <0 135 4>, <0 136 4>, <0 137 4>, <0 138 4>;
113             clocks = <&can1_clk>;
114             resets = <&rst CAN1_RESET>;
115             status = "disabled";
116         };
117
118         clkmgr@ffd04000 {
119                 compatible = "altr,clk-mgr";
120                 reg = <0xffd04000 0x1000>;
121
122                 clocks {
123                     #address-cells = <1>;
124                     #size-cells = <0>;
125
126                     osc1: osc1 {
127                         #clock-cells = <0>;
128                         compatible = "fixed-clock";
129                     };
130
131                     osc2: osc2 {
132                         #clock-cells = <0>;
133                         compatible = "fixed-clock";
134                     };
135
136                     f2s_periph_ref_clk: f2s_periph_ref_clk {
137                         #clock-cells = <0>;
138                         compatible = "fixed-clock";
```

```
                        };

                        f2s_sdram_ref_clk: f2s_sdram_ref_clk {
                            #clock-cells = <0>;
                            compatible = "fixed-clock";
                        };

                        main_pll: main_pll@40 {
                            #address-cells = <1>;
                            #size-cells = <0>;
                            #clock-cells = <0>;
                            compatible = "altr,socfpga-pll-clock";
                            clocks = <&osc1>;
                            reg = <0x40>;

                            mpuclk: mpuclk@48 {
                                #clock-cells = <0>;
                                compatible = "altr,socfpga-perip-clk";
                                clocks = <&main_pll>;
                                div-reg = <0xe0 0 9>;
                                reg = <0x48>;
                            };

                            mainclk: mainclk@4c {
                                #clock-cells = <0>;
                                compatible = "altr,socfpga-perip-clk";
                                clocks = <&main_pll>;
                                div-reg = <0xe4 0 9>;
                                reg = <0x4C>;
                            };

                            dbg_base_clk: dbg_base_clk@50 {
                                #clock-cells = <0>;
                                compatible = "altr,socfpga-perip-clk";
                                clocks = <&main_pll>, <&osc1>;
                                div-reg = <0xe8 0 9>;
                                reg = <0x50>;
                            };

                            main_qspi_clk: main_qspi_clk@54 {
                                #clock-cells = <0>;
                                compatible = "altr,socfpga-perip-clk";
                                clocks = <&main_pll>;
                                reg = <0x54>;
                            };

                            main_nand_sdmmc_clk: main_nand_sdmmc_clk@58 {
                                #clock-cells = <0>;
                                compatible = "altr,socfpga-perip-clk";
                                clocks = <&main_pll>;
                                reg = <0x58>;
                            };

                            cfg_h2f_usr0_clk: cfg_h2f_usr0_clk@5c {
                                #clock-cells = <0>;
                                compatible = "altr,socfpga-perip-clk";
                                clocks = <&main_pll>;
                                reg = <0x5C>;
                            };
                        };

                        periph_pll: periph_pll@80 {
                            #address-cells = <1>;
                            #size-cells = <0>;
                            #clock-cells = <0>;
                            compatible = "altr,socfpga-pll-clock";
                            clocks = <&osc1>, <&osc2>, <&f2s_periph_ref_clk>;
                            reg = <0x80>;

```

```
208                         emac0_clk: emac0_clk@88 {
209                             #clock-cells = <0>;
210                             compatible = "altr,socfpga-perip-clk";
211                             clocks = <&periph_pll>;
212                             reg = <0x88>;
213                         };
214
215                         emac1_clk: emac1_clk@8c {
216                             #clock-cells = <0>;
217                             compatible = "altr,socfpga-perip-clk";
218                             clocks = <&periph_pll>;
219                             reg = <0x8C>;
220                         };
221
222                         per_qspi_clk: per_qsi_clk@90 {
223                             #clock-cells = <0>;
224                             compatible = "altr,socfpga-perip-clk";
225                             clocks = <&periph_pll>;
226                             reg = <0x90>;
227                         };
228
229                         per_nand_mmc_clk: per_nand_mmc_clk@94 {
230                             #clock-cells = <0>;
231                             compatible = "altr,socfpga-perip-clk";
232                             clocks = <&periph_pll>;
233                             reg = <0x94>;
234                         };
235
236                         per_base_clk: per_base_clk@98 {
237                             #clock-cells = <0>;
238                             compatible = "altr,socfpga-perip-clk";
239                             clocks = <&periph_pll>;
240                             reg = <0x98>;
241                         };
242
243                         h2f_usr1_clk: h2f_usr1_clk@9c {
244                             #clock-cells = <0>;
245                             compatible = "altr,socfpga-perip-clk";
246                             clocks = <&periph_pll>;
247                             reg = <0x9C>;
248                         };
249                     };
250
251                     sdram_pll: sdram_pll@c0 {
252                         #address-cells = <1>;
253                         #size-cells = <0>;
254                         #clock-cells = <0>;
255                         compatible = "altr,socfpga-pll-clock";
256                         clocks = <&osc1>, <&osc2>, <&f2s_sdram_ref_clk>;
257                         reg = <0xC0>;
258
259                         ddr_dqs_clk: ddr_dqs_clk@c8 {
260                             #clock-cells = <0>;
261                             compatible = "altr,socfpga-perip-clk";
262                             clocks = <&sdram_pll>;
263                             reg = <0xC8>;
264                         };
265
266                         ddr_2x_dqs_clk: ddr_2x_dqs_clk@cc {
267                             #clock-cells = <0>;
268                             compatible = "altr,socfpga-perip-clk";
269                             clocks = <&sdram_pll>;
270                             reg = <0xCC>;
271                         };
272
273                         ddr_dq_clk: ddr_dq_clk@d0 {
274                             #clock-cells = <0>;
275                             compatible = "altr,socfpga-perip-clk";
276                             clocks = <&sdram_pll>;
```

```
277                         reg = <0xD0>;
278                     };
279
280                     h2f_usr2_clk: h2f_usr2_clk@d4 {
281                         #clock-cells = <0>;
282                         compatible = "altr,socfpga-perip-clk";
283                         clocks = <&sdram_pll>;
284                         reg = <0xD4>;
285                     };
286                 };
287
288                 mpu_periph_clk: mpu_periph_clk {
289                     #clock-cells = <0>;
290                     compatible = "altr,socfpga-perip-clk";
291                     clocks = <&mpuclk>;
292                     fixed-divider = <4>;
293                 };
294
295                 mpu_l2_ram_clk: mpu_l2_ram_clk {
296                     #clock-cells = <0>;
297                     compatible = "altr,socfpga-perip-clk";
298                     clocks = <&mpuclk>;
299                     fixed-divider = <2>;
300                 };
301
302                 l4_main_clk: l4_main_clk {
303                     #clock-cells = <0>;
304                     compatible = "altr,socfpga-gate-clk";
305                     clocks = <&mainclk>;
306                     clk-gate = <0x60 0>;
307                 };
308
309                 l3_main_clk: l3_main_clk {
310                     #clock-cells = <0>;
311                     compatible = "altr,socfpga-perip-clk";
312                     clocks = <&mainclk>;
313                     fixed-divider = <1>;
314                 };
315
316                 l3_mp_clk: l3_mp_clk {
317                     #clock-cells = <0>;
318                     compatible = "altr,socfpga-gate-clk";
319                     clocks = <&mainclk>;
320                     div-reg = <0x64 0 2>;
321                     clk-gate = <0x60 1>;
322                 };
323
324                 l3_sp_clk: l3_sp_clk {
325                     #clock-cells = <0>;
326                     compatible = "altr,socfpga-gate-clk";
327                     clocks = <&l3_mp_clk>;
328                     div-reg = <0x64 2 2>;
329                 };
330
331                 l4_mp_clk: l4_mp_clk {
332                     #clock-cells = <0>;
333                     compatible = "altr,socfpga-gate-clk";
334                     clocks = <&mainclk>, <&per_base_clk>;
335                     div-reg = <0x64 4 3>;
336                     clk-gate = <0x60 2>;
337                 };
338
339                 l4_sp_clk: l4_sp_clk {
340                     #clock-cells = <0>;
341                     compatible = "altr,socfpga-gate-clk";
342                     clocks = <&mainclk>, <&per_base_clk>;
343                     div-reg = <0x64 7 3>;
344                     clk-gate = <0x60 3>;
345                 };
```

```
346
347                     dbg_at_clk: dbg_at_clk {
348                         #clock-cells = <0>;
349                         compatible = "altr,socfpga-gate-clk";
350                         clocks = <&dbg_base_clk>;
351                         div-reg = <0x68 0 2>;
352                         clk-gate = <0x60 4>;
353                     };
354
355                     dbg_clk: dbg_clk {
356                         #clock-cells = <0>;
357                         compatible = "altr,socfpga-gate-clk";
358                         clocks = <&dbg_at_clk>;
359                         div-reg = <0x68 2 2>;
360                         clk-gate = <0x60 5>;
361                     };
362
363                     dbg_trace_clk: dbg_trace_clk {
364                         #clock-cells = <0>;
365                         compatible = "altr,socfpga-gate-clk";
366                         clocks = <&dbg_base_clk>;
367                         div-reg = <0x6C 0 3>;
368                         clk-gate = <0x60 6>;
369                     };
370
371                     dbg_timer_clk: dbg_timer_clk {
372                         #clock-cells = <0>;
373                         compatible = "altr,socfpga-gate-clk";
374                         clocks = <&dbg_base_clk>;
375                         clk-gate = <0x60 7>;
376                     };
377
378                     cfg_clk: cfg_clk {
379                         #clock-cells = <0>;
380                         compatible = "altr,socfpga-gate-clk";
381                         clocks = <&cfg_h2f_usr0_clk>;
382                         clk-gate = <0x60 8>;
383                     };
384
385                     h2f_user0_clk: h2f_user0_clk {
386                         #clock-cells = <0>;
387                         compatible = "altr,socfpga-gate-clk";
388                         clocks = <&cfg_h2f_usr0_clk>;
389                         clk-gate = <0x60 9>;
390                     };
391
392                     emac_0_clk: emac_0_clk {
393                         #clock-cells = <0>;
394                         compatible = "altr,socfpga-gate-clk";
395                         clocks = <&emac0_clk>;
396                         clk-gate = <0xa0 0>;
397                     };
398
399                     emac_1_clk: emac_1_clk {
400                         #clock-cells = <0>;
401                         compatible = "altr,socfpga-gate-clk";
402                         clocks = <&emac1_clk>;
403                         clk-gate = <0xa0 1>;
404                     };
405
406                     usb_mp_clk: usb_mp_clk {
407                         #clock-cells = <0>;
408                         compatible = "altr,socfpga-gate-clk";
409                         clocks = <&per_base_clk>;
410                         clk-gate = <0xa0 2>;
411                         div-reg = <0xa4 0 3>;
412                     };
413
414                     spi_m_clk: spi_m_clk {
```

```
415                         #clock-cells = <0>;
416                         compatible = "altr,socfpga-gate-clk";
417                         clocks = <&per_base_clk>;
418                         clk-gate = <0xa0 3>;
419                         div-reg = <0xa4 3 3>;
420                     };
421
422                     can0_clk: can0_clk {
423                         #clock-cells = <0>;
424                         compatible = "altr,socfpga-gate-clk";
425                         clocks = <&per_base_clk>;
426                         clk-gate = <0xa0 4>;
427                         div-reg = <0xa4 6 3>;
428                     };
429
430                     can1_clk: can1_clk {
431                         #clock-cells = <0>;
432                         compatible = "altr,socfpga-gate-clk";
433                         clocks = <&per_base_clk>;
434                         clk-gate = <0xa0 5>;
435                         div-reg = <0xa4 9 3>;
436                     };
437
438                     gpio_db_clk: gpio_db_clk {
439                         #clock-cells = <0>;
440                         compatible = "altr,socfpga-gate-clk";
441                         clocks = <&per_base_clk>;
442                         clk-gate = <0xa0 6>;
443                         div-reg = <0xa8 0 24>;
444                     };
445
446                     h2f_user1_clk: h2f_user1_clk {
447                         #clock-cells = <0>;
448                         compatible = "altr,socfpga-gate-clk";
449                         clocks = <&h2f_usr1_clk>;
450                         clk-gate = <0xa0 7>;
451                     };
452
453                     sdmmc_clk: sdmmc_clk {
454                         #clock-cells = <0>;
455                         compatible = "altr,socfpga-gate-clk";
456                         clocks = <&f2s_periph_ref_clk>, <&main_nand_sdmmc_clk>,
                         <&per_nand_mmc_clk>;
457                         clk-gate = <0xa0 8>;
458                         clk-phase = <0 135>;
459                     };
460
461                     sdmmc_clk_divided: sdmmc_clk_divided {
462                         #clock-cells = <0>;
463                         compatible = "altr,socfpga-gate-clk";
464                         clocks = <&sdmmc_clk>;
465                         clk-gate = <0xa0 8>;
466                         fixed-divider = <4>;
467                     };
468
469                     nand_x_clk: nand_x_clk {
470                         #clock-cells = <0>;
471                         compatible = "altr,socfpga-gate-clk";
472                         clocks = <&f2s_periph_ref_clk>, <&main_nand_sdmmc_clk>,
                         <&per_nand_mmc_clk>;
473                         clk-gate = <0xa0 9>;
474                     };
475
476                     nand_ecc_clk: nand_ecc_clk {
477                         #clock-cells = <0>;
478                         compatible = "altr,socfpga-gate-clk";
479                         clocks = <&nand_x_clk>;
480                         clk-gate = <0xa0 9>;
481                     };
```

```
482
483                     nand_clk: nand_clk {
484                         #clock-cells = <0>;
485                         compatible = "altr,socfpga-gate-clk";
486                         clocks = <&nand_x_clk>;
487                         clk-gate = <0xa0 10>;
488                         fixed-divider = <4>;
489                     };
490
491                     qspi_clk: qspi_clk {
492                         #clock-cells = <0>;
493                         compatible = "altr,socfpga-gate-clk";
494                         clocks = <&f2s_periph_ref_clk>, <&main_qspi_clk>,
                        <&per_qspi_clk>;
495                         clk-gate = <0xa0 11>;
496                     };
497
498                     ddr_dqs_clk_gate: ddr_dqs_clk_gate {
499                         #clock-cells = <0>;
500                         compatible = "altr,socfpga-gate-clk";
501                         clocks = <&ddr_dqs_clk>;
502                         clk-gate = <0xd8 0>;
503                     };
504
505                     ddr_2x_dqs_clk_gate: ddr_2x_dqs_clk_gate {
506                         #clock-cells = <0>;
507                         compatible = "altr,socfpga-gate-clk";
508                         clocks = <&ddr_2x_dqs_clk>;
509                         clk-gate = <0xd8 1>;
510                     };
511
512                     ddr_dq_clk_gate: ddr_dq_clk_gate {
513                         #clock-cells = <0>;
514                         compatible = "altr,socfpga-gate-clk";
515                         clocks = <&ddr_dq_clk>;
516                         clk-gate = <0xd8 2>;
517                     };
518
519                     h2f_user2_clk: h2f_user2_clk {
520                         #clock-cells = <0>;
521                         compatible = "altr,socfpga-gate-clk";
522                         clocks = <&h2f_usr2_clk>;
523                         clk-gate = <0xd8 3>;
524                     };
525
526                 };
527             };
528
529             fpga_bridge0: fpga_bridge@ff200000 {
530                 compatible = "altr,socfpga-lwhps2fpga-bridge";
531                 reg = <0xff200000 0x200000>;
532                 resets = <&rst LWHPS2FPGA_RESET>;
533                 clocks = <&l4_main_clk>;
534             };
535
536             fpga_bridge1: fpga_bridge@ff500000 {
537                 compatible = "altr,socfpga-hps2fpga-bridge";
538                 reg = <0xff500000 0x10000>;
539                 resets = <&rst HPS2FPGA_RESET>;
540                 clocks = <&l4_main_clk>;
541             };
542
543             fpgamgr0: fpgamgr@ff706000 {
544                 compatible = "altr,socfpga-fpga-mgr";
545                 reg = <0xff706000 0x1000
546                        0xffb90000 0x4>;
547                 interrupts = <0 175 4>;
548             };
549
```

```
550             gmac0: ethernet@ff700000 {
551                 compatible = "altr,socfpga-stmmac", "snps,dwmac-3.70a", "snps,dwmac";
552                 altr,sysmgr-syscon = <&sysmgr 0x60 0>;
553                 reg = <0xff700000 0x2000>;
554                 interrupts = <0 115 4>;
555                 interrupt-names = "macirq";
556                 mac-address = [00 00 00 00 00 00];/* Filled in by U-Boot */
557                 clocks = <&emac_0_clk>;
558                 clock-names = "stmmaceth";
559                 resets = <&rst EMAC0_RESET>;
560                 reset-names = "stmmaceth";
561                 snps,multicast-filter-bins = <256>;
562                 snps,perfect-filter-entries = <128>;
563                 tx-fifo-depth = <4096>;
564                 rx-fifo-depth = <4096>;
565                 status = "disabled";
566             };
567
568             gmac1: ethernet@ff702000 {
569                 compatible = "altr,socfpga-stmmac", "snps,dwmac-3.70a", "snps,dwmac";
570                 altr,sysmgr-syscon = <&sysmgr 0x60 2>;
571                 reg = <0xff702000 0x2000>;
572                 interrupts = <0 120 4>;
573                 interrupt-names = "macirq";
574                 mac-address = [00 00 00 00 00 00];/* Filled in by U-Boot */
575                 clocks = <&emac_1_clk>;
576                 clock-names = "stmmaceth";
577                 resets = <&rst EMAC1_RESET>;
578                 reset-names = "stmmaceth";
579                 snps,multicast-filter-bins = <256>;
580                 snps,perfect-filter-entries = <128>;
581                 tx-fifo-depth = <4096>;
582                 rx-fifo-depth = <4096>;
583                 status = "disabled";
584             };
585
586             gpio0: gpio@ff708000 {
587                 #address-cells = <1>;
588                 #size-cells = <0>;
589                 compatible = "snps,dw-apb-gpio";
590                 reg = <0xff708000 0x1000>;
591                 clocks = <&l4_mp_clk>;
592                 resets = <&rst GPIO0_RESET>;
593                 status = "disabled";
594
595                 porta: gpio-controller@0 {
596                     compatible = "snps,dw-apb-gpio-port";
597                     gpio-controller;
598                     #gpio-cells = <2>;
599                     snps,nr-gpios = <29>;
600                     reg = <0>;
601                     interrupt-controller;
602                     #interrupt-cells = <2>;
603                     interrupts = <0 164 4>;
604                 };
605             };
606
607             gpio1: gpio@ff709000 {
608                 #address-cells = <1>;
609                 #size-cells = <0>;
610                 compatible = "snps,dw-apb-gpio";
611                 reg = <0xff709000 0x1000>;
612                 clocks = <&l4_mp_clk>;
613                 resets = <&rst GPIO1_RESET>;
614                 status = "disabled";
615
616                 portb: gpio-controller@0 {
617                     compatible = "snps,dw-apb-gpio-port";
618                     gpio-controller;
```

```
619                 #gpio-cells = <2>;
620                 snps,nr-gpios = <29>;
621                 reg = <0>;
622                 interrupt-controller;
623                 #interrupt-cells = <2>;
624                 interrupts = <0 165 4>;
625             };
626         };
627
628         gpio2: gpio@ff70a000 {
629             #address-cells = <1>;
630             #size-cells = <0>;
631             compatible = "snps,dw-apb-gpio";
632             reg = <0xff70a000 0x1000>;
633             clocks = <&l4_mp_clk>;
634             resets = <&rst GPIO2_RESET>;
635             status = "disabled";
636
637             portc: gpio-controller@0 {
638                 compatible = "snps,dw-apb-gpio-port";
639                 gpio-controller;
640                 #gpio-cells = <2>;
641                 snps,nr-gpios = <27>;
642                 reg = <0>;
643                 interrupt-controller;
644                 #interrupt-cells = <2>;
645                 interrupts = <0 166 4>;
646             };
647         };
648
649         i2c0: i2c@ffc04000 {
650             #address-cells = <1>;
651             #size-cells = <0>;
652             compatible = "snps,designware-i2c";
653             reg = <0xffc04000 0x1000>;
654             resets = <&rst I2C0_RESET>;
655             clocks = <&l4_sp_clk>;
656             interrupts = <0 158 0x4>;
657             status = "disabled";
658         };
659
660         i2c1: i2c@ffc05000 {
661             #address-cells = <1>;
662             #size-cells = <0>;
663             compatible = "snps,designware-i2c";
664             reg = <0xffc05000 0x1000>;
665             resets = <&rst I2C1_RESET>;
666             clocks = <&l4_sp_clk>;
667             interrupts = <0 159 0x4>;
668             status = "disabled";
669         };
670
671         i2c2: i2c@ffc06000 {
672             #address-cells = <1>;
673             #size-cells = <0>;
674             compatible = "snps,designware-i2c";
675             reg = <0xffc06000 0x1000>;
676             resets = <&rst I2C2_RESET>;
677             clocks = <&l4_sp_clk>;
678             interrupts = <0 160 0x4>;
679             status = "disabled";
680         };
681
682         i2c3: i2c@ffc07000 {
683             #address-cells = <1>;
684             #size-cells = <0>;
685             compatible = "snps,designware-i2c";
686             reg = <0xffc07000 0x1000>;
687             resets = <&rst I2C3_RESET>;
```

```
            clocks = <&l4_sp_clk>;
            interrupts = <0 161 0x4>;
            status = "disabled";
        };

        eccmgr: eccmgr {
            compatible = "altr,socfpga-ecc-manager";
            #address-cells = <1>;
            #size-cells = <1>;
            ranges;

            l2-ecc@ffd08140 {
                compatible = "altr,socfpga-l2-ecc";
                reg = <0xffd08140 0x4>;
                interrupts = <0 36 1>, <0 37 1>;
            };

            ocram-ecc@ffd08144 {
                compatible = "altr,socfpga-ocram-ecc";
                reg = <0xffd08144 0x4>;
                iram = <&ocram>;
                interrupts = <0 178 1>, <0 179 1>;
            };
        };

        L2: l2-cache@fffef000 {
            compatible = "arm,pl310-cache";
            reg = <0xfffef000 0x1000>;
            interrupts = <0 38 0x04>;
            cache-unified;
            cache-level = <2>;
            arm,tag-latency = <1 1 1>;
            arm,data-latency = <2 1 1>;
            prefetch-data = <1>;
            prefetch-instr = <1>;
            arm,shared-override;
            arm,double-linefill = <1>;
            arm,double-linefill-incr = <0>;
            arm,double-linefill-wrap = <1>;
            arm,prefetch-drop = <0>;
            arm,prefetch-offset = <7>;
        };

        l3regs@0xff800000 {
            compatible = "altr,l3regs", "syscon";
            reg = <0xff800000 0x1000>;
        };

        mmc: dwmmc0@ff704000 {
            compatible = "altr,socfpga-dw-mshc";
            reg = <0xff704000 0x1000>;
            interrupts = <0 139 4>;
            fifo-depth = <0x400>;
            #address-cells = <1>;
            #size-cells = <0>;
            clocks = <&l4_mp_clk>, <&sdmmc_clk_divided>;
            clock-names = "biu", "ciu";
            resets = <&rst SDMMC_RESET>;
            status = "disabled";
        };

        nand0: nand@ff900000 {
            #address-cells = <0x1>;
            #size-cells = <0x0>;
            compatible = "altr,socfpga-denali-nand";
            reg = <0xff900000 0x100000>,
                  <0xffb80000 0x10000>;
            reg-names = "nand_data", "denali_reg";
            interrupts = <0x0 0x90 0x4>;
```

```
            clocks = <&nand_clk>, <&nand_x_clk>, <&nand_ecc_clk>;
            clock-names = "nand", "nand_x", "ecc";
            resets = <&rst NAND_RESET>;
            status = "disabled";
        };

        ocram: sram@ffff0000 {
            compatible = "mmio-sram";
            reg = <0xffff0000 0x10000>;
        };

        qspi: spi@ff705000 {
            compatible = "cdns,qspi-nor";
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <0xff705000 0x1000>,
                  <0xffa00000 0x1000>;
            interrupts = <0 151 4>;
            cdns,fifo-depth = <128>;
            cdns,fifo-width = <4>;
            cdns,trigger-address = <0x00000000>;
            clocks = <&qspi_clk>;
            resets = <&rst QSPI_RESET>;
            status = "disabled";
        };

        rst: rstmgr@ffd05000 {
            #reset-cells = <1>;
            compatible = "altr,rst-mgr";
            reg = <0xffd05000 0x1000>;
            altr,modrst-offset = <0x10>;
        };

        scu: snoop-control-unit@fffec000 {
            compatible = "arm,cortex-a9-scu";
            reg = <0xfffec000 0x100>;
        };

        sdr: sdr@ffc25000 {
            compatible = "altr,sdr-ctl", "syscon";
            reg = <0xffc25000 0x1000>;
            resets = <&rst SDR_RESET>;
        };

        sdramedac {
            compatible = "altr,sdram-edac";
            altr,sdr-syscon = <&sdr>;
            interrupts = <0 39 4>;
        };

        spi0: spi@fff00000 {
            compatible = "snps,dw-apb-ssi";
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <0xfff00000 0x1000>;
            interrupts = <0 154 4>;
            num-cs = <4>;
            clocks = <&spi_m_clk>;
            resets = <&rst SPIM0_RESET>;
            status = "disabled";
        };

        spi1: spi@fff01000 {
            compatible = "snps,dw-apb-ssi";
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <0xfff01000 0x1000>;
            interrupts = <0 155 4>;
            num-cs = <4>;
```

```
826             clocks = <&spi_m_clk>;
827             resets = <&rst SPIM1_RESET>;
828             status = "disabled";
829         };
830
831         sysmgr: sysmgr@ffd08000 {
832             compatible = "altr,sys-mgr", "syscon";
833             reg = <0xffd08000 0x4000>;
834         };
835
836         /* Local timer */
837         timer@fffec600 {
838             compatible = "arm,cortex-a9-twd-timer";
839             reg = <0xfffec600 0x100>;
840             interrupts = <1 13 0xf01>;
841             clocks = <&mpu_periph_clk>;
842         };
843
844         timer0: timer0@ffc08000 {
845             compatible = "snps,dw-apb-timer";
846             interrupts = <0 167 4>;
847             reg = <0xffc08000 0x1000>;
848             clocks = <&l4_sp_clk>;
849             clock-names = "timer";
850             resets = <&rst SPTIMER0_RESET>;
851             reset-names = "timer";
852         };
853
854         timer1: timer1@ffc09000 {
855             compatible = "snps,dw-apb-timer";
856             interrupts = <0 168 4>;
857             reg = <0xffc09000 0x1000>;
858             clocks = <&l4_sp_clk>;
859             clock-names = "timer";
860             resets = <&rst SPTIMER1_RESET>;
861             reset-names = "timer";
862         };
863
864         timer2: timer2@ffd00000 {
865             compatible = "snps,dw-apb-timer";
866             interrupts = <0 169 4>;
867             reg = <0xffd00000 0x1000>;
868             clocks = <&osc1>;
869             clock-names = "timer";
870             resets = <&rst OSC1TIMER0_RESET>;
871             reset-names = "timer";
872         };
873
874         timer3: timer3@ffd01000 {
875             compatible = "snps,dw-apb-timer";
876             interrupts = <0 170 4>;
877             reg = <0xffd01000 0x1000>;
878             clocks = <&osc1>;
879             clock-names = "timer";
880             resets = <&rst OSC1TIMER1_RESET>;
881             reset-names = "timer";
882         };
883
884         uart0: serial0@ffc02000 {
885             compatible = "snps,dw-apb-uart";
886             reg = <0xffc02000 0x1000>;
887             interrupts = <0 162 4>;
888             reg-shift = <2>;
889             reg-io-width = <4>;
890             clocks = <&l4_sp_clk>;
891             dmas = <&pdma 28>,
892                    <&pdma 29>;
893             dma-names = "tx", "rx";
894             resets = <&rst UART0_RESET>;
```

```
        };

        uart1: serial1@ffc03000 {
            compatible = "snps,dw-apb-uart";
            reg = <0xffc03000 0x1000>;
            interrupts = <0 163 4>;
            reg-shift = <2>;
            reg-io-width = <4>;
            clocks = <&l4_sp_clk>;
            dmas = <&pdma 30>,
                   <&pdma 31>;
            dma-names = "tx", "rx";
            resets = <&rst UART1_RESET>;
        };

        usbphy0: usbphy {
            #phy-cells = <0>;
            compatible = "usb-nop-xceiv";
            status = "okay";
        };

        usb0: usb@ffb00000 {
            compatible = "snps,dwc2";
            reg = <0xffb00000 0xffff>;
            interrupts = <0 125 4>;
            clocks = <&usb_mp_clk>;
            clock-names = "otg";
            resets = <&rst USB0_RESET>;
            reset-names = "dwc2";
            phys = <&usbphy0>;
            phy-names = "usb2-phy";
            status = "disabled";
        };

        usb1: usb@ffb40000 {
            compatible = "snps,dwc2";
            reg = <0xffb40000 0xffff>;
            interrupts = <0 128 4>;
            clocks = <&usb_mp_clk>;
            clock-names = "otg";
            resets = <&rst USB1_RESET>;
            reset-names = "dwc2";
            phys = <&usbphy0>;
            phy-names = "usb2-phy";
            status = "disabled";
        };

        watchdog0: watchdog@ffd02000 {
            compatible = "snps,dw-wdt";
            reg = <0xffd02000 0x1000>;
            interrupts = <0 171 4>;
            clocks = <&osc1>;
            resets = <&rst L4WD0_RESET>;
            status = "disabled";
        };

        watchdog1: watchdog@ffd03000 {
            compatible = "snps,dw-wdt";
            reg = <0xffd03000 0x1000>;
            interrupts = <0 172 4>;
            clocks = <&osc1>;
            resets = <&rst L4WD1_RESET>;
            status = "disabled";
        };
    };
};
```