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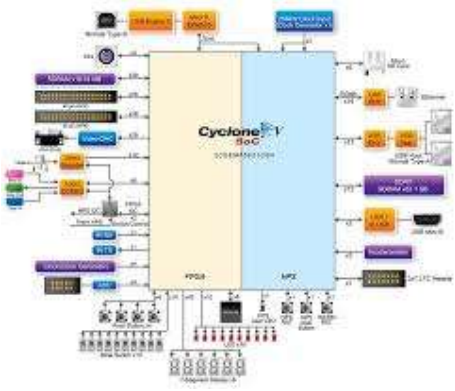
Digital Systems

Porter Linux sur la DE-1

SYSTÈME SOC INTÉGRÉ AVEC FPGA (SOCF)



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Introduction

Ce laboratoire a pour but d'apprendre comment partitionner une carte SD, compiler et démarrer Linux. Un bitstream « DE1_SoC_top.sof » nous a été fourni.

Génération de la carte SD

Le but de cette étape est de récupérer une image SD officiel pour la DE1-SoC « Linux console » de Teraisc afin de la copier sur une carte SD et de démarrer correctement la DE1 avec cette carte SD.

Préambule

Le firmware du HPS est capable de démarrer depuis une carte SD. Il s'attend à trouver le SPL sur une partition contenant l'identificateur 0xA2. Cette partition peut se trouver n'importe où. Le reste peut être partitionné n'importe comment. L'exemple suivant comprend

- Une partition 0xA2 contenant le SPL et U-Boot.
- Une partition FAT32 contient le kernel Linux (zImage), le device tree (dtb) et le bitstream (rbf).
- Une partition ext4 contient le rootfs utilisé par Linux.

```
# fdisk -lu /dev/sdX
Disk /dev/sdX: 7948 MB, 7948206080 bytes
245 heads, 62 sectors/track, 1021 cylinders, total 15523840 sectors
Units = sectors of 1 * 512 = 512 bytes
```

Device Boot	Start	End	Blocks	Id	System
/dev/sdX1	62	167089	83514	b	W95 FAT32
/dev/sdX2	167090	182279	7595	a2	Unknown
/dev/sdX3	182280	15508989	7663355	83	Linux

Figure 0-1 : Exemple de partition

Il existe de la documentation et un référence design pour la carte DE-1. Il sera possible de récupérer une image de carte SD. Ceci permet d'avoir une base de travail stable et nous épargnera la création des partitions avec fdisk, la compilation de U-Boot et la création du rootfs avec Buildroot. Ce référence design étant vieux (Linux 3.12), il faudra donc recompiler et mettre à jour une version récente du kernel.

Manipulations

Pour commencer, il faut télécharger l'image de la carte SD « Linux console » de Teraisc que j'ai trouvé directement sur le site de Teraisc : https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=836&PartNo=4

Une fois que le fichier ZIP est téléchargé, il faut l'extraire.

Ensuite, il faut brancher la carte SD sur laquelle on souhaite mettre l'image « Linux console ». Il faut trouver quel device correspond à la carte avec l'aide de la commande « sudo fdisk -l ». Comme par exemple /dev/sdd.

Une fois que ceci est fait, il faut copier l'image binaire précédemment extrait du fichier ZIP sur le périphérique préalablement trouvé (carte SD). Il est possible de faire ceci avec la commande « dd ». Voici par exemple la commande que j'ai effectuée :

dd bs=4M if=DE1_SoC_SD.img of=/dev/sdd conv=fsync

Vérification

Maintenant que la carte SD contient l'image « Linux console » de Teraisc, nous pouvons vérifier que la carte DE1-SoC démarre correctement. Pour ce faire :

1. Insérer la carte SD dans le support de la carte DE1
2. Brancher une câble USB entre la board et l'ordinateur
3. Utiliser la commande « picocom » (baudrate de 115200) sur le device USB afin d'observer les logs. Exemple : **sudo picocom -b 115200 /dev/ttyUSB0**
4. Allumer la carte DE1-SoC

On peut observer que la carte démarre bien et nous propose de se loger :

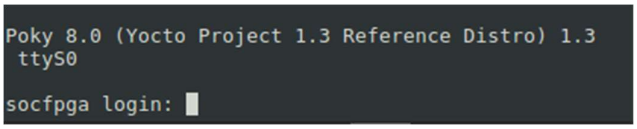

Figure 0-2 : affichage du login

On est donc sûr que le démarrage s'effectue correctement.

Compilation de Linux

Le but de cette étape est de récupérer linux mainline, de le compiler et d'utiliser la nouvelle image linux sur la carte SD.

Préambule

Depuis 2018, les FPGA-SoC sont supporté dans le linux mainline, contrairement à avant où Altera maintenait sa propre version pour ses FPGA-SoC.

Il est possible de trouver les sources sur Github : https://github.com/torvalds/linux/tree/master.

Il existe une configuration du noyau pour tous les SoC FPGA. Le kernel n'est donc pas dépendant de la board utilisée ou de la famille du SoC (ceci est géré dans le device tree).

Manipulations

Il faut commencer par récupérer linux mainline en faisant un clone du repo git ou en téléchargeant directement le repo.

Une fois dans le dossier de linux, il faut configurer et compiler le noyau pour ARM. Pour ce faire, une toolchain ARM est nécessaire. Dans mon cas, elle se trouve sur la machine dans /opt.

Pour configurer le noyau, il faut commencer par exécuter cette commande « make ARCH=arm CROSS_COMPILE=<TOOLCHAIN_DIR>/bin/arm-linux-gnueabihf- socfpga_defconfig ». Pour ma part, voici la commande utilisé :

make ARCH=arm CROSS_COMPILE=/opt/toolchain/gcc-linaro-arm-linux-gnueabihf-4.7-2013.04-20130415_linux/bin/arm-linux-gnueabihf- socfpga_defconfig

Une fois ceci fait, il est possible de compiler le noyau à l'aide de cette commande « make ARCH=arm CROSS_COMPILE=/bin/arm-linux-gnueabihf- -j8 ». Voici la commande que j'ai exécuté :

make ARCH=arm CROSS_COMPILE=/opt/toolchain/gcc-linaro-arm-linux-gnueabihf-4.7-2013.04-20130415_linux/bin/arm-linux-gnueabihf- -j8

Maintenant que le noyau est correctement compilé, un nouveau fichier « zImage » a été généré dans « linux/arch/arm/boot ». Il faut mettre à jour ce fichier dans la carte SD. Personnellement, j'ai simplement glissé le zImage dans la bonne partition :

Figure 0-1 : Mise à jour du fichier zImage

Vérification

Maintenant que l'image du linux a été mise à jour sur la carte SD, une vérification peut être faite. Cette étape consiste aux mêmes opérations que la vérification du chapitre précédent. Cependant, le résultat ne doit plus être une demande de login mais le boot doit échouer pendant l'initialisation du kernel. Il doit être possible de voir des logs qui doit ressembler à ceci :

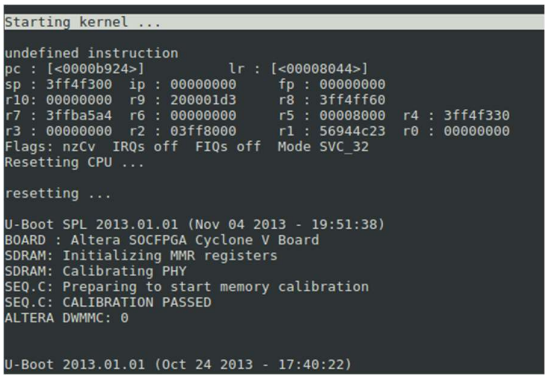

Figure 0-2 : Echec du boot

Création du Device Tree

Le but de cette étape est de créer un device tree correspondant à la DE1-SoC afin de démarrer correctement jusqu'au login.

Préambule

Le device tree décrit les composants présents dans le SoC et sur la carte. Le kernel met à disposition des dtsi à inclure dans votre device tree. Ces dtsi décrivent les principales familles de SoC (Cyclone V, Aria V, Aria 10, Stratix 10, etc.).

Il nous reste qu'à activer et configurer les principaux composants présents sur la DE-1. Un conseil que l'on rencontre souvent lorsque l'on désire porter une carte sur Linux ou U-Boot est de partir d'une carte similaire déjà supportée. Un device tree pour la DE-0 est déjà présent dans les sources du kernel, nous allons l'utiliser comme point de départ. Le device tree doit être compilé.

Manipulations

La première étape est de trouver le device tree pour la DE-0 afin d'avoir un bon point de départ. Voici la commande que j'ai utilisée afin de trouver rapidement le device tree :

```
redsuser@reds-eda:~/Desktop/linux$ sudo find . -iname *DE0*.dts
./arch/arm/boot/dts/socfpga_cyclone5_de0_nano_soc.dts
```

Figure 0-1 : Commande de recherche

Ensuite, il faut copier ce device tree sous un nouveau nom afin de crée le device tree pour la DE1 :

```
redsuser@reds-eda:~/Desktop/linux/arch/arm/boot/dts$ cp socfpga_cyclone5_de0_nano_soc.dts socfpga_cyclone5_de1.dts
```

Figure 0-2 : Commande de copie

Après avoir analysé complètement le device tree, j'ai pu enlever les nœuds gpio1, gpio2, gpio3 et le nœud i2c0. Ensuite, il faut corriger l'adresse de base du bridge lightweight dans le fichier source socfpga.dtsi comme ceci :

```
fpga_bridge0: fpga_bridge@ff200000 {
        compatible = "altr,socfpga-lwhps2fpga-bridge";
        reg = <0xff200000 0x200000>;
        resets = <&rst LWHPS2FPGA_RESET>;
        clocks = <&l4_main_clk>;
};
```

Figure 0-3 : Noeud du bridge lightweight

Maintenant que le device est compatible avec la board DE1, il faut compiler le device tree avec le nom donné au nouveau fichier :

```
redsuser@reds-eda:~/Desktop/linux$ make ARCH=arm CROSS_COMPILE=/opt/toolchain/gcc-linaro-arm-linux-gnueabihf-4.7-2013.04-20130415_linux/bin/arm-linux-gnueabihf- socfpga_cyclone5_de1.dtb
  UPD     include/config/kernel.release
  DTC     arch/arm/boot/dts/socfpga_cyclone5_de1.dtb
```

Figure 0-4 : Compilation du device tree

Une fois le device tree compilé, un fichier « arch/arm/boot/dts/<Nom_du_new_fichier>.dts » est créé. Il faut le copier sur la carte SD dans la partition FAT32 en le renommant « **socfpga.dtb** » afin d'écraser l'ancien device tree.

Vérification

Maintenant que le device tree a été mise à jour sur la carte SD, une vérification peut être faite. Cette étape consiste aux mêmes opérations que la vérification du premier chapitre. Le résultat devrait être un démarrage correcte de la carte avec un login.

Test du bridge HPS <-> FPGA

Le but de cette étape consiste à s'assurer que le bridge (lwhps2fpga) entre le HPS et la FPGA fonctionne correctement.

Préambule

Un mapping de la mémoire physique est accessible par le fichier /dev/mem. Il existe un utilitaire nommé devmem2 qui permet de lire et d'écrire dans ce fichier facilement.

Le code source de cet utilitaire est disponible sur Github :
https://github.com/hackndev/tools/blob/master/devmem2.c

Manipulations

Pour commencer, il est recommandé de s'assurer que le portage c'est correctement effectué. Pour ce faire, il faut observer les logs de démarrage du kernel grâce à la commande « dmesg ». Par exemple, les bridge doivent être correctement initialisés. Il doit être possible de voir ces messages :

```
1.540657] usbhid: USB HID core driver
1.544778] fpga_manager fpga0: Altera SOCFPGA FPGA Manager registered
1.551859] altera_hps2fpga_bridge ff200000.fpga_bridge: fpga bridge [lwhps2fpga] registered
1.560550] altera_hps2fpga_bridge ff500000.fpga_bridge: fpga bridge [hps2fpga] registered
```

Figure 0-1 : Dmesg - bridges

Ensuite, il faut charger le bitstream qu'a été fourni à l'aide de Quatus. Une fois le paramétrage correcte et le fichier de bitstream sélectionné, on peut commencer le chargement.

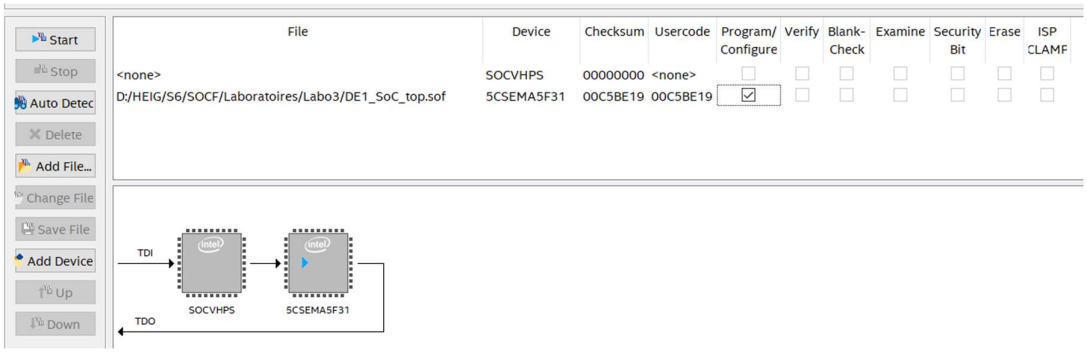

Figure 0-2 : Chargement du bitstream

Une fois le chargement terminé, il doit être possible de voir deux des 7 segments s'allumer comme ci-dessous :

Figure 0-3 : Validation du chargement

On peut maintenant avoir la confirmation que le chargement c'est correctement effectué.

Afin de profiter de l'utilitaire « devmeme2 », il faut commencer par le récupérer via le git précédemment indiqué. Ensuite, il faut le cross-compiler afin qu'il soit exécutable sur la board DE1.

Pour ce faire, il est nécessaire d'utiliser la toolchain précédemment évoquée. Voici la commande que j'ai effectué :

```
redsuser@reds-eda:~/Desktop/SOCF/Labo3/devmem2$ /opt/toolchain/gcc-linaro-arm-linux-gnueabihf-4.7-2013.04-20130415_linux/bin/arm-linux-gnueabihf-gcc devmem2.c -o devmem2
redsuser@reds-eda:~/Desktop/SOCF/Labo3/devmem2$ ls
devmem2  devmem2.c
```

Figure 0-4 : Cross-compilation

Maintenant que l'exécutable est prêt, il faut le placer dans le rootfs de la carte SD afin d'y avoir accès dans la DE1. Par exemple, on peut le mettre dans le dossier « /home/root/ ». Comme ceci :

Figure 0-5 : devmeme2 sur la carte SD

On peut voir que l'exécutable a été placé dans le dossier « /home/root/ ».

Vérification

Afin de vérifier le bon fonctionnement du bridge avec le nouvel utilitaire, on peut placer la carte SD, avec l'exécutable, dans la DE1 et la démarrer. Il faut ensuite se loger avec « root ». Il est maintenant possible de tester l'utilitaire afin de lire l'état des boutons poussoirs et des switches. Les boutons sont mappés sur le lwhps2fpga bridge à l'offset 0x30 et les switches à l'offset 0x20.

J'ai commencé par lire l'état des Keys en cliquant sur les 4 boutons :

```
root@socfpga:~# ./devmem2 0xff200030
/dev/mem opened.
Memory mapped at address 0xb6f7a000.
Value at address 0xFF200030 (0xb6f7a030): 0xF
root@socfpga:~#
```

Figure 0-6 : Lecture des keys

On peut voir que la valeur lue est bien 0xF.

Ensuite, j'ai lu l'état des switches avec un switch sur deux activés :

```
root@socfpga:~# ./devmem2 0xff200020
/dev/mem opened.
Memory mapped at address 0xb6f6c000.
Value at address 0xFF200020 (0xb6f6c020): 0x155
root@socfpga:~#
```

Figure 0-7 : Lecture des switches

On peut voir que la lecture c'est correctement effectuée.

Annexes

Voici la liste dans l'ordre des annexes :

1. socfpga_cyclone5_de1.dts
2. socfpga_cyclone5.dtsi
3. socfpga.dtsi
4. kernel.log

Conclusion

Difficultés rencontrées

- Pendant ce laboratoire, j'ai eu des problèmes avec ma carte SD. Elle est passé en mode « read only » après plusieurs changements de fichier. Pour résoudre le problème, j'ai dû recopier l'image binaire sur la carte SD.

Compétences acquises

- Amélioration de compréhension sur le fonctionnement global d'un système HPS FPGA avec Linux et les devices tree.

Résultats obtenus

J'ai réussi à mettre en place toutes les étapes qui m'était demandées dans ce laboratoire.

Date : 29.05.20

Nom de l'étudiant : Spinelli Isaia

```
// SPDX-License-Identifier: GPL-2.0
/*
 * Copyright Altera Corporation (C) 2015. All rights reserved.
 */

#include "socfpga_cyclone5.dtsi"

/ {
    model = "Terasic DE-0(Atlas)";
    compatible = "terasic,de0-atlas", "altr,socfpga-cyclone5", "altr,socfpga";

    chosen {
        bootargs = "earlyprintk";
        stdout-path = "serial0:115200n8";
    };

    memory@0 {
        name = "memory";
        device_type = "memory";
        reg = <0x0 0x40000000>; /* 1GB */
    };

    aliases {
        ethernet0 = &gmac1;
    };

    regulator_3_3v: 3-3-v-regulator {
        compatible = "regulator-fixed";
        regulator-name = "3.3V";
        regulator-min-microvolt = <3300000>;
        regulator-max-microvolt = <3300000>;
    };

    leds {
        compatible = "gpio-leds";
        hps0 {
            label = "hps_led0";
            gpios = <&portb 24 0>;
            linux,default-trigger = "heartbeat";
        };
    };
};

&gmac1 {
    status = "okay";
    phy-mode = "rgmii";

    txd0-skew-ps = <0>; /* -420ps */
    txd1-skew-ps = <0>; /* -420ps */
    txd2-skew-ps = <0>; /* -420ps */
    txd3-skew-ps = <0>; /* -420ps */
    rxd0-skew-ps = <420>; /* 0ps */
    rxd1-skew-ps = <420>; /* 0ps */
    rxd2-skew-ps = <420>; /* 0ps */
    rxd3-skew-ps = <420>; /* 0ps */
    txen-skew-ps = <0>; /* -420ps */
    txc-skew-ps = <1860>; /* 960ps */
    rxdv-skew-ps = <420>; /* 0ps */
    rxc-skew-ps = <1680>; /* 780ps */

    max-frame-size = <3800>;
};


&mmc0 {
    vmmc-supply = <&regulator_3_3v>;
    vqmmc-supply = <&regulator_3_3v>;
    status = "okay";
};
```

```
70
71  &uart0 {
72      status = "okay";
73  };
74
75  &usb1 {
76      status = "okay";
77  };
78
```

```
// SPDX-License-Identifier: GPL-2.0+
/*
 * Copyright (C) 2012 Altera Corporation <www.altera.com>
 */

/dts-v1/;
/* First 4KB has trampoline code for secondary cores. */
/memreserve/ 0x00000000 0x0001000;
#include "socfpga.dtsi"

/ {
    soc {
        clkmgr@ffd04000 {
            clocks {
                osc1 {
                    clock-frequency = <25000000>;
                };
            };
        };

        mmc0: dwmmc0@ff704000 {
            broken-cd;
            bus-width = <4>;
            cap-mmc-highspeed;
            cap-sd-highspeed;
        };

        sysmgr@ffd08000 {
            cpu1-start-addr = <0xffd080c4>;
        };
    };
};

&watchdog0 {
    status = "okay";
};

```

```
// SPDX-License-Identifier: GPL-2.0+
/*
 * Copyright (C) 2012 Altera <www.altera.com>
 */

#include <dt-bindings/reset/altr,rst-mgr.h>

/ {
    #address-cells = <1>;
    #size-cells = <1>;

    aliases {
        serial0 = &uart0;
        serial1 = &uart1;
        timer0 = &timer0;
        timer1 = &timer1;
        timer2 = &timer2;
        timer3 = &timer3;
    };

    cpus {
        #address-cells = <1>;
        #size-cells = <0>;
        enable-method = "altr,socfpga-smp";

        cpu0: cpu@0 {
            compatible = "arm,cortex-a9";
            device_type = "cpu";
            reg = <0>;
            next-level-cache = <&L2>;
        };
        cpu1: cpu@1 {
            compatible = "arm,cortex-a9";
            device_type = "cpu";
            reg = <1>;
            next-level-cache = <&L2>;
        };
    };

    pmu: pmu@ff111000 {
        compatible = "arm,cortex-a9-pmu";
        interrupt-parent = <&intc>;
        interrupts = <0 176 4>, <0 177 4>;
        interrupt-affinity = <&cpu0>, <&cpu1>;
        reg = <0xff111000 0x1000>,
              <0xff113000 0x1000>;
    };

    intc: intc@fffed000 {
        compatible = "arm,cortex-a9-gic";
        #interrupt-cells = <3>;
        interrupt-controller;
        reg = <0xfffed000 0x1000>,
              <0xfffec100 0x100>;
    };

    soc {
        #address-cells = <1>;
        #size-cells = <1>;
        compatible = "simple-bus";
        device_type = "soc";
        interrupt-parent = <&intc>;
        ranges;

        amba {
            compatible = "simple-bus";
            #address-cells = <1>;
            #size-cells = <1>;
            ranges;
```

```
70
71              pdma: pdma@ffe01000 {
72                  compatible = "arm,pl330", "arm,primecell";
73                  reg = <0xffe01000 0x1000>;
74                  interrupts = <0 104 4>,
75                               <0 105 4>,
76                               <0 106 4>,
77                               <0 107 4>,
78                               <0 108 4>,
79                               <0 109 4>,
80                               <0 110 4>,
81                               <0 111 4>;
82                  #dma-cells = <1>;
83                  #dma-channels = <8>;
84                  #dma-requests = <32>;
85                  clocks = <&l4_main_clk>;
86                  clock-names = "apb_pclk";
87                  resets = <&rst DMA_RESET>;
88                  reset-names = "dma";
89              };
90          };
91
92          base_fpga_region {
93              compatible = "fpga-region";
94              fpga-mgr = <&fpgamgr0>;
95
96              #address-cells = <0x1>;
97              #size-cells = <0x1>;
98          };
99
100         can0: can@ffc00000 {
101             compatible = "bosch,d_can";
102             reg = <0xffc00000 0x1000>;
103             interrupts = <0 131 4>, <0 132 4>, <0 133 4>, <0 134 4>;
104             clocks = <&can0_clk>;
105             resets = <&rst CAN0_RESET>;
106             status = "disabled";
107         };
108
109         can1: can@ffc01000 {
110             compatible = "bosch,d_can";
111             reg = <0xffc01000 0x1000>;
112             interrupts = <0 135 4>, <0 136 4>, <0 137 4>, <0 138 4>;
113             clocks = <&can1_clk>;
114             resets = <&rst CAN1_RESET>;
115             status = "disabled";
116         };
117
118         clkmgr@ffd04000 {
119                 compatible = "altr,clk-mgr";
120                 reg = <0xffd04000 0x1000>;
121
122                 clocks {
123                     #address-cells = <1>;
124                     #size-cells = <0>;
125
126                     osc1: osc1 {
127                         #clock-cells = <0>;
128                         compatible = "fixed-clock";
129                     };
130
131                     osc2: osc2 {
132                         #clock-cells = <0>;
133                         compatible = "fixed-clock";
134                     };
135
136                     f2s_periph_ref_clk: f2s_periph_ref_clk {
137                         #clock-cells = <0>;
138                         compatible = "fixed-clock";
```

```
                        };

                        f2s_sdram_ref_clk: f2s_sdram_ref_clk {
                            #clock-cells = <0>;
                            compatible = "fixed-clock";
                        };

                        main_pll: main_pll@40 {
                            #address-cells = <1>;
                            #size-cells = <0>;
                            #clock-cells = <0>;
                            compatible = "altr,socfpga-pll-clock";
                            clocks = <&osc1>;
                            reg = <0x40>;

                            mpuclk: mpuclk@48 {
                                #clock-cells = <0>;
                                compatible = "altr,socfpga-perip-clk";
                                clocks = <&main_pll>;
                                div-reg = <0xe0 0 9>;
                                reg = <0x48>;
                            };

                            mainclk: mainclk@4c {
                                #clock-cells = <0>;
                                compatible = "altr,socfpga-perip-clk";
                                clocks = <&main_pll>;
                                div-reg = <0xe4 0 9>;
                                reg = <0x4C>;
                            };

                            dbg_base_clk: dbg_base_clk@50 {
                                #clock-cells = <0>;
                                compatible = "altr,socfpga-perip-clk";
                                clocks = <&main_pll>, <&osc1>;
                                div-reg = <0xe8 0 9>;
                                reg = <0x50>;
                            };

                            main_qspi_clk: main_qspi_clk@54 {
                                #clock-cells = <0>;
                                compatible = "altr,socfpga-perip-clk";
                                clocks = <&main_pll>;
                                reg = <0x54>;
                            };

                            main_nand_sdmmc_clk: main_nand_sdmmc_clk@58 {
                                #clock-cells = <0>;
                                compatible = "altr,socfpga-perip-clk";
                                clocks = <&main_pll>;
                                reg = <0x58>;
                            };

                            cfg_h2f_usr0_clk: cfg_h2f_usr0_clk@5c {
                                #clock-cells = <0>;
                                compatible = "altr,socfpga-perip-clk";
                                clocks = <&main_pll>;
                                reg = <0x5C>;
                            };
                        };

                        periph_pll: periph_pll@80 {
                            #address-cells = <1>;
                            #size-cells = <0>;
                            #clock-cells = <0>;
                            compatible = "altr,socfpga-pll-clock";
                            clocks = <&osc1>, <&osc2>, <&f2s_periph_ref_clk>;
                            reg = <0x80>;

```

```
208                         emac0_clk: emac0_clk@88 {
209                             #clock-cells = <0>;
210                             compatible = "altr,socfpga-perip-clk";
211                             clocks = <&periph_pll>;
212                             reg = <0x88>;
213                         };
214
215                         emac1_clk: emac1_clk@8c {
216                             #clock-cells = <0>;
217                             compatible = "altr,socfpga-perip-clk";
218                             clocks = <&periph_pll>;
219                             reg = <0x8C>;
220                         };
221
222                         per_qspi_clk: per_qsi_clk@90 {
223                             #clock-cells = <0>;
224                             compatible = "altr,socfpga-perip-clk";
225                             clocks = <&periph_pll>;
226                             reg = <0x90>;
227                         };
228
229                         per_nand_mmc_clk: per_nand_mmc_clk@94 {
230                             #clock-cells = <0>;
231                             compatible = "altr,socfpga-perip-clk";
232                             clocks = <&periph_pll>;
233                             reg = <0x94>;
234                         };
235
236                         per_base_clk: per_base_clk@98 {
237                             #clock-cells = <0>;
238                             compatible = "altr,socfpga-perip-clk";
239                             clocks = <&periph_pll>;
240                             reg = <0x98>;
241                         };
242
243                         h2f_usr1_clk: h2f_usr1_clk@9c {
244                             #clock-cells = <0>;
245                             compatible = "altr,socfpga-perip-clk";
246                             clocks = <&periph_pll>;
247                             reg = <0x9C>;
248                         };
249                     };
250
251                     sdram_pll: sdram_pll@c0 {
252                         #address-cells = <1>;
253                         #size-cells = <0>;
254                         #clock-cells = <0>;
255                         compatible = "altr,socfpga-pll-clock";
256                         clocks = <&osc1>, <&osc2>, <&f2s_sdram_ref_clk>;
257                         reg = <0xC0>;
258
259                         ddr_dqs_clk: ddr_dqs_clk@c8 {
260                             #clock-cells = <0>;
261                             compatible = "altr,socfpga-perip-clk";
262                             clocks = <&sdram_pll>;
263                             reg = <0xC8>;
264                         };
265
266                         ddr_2x_dqs_clk: ddr_2x_dqs_clk@cc {
267                             #clock-cells = <0>;
268                             compatible = "altr,socfpga-perip-clk";
269                             clocks = <&sdram_pll>;
270                             reg = <0xCC>;
271                         };
272
273                         ddr_dq_clk: ddr_dq_clk@d0 {
274                             #clock-cells = <0>;
275                             compatible = "altr,socfpga-perip-clk";
276                             clocks = <&sdram_pll>;
```

```
277                         reg = <0xD0>;
278                     };
279
280                     h2f_usr2_clk: h2f_usr2_clk@d4 {
281                         #clock-cells = <0>;
282                         compatible = "altr,socfpga-perip-clk";
283                         clocks = <&sdram_pll>;
284                         reg = <0xD4>;
285                     };
286                 };
287
288                 mpu_periph_clk: mpu_periph_clk {
289                     #clock-cells = <0>;
290                     compatible = "altr,socfpga-perip-clk";
291                     clocks = <&mpuclk>;
292                     fixed-divider = <4>;
293                 };
294
295                 mpu_l2_ram_clk: mpu_l2_ram_clk {
296                     #clock-cells = <0>;
297                     compatible = "altr,socfpga-perip-clk";
298                     clocks = <&mpuclk>;
299                     fixed-divider = <2>;
300                 };
301
302                 l4_main_clk: l4_main_clk {
303                     #clock-cells = <0>;
304                     compatible = "altr,socfpga-gate-clk";
305                     clocks = <&mainclk>;
306                     clk-gate = <0x60 0>;
307                 };
308
309                 l3_main_clk: l3_main_clk {
310                     #clock-cells = <0>;
311                     compatible = "altr,socfpga-perip-clk";
312                     clocks = <&mainclk>;
313                     fixed-divider = <1>;
314                 };
315
316                 l3_mp_clk: l3_mp_clk {
317                     #clock-cells = <0>;
318                     compatible = "altr,socfpga-gate-clk";
319                     clocks = <&mainclk>;
320                     div-reg = <0x64 0 2>;
321                     clk-gate = <0x60 1>;
322                 };
323
324                 l3_sp_clk: l3_sp_clk {
325                     #clock-cells = <0>;
326                     compatible = "altr,socfpga-gate-clk";
327                     clocks = <&l3_mp_clk>;
328                     div-reg = <0x64 2 2>;
329                 };
330
331                 l4_mp_clk: l4_mp_clk {
332                     #clock-cells = <0>;
333                     compatible = "altr,socfpga-gate-clk";
334                     clocks = <&mainclk>, <&per_base_clk>;
335                     div-reg = <0x64 4 3>;
336                     clk-gate = <0x60 2>;
337                 };
338
339                 l4_sp_clk: l4_sp_clk {
340                     #clock-cells = <0>;
341                     compatible = "altr,socfpga-gate-clk";
342                     clocks = <&mainclk>, <&per_base_clk>;
343                     div-reg = <0x64 7 3>;
344                     clk-gate = <0x60 3>;
345                 };
```

```
346
347                     dbg_at_clk: dbg_at_clk {
348                         #clock-cells = <0>;
349                         compatible = "altr,socfpga-gate-clk";
350                         clocks = <&dbg_base_clk>;
351                         div-reg = <0x68 0 2>;
352                         clk-gate = <0x60 4>;
353                     };
354
355                     dbg_clk: dbg_clk {
356                         #clock-cells = <0>;
357                         compatible = "altr,socfpga-gate-clk";
358                         clocks = <&dbg_at_clk>;
359                         div-reg = <0x68 2 2>;
360                         clk-gate = <0x60 5>;
361                     };
362
363                     dbg_trace_clk: dbg_trace_clk {
364                         #clock-cells = <0>;
365                         compatible = "altr,socfpga-gate-clk";
366                         clocks = <&dbg_base_clk>;
367                         div-reg = <0x6C 0 3>;
368                         clk-gate = <0x60 6>;
369                     };
370
371                     dbg_timer_clk: dbg_timer_clk {
372                         #clock-cells = <0>;
373                         compatible = "altr,socfpga-gate-clk";
374                         clocks = <&dbg_base_clk>;
375                         clk-gate = <0x60 7>;
376                     };
377
378                     cfg_clk: cfg_clk {
379                         #clock-cells = <0>;
380                         compatible = "altr,socfpga-gate-clk";
381                         clocks = <&cfg_h2f_usr0_clk>;
382                         clk-gate = <0x60 8>;
383                     };
384
385                     h2f_user0_clk: h2f_user0_clk {
386                         #clock-cells = <0>;
387                         compatible = "altr,socfpga-gate-clk";
388                         clocks = <&cfg_h2f_usr0_clk>;
389                         clk-gate = <0x60 9>;
390                     };
391
392                     emac_0_clk: emac_0_clk {
393                         #clock-cells = <0>;
394                         compatible = "altr,socfpga-gate-clk";
395                         clocks = <&emac0_clk>;
396                         clk-gate = <0xa0 0>;
397                     };
398
399                     emac_1_clk: emac_1_clk {
400                         #clock-cells = <0>;
401                         compatible = "altr,socfpga-gate-clk";
402                         clocks = <&emac1_clk>;
403                         clk-gate = <0xa0 1>;
404                     };
405
406                     usb_mp_clk: usb_mp_clk {
407                         #clock-cells = <0>;
408                         compatible = "altr,socfpga-gate-clk";
409                         clocks = <&per_base_clk>;
410                         clk-gate = <0xa0 2>;
411                         div-reg = <0xa4 0 3>;
412                     };
413
414                     spi_m_clk: spi_m_clk {
```

```
415                         #clock-cells = <0>;
416                         compatible = "altr,socfpga-gate-clk";
417                         clocks = <&per_base_clk>;
418                         clk-gate = <0xa0 3>;
419                         div-reg = <0xa4 3 3>;
420                     };
421
422                     can0_clk: can0_clk {
423                         #clock-cells = <0>;
424                         compatible = "altr,socfpga-gate-clk";
425                         clocks = <&per_base_clk>;
426                         clk-gate = <0xa0 4>;
427                         div-reg = <0xa4 6 3>;
428                     };
429
430                     can1_clk: can1_clk {
431                         #clock-cells = <0>;
432                         compatible = "altr,socfpga-gate-clk";
433                         clocks = <&per_base_clk>;
434                         clk-gate = <0xa0 5>;
435                         div-reg = <0xa4 9 3>;
436                     };
437
438                     gpio_db_clk: gpio_db_clk {
439                         #clock-cells = <0>;
440                         compatible = "altr,socfpga-gate-clk";
441                         clocks = <&per_base_clk>;
442                         clk-gate = <0xa0 6>;
443                         div-reg = <0xa8 0 24>;
444                     };
445
446                     h2f_user1_clk: h2f_user1_clk {
447                         #clock-cells = <0>;
448                         compatible = "altr,socfpga-gate-clk";
449                         clocks = <&h2f_usr1_clk>;
450                         clk-gate = <0xa0 7>;
451                     };
452
453                     sdmmc_clk: sdmmc_clk {
454                         #clock-cells = <0>;
455                         compatible = "altr,socfpga-gate-clk";
456                         clocks = <&f2s_periph_ref_clk>, <&main_nand_sdmmc_clk>,
                         <&per_nand_mmc_clk>;
457                         clk-gate = <0xa0 8>;
458                         clk-phase = <0 135>;
459                     };
460
461                     sdmmc_clk_divided: sdmmc_clk_divided {
462                         #clock-cells = <0>;
463                         compatible = "altr,socfpga-gate-clk";
464                         clocks = <&sdmmc_clk>;
465                         clk-gate = <0xa0 8>;
466                         fixed-divider = <4>;
467                     };
468
469                     nand_x_clk: nand_x_clk {
470                         #clock-cells = <0>;
471                         compatible = "altr,socfpga-gate-clk";
472                         clocks = <&f2s_periph_ref_clk>, <&main_nand_sdmmc_clk>,
                         <&per_nand_mmc_clk>;
473                         clk-gate = <0xa0 9>;
474                     };
475
476                     nand_ecc_clk: nand_ecc_clk {
477                         #clock-cells = <0>;
478                         compatible = "altr,socfpga-gate-clk";
479                         clocks = <&nand_x_clk>;
480                         clk-gate = <0xa0 9>;
481                     };
```

```
482
483                     nand_clk: nand_clk {
484                         #clock-cells = <0>;
485                         compatible = "altr,socfpga-gate-clk";
486                         clocks = <&nand_x_clk>;
487                         clk-gate = <0xa0 10>;
488                         fixed-divider = <4>;
489                     };
490
491                     qspi_clk: qspi_clk {
492                         #clock-cells = <0>;
493                         compatible = "altr,socfpga-gate-clk";
494                         clocks = <&f2s_periph_ref_clk>, <&main_qspi_clk>,
                        <&per_qspi_clk>;
495                         clk-gate = <0xa0 11>;
496                     };
497
498                     ddr_dqs_clk_gate: ddr_dqs_clk_gate {
499                         #clock-cells = <0>;
500                         compatible = "altr,socfpga-gate-clk";
501                         clocks = <&ddr_dqs_clk>;
502                         clk-gate = <0xd8 0>;
503                     };
504
505                     ddr_2x_dqs_clk_gate: ddr_2x_dqs_clk_gate {
506                         #clock-cells = <0>;
507                         compatible = "altr,socfpga-gate-clk";
508                         clocks = <&ddr_2x_dqs_clk>;
509                         clk-gate = <0xd8 1>;
510                     };
511
512                     ddr_dq_clk_gate: ddr_dq_clk_gate {
513                         #clock-cells = <0>;
514                         compatible = "altr,socfpga-gate-clk";
515                         clocks = <&ddr_dq_clk>;
516                         clk-gate = <0xd8 2>;
517                     };
518
519                     h2f_user2_clk: h2f_user2_clk {
520                         #clock-cells = <0>;
521                         compatible = "altr,socfpga-gate-clk";
522                         clocks = <&h2f_usr2_clk>;
523                         clk-gate = <0xd8 3>;
524                     };
525
526                 };
527             };
528
529             fpga_bridge0: fpga_bridge@ff200000 {
530                 compatible = "altr,socfpga-lwhps2fpga-bridge";
531                 reg = <0xff200000 0x200000>;
532                 resets = <&rst LWHPS2FPGA_RESET>;
533                 clocks = <&l4_main_clk>;
534             };
535
536             fpga_bridge1: fpga_bridge@ff500000 {
537                 compatible = "altr,socfpga-hps2fpga-bridge";
538                 reg = <0xff500000 0x10000>;
539                 resets = <&rst HPS2FPGA_RESET>;
540                 clocks = <&l4_main_clk>;
541             };
542
543             fpgamgr0: fpgamgr@ff706000 {
544                 compatible = "altr,socfpga-fpga-mgr";
545                 reg = <0xff706000 0x1000
546                        0xffb90000 0x4>;
547                 interrupts = <0 175 4>;
548             };
549
```

```
550             gmac0: ethernet@ff700000 {
551                 compatible = "altr,socfpga-stmmac", "snps,dwmac-3.70a", "snps,dwmac";
552                 altr,sysmgr-syscon = <&sysmgr 0x60 0>;
553                 reg = <0xff700000 0x2000>;
554                 interrupts = <0 115 4>;
555                 interrupt-names = "macirq";
556                 mac-address = [00 00 00 00 00 00];/* Filled in by U-Boot */
557                 clocks = <&emac_0_clk>;
558                 clock-names = "stmmaceth";
559                 resets = <&rst EMAC0_RESET>;
560                 reset-names = "stmmaceth";
561                 snps,multicast-filter-bins = <256>;
562                 snps,perfect-filter-entries = <128>;
563                 tx-fifo-depth = <4096>;
564                 rx-fifo-depth = <4096>;
565                 status = "disabled";
566             };
567
568             gmac1: ethernet@ff702000 {
569                 compatible = "altr,socfpga-stmmac", "snps,dwmac-3.70a", "snps,dwmac";
570                 altr,sysmgr-syscon = <&sysmgr 0x60 2>;
571                 reg = <0xff702000 0x2000>;
572                 interrupts = <0 120 4>;
573                 interrupt-names = "macirq";
574                 mac-address = [00 00 00 00 00 00];/* Filled in by U-Boot */
575                 clocks = <&emac_1_clk>;
576                 clock-names = "stmmaceth";
577                 resets = <&rst EMAC1_RESET>;
578                 reset-names = "stmmaceth";
579                 snps,multicast-filter-bins = <256>;
580                 snps,perfect-filter-entries = <128>;
581                 tx-fifo-depth = <4096>;
582                 rx-fifo-depth = <4096>;
583                 status = "disabled";
584             };
585
586             gpio0: gpio@ff708000 {
587                 #address-cells = <1>;
588                 #size-cells = <0>;
589                 compatible = "snps,dw-apb-gpio";
590                 reg = <0xff708000 0x1000>;
591                 clocks = <&l4_mp_clk>;
592                 resets = <&rst GPIO0_RESET>;
593                 status = "disabled";
594
595                 porta: gpio-controller@0 {
596                     compatible = "snps,dw-apb-gpio-port";
597                     gpio-controller;
598                     #gpio-cells = <2>;
599                     snps,nr-gpios = <29>;
600                     reg = <0>;
601                     interrupt-controller;
602                     #interrupt-cells = <2>;
603                     interrupts = <0 164 4>;
604                 };
605             };
606
607             gpio1: gpio@ff709000 {
608                 #address-cells = <1>;
609                 #size-cells = <0>;
610                 compatible = "snps,dw-apb-gpio";
611                 reg = <0xff709000 0x1000>;
612                 clocks = <&l4_mp_clk>;
613                 resets = <&rst GPIO1_RESET>;
614                 status = "disabled";
615
616                 portb: gpio-controller@0 {
617                     compatible = "snps,dw-apb-gpio-port";
618                     gpio-controller;
```

```
619                 #gpio-cells = <2>;
620                 snps,nr-gpios = <29>;
621                 reg = <0>;
622                 interrupt-controller;
623                 #interrupt-cells = <2>;
624                 interrupts = <0 165 4>;
625             };
626         };
627
628         gpio2: gpio@ff70a000 {
629             #address-cells = <1>;
630             #size-cells = <0>;
631             compatible = "snps,dw-apb-gpio";
632             reg = <0xff70a000 0x1000>;
633             clocks = <&l4_mp_clk>;
634             resets = <&rst GPIO2_RESET>;
635             status = "disabled";
636
637             portc: gpio-controller@0 {
638                 compatible = "snps,dw-apb-gpio-port";
639                 gpio-controller;
640                 #gpio-cells = <2>;
641                 snps,nr-gpios = <27>;
642                 reg = <0>;
643                 interrupt-controller;
644                 #interrupt-cells = <2>;
645                 interrupts = <0 166 4>;
646             };
647         };
648
649         i2c0: i2c@ffc04000 {
650             #address-cells = <1>;
651             #size-cells = <0>;
652             compatible = "snps,designware-i2c";
653             reg = <0xffc04000 0x1000>;
654             resets = <&rst I2C0_RESET>;
655             clocks = <&l4_sp_clk>;
656             interrupts = <0 158 0x4>;
657             status = "disabled";
658         };
659
660         i2c1: i2c@ffc05000 {
661             #address-cells = <1>;
662             #size-cells = <0>;
663             compatible = "snps,designware-i2c";
664             reg = <0xffc05000 0x1000>;
665             resets = <&rst I2C1_RESET>;
666             clocks = <&l4_sp_clk>;
667             interrupts = <0 159 0x4>;
668             status = "disabled";
669         };
670
671         i2c2: i2c@ffc06000 {
672             #address-cells = <1>;
673             #size-cells = <0>;
674             compatible = "snps,designware-i2c";
675             reg = <0xffc06000 0x1000>;
676             resets = <&rst I2C2_RESET>;
677             clocks = <&l4_sp_clk>;
678             interrupts = <0 160 0x4>;
679             status = "disabled";
680         };
681
682         i2c3: i2c@ffc07000 {
683             #address-cells = <1>;
684             #size-cells = <0>;
685             compatible = "snps,designware-i2c";
686             reg = <0xffc07000 0x1000>;
687             resets = <&rst I2C3_RESET>;
```

```
            clocks = <&l4_sp_clk>;
            interrupts = <0 161 0x4>;
            status = "disabled";
        };

        eccmgr: eccmgr {
            compatible = "altr,socfpga-ecc-manager";
            #address-cells = <1>;
            #size-cells = <1>;
            ranges;

            l2-ecc@ffd08140 {
                compatible = "altr,socfpga-l2-ecc";
                reg = <0xffd08140 0x4>;
                interrupts = <0 36 1>, <0 37 1>;
            };

            ocram-ecc@ffd08144 {
                compatible = "altr,socfpga-ocram-ecc";
                reg = <0xffd08144 0x4>;
                iram = <&ocram>;
                interrupts = <0 178 1>, <0 179 1>;
            };
        };

        L2: l2-cache@fffef000 {
            compatible = "arm,pl310-cache";
            reg = <0xfffef000 0x1000>;
            interrupts = <0 38 0x04>;
            cache-unified;
            cache-level = <2>;
            arm,tag-latency = <1 1 1>;
            arm,data-latency = <2 1 1>;
            prefetch-data = <1>;
            prefetch-instr = <1>;
            arm,shared-override;
            arm,double-linefill = <1>;
            arm,double-linefill-incr = <0>;
            arm,double-linefill-wrap = <1>;
            arm,prefetch-drop = <0>;
            arm,prefetch-offset = <7>;
        };

        l3regs@0xff800000 {
            compatible = "altr,l3regs", "syscon";
            reg = <0xff800000 0x1000>;
        };

        mmc: dwmmc0@ff704000 {
            compatible = "altr,socfpga-dw-mshc";
            reg = <0xff704000 0x1000>;
            interrupts = <0 139 4>;
            fifo-depth = <0x400>;
            #address-cells = <1>;
            #size-cells = <0>;
            clocks = <&l4_mp_clk>, <&sdmmc_clk_divided>;
            clock-names = "biu", "ciu";
            resets = <&rst SDMMC_RESET>;
            status = "disabled";
        };

        nand0: nand@ff900000 {
            #address-cells = <0x1>;
            #size-cells = <0x0>;
            compatible = "altr,socfpga-denali-nand";
            reg = <0xff900000 0x100000>,
                  <0xffb80000 0x10000>;
            reg-names = "nand_data", "denali_reg";
            interrupts = <0x0 0x90 0x4>;
```

```
            clocks = <&nand_clk>, <&nand_x_clk>, <&nand_ecc_clk>;
            clock-names = "nand", "nand_x", "ecc";
            resets = <&rst NAND_RESET>;
            status = "disabled";
        };

        ocram: sram@ffff0000 {
            compatible = "mmio-sram";
            reg = <0xffff0000 0x10000>;
        };

        qspi: spi@ff705000 {
            compatible = "cdns,qspi-nor";
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <0xff705000 0x1000>,
                  <0xffa00000 0x1000>;
            interrupts = <0 151 4>;
            cdns,fifo-depth = <128>;
            cdns,fifo-width = <4>;
            cdns,trigger-address = <0x00000000>;
            clocks = <&qspi_clk>;
            resets = <&rst QSPI_RESET>;
            status = "disabled";
        };

        rst: rstmgr@ffd05000 {
            #reset-cells = <1>;
            compatible = "altr,rst-mgr";
            reg = <0xffd05000 0x1000>;
            altr,modrst-offset = <0x10>;
        };

        scu: snoop-control-unit@fffec000 {
            compatible = "arm,cortex-a9-scu";
            reg = <0xfffec000 0x100>;
        };

        sdr: sdr@ffc25000 {
            compatible = "altr,sdr-ctl", "syscon";
            reg = <0xffc25000 0x1000>;
            resets = <&rst SDR_RESET>;
        };

        sdramedac {
            compatible = "altr,sdram-edac";
            altr,sdr-syscon = <&sdr>;
            interrupts = <0 39 4>;
        };

        spi0: spi@fff00000 {
            compatible = "snps,dw-apb-ssi";
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <0xfff00000 0x1000>;
            interrupts = <0 154 4>;
            num-cs = <4>;
            clocks = <&spi_m_clk>;
            resets = <&rst SPIM0_RESET>;
            status = "disabled";
        };

        spi1: spi@fff01000 {
            compatible = "snps,dw-apb-ssi";
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <0xfff01000 0x1000>;
            interrupts = <0 155 4>;
            num-cs = <4>;
```

```
826             clocks = <&spi_m_clk>;
827             resets = <&rst SPIM1_RESET>;
828             status = "disabled";
829         };
830
831         sysmgr: sysmgr@ffd08000 {
832             compatible = "altr,sys-mgr", "syscon";
833             reg = <0xffd08000 0x4000>;
834         };
835
836         /* Local timer */
837         timer@fffec600 {
838             compatible = "arm,cortex-a9-twd-timer";
839             reg = <0xfffec600 0x100>;
840             interrupts = <1 13 0xf01>;
841             clocks = <&mpu_periph_clk>;
842         };
843
844         timer0: timer0@ffc08000 {
845             compatible = "snps,dw-apb-timer";
846             interrupts = <0 167 4>;
847             reg = <0xffc08000 0x1000>;
848             clocks = <&l4_sp_clk>;
849             clock-names = "timer";
850             resets = <&rst SPTIMER0_RESET>;
851             reset-names = "timer";
852         };
853
854         timer1: timer1@ffc09000 {
855             compatible = "snps,dw-apb-timer";
856             interrupts = <0 168 4>;
857             reg = <0xffc09000 0x1000>;
858             clocks = <&l4_sp_clk>;
859             clock-names = "timer";
860             resets = <&rst SPTIMER1_RESET>;
861             reset-names = "timer";
862         };
863
864         timer2: timer2@ffd00000 {
865             compatible = "snps,dw-apb-timer";
866             interrupts = <0 169 4>;
867             reg = <0xffd00000 0x1000>;
868             clocks = <&osc1>;
869             clock-names = "timer";
870             resets = <&rst OSC1TIMER0_RESET>;
871             reset-names = "timer";
872         };
873
874         timer3: timer3@ffd01000 {
875             compatible = "snps,dw-apb-timer";
876             interrupts = <0 170 4>;
877             reg = <0xffd01000 0x1000>;
878             clocks = <&osc1>;
879             clock-names = "timer";
880             resets = <&rst OSC1TIMER1_RESET>;
881             reset-names = "timer";
882         };
883
884         uart0: serial0@ffc02000 {
885             compatible = "snps,dw-apb-uart";
886             reg = <0xffc02000 0x1000>;
887             interrupts = <0 162 4>;
888             reg-shift = <2>;
889             reg-io-width = <4>;
890             clocks = <&l4_sp_clk>;
891             dmas = <&pdma 28>,
892                    <&pdma 29>;
893             dma-names = "tx", "rx";
894             resets = <&rst UART0_RESET>;
```

```
        };

        uart1: serial1@ffc03000 {
            compatible = "snps,dw-apb-uart";
            reg = <0xffc03000 0x1000>;
            interrupts = <0 163 4>;
            reg-shift = <2>;
            reg-io-width = <4>;
            clocks = <&l4_sp_clk>;
            dmas = <&pdma 30>,
                   <&pdma 31>;
            dma-names = "tx", "rx";
            resets = <&rst UART1_RESET>;
        };

        usbphy0: usbphy {
            #phy-cells = <0>;
            compatible = "usb-nop-xceiv";
            status = "okay";
        };

        usb0: usb@ffb00000 {
            compatible = "snps,dwc2";
            reg = <0xffb00000 0xffff>;
            interrupts = <0 125 4>;
            clocks = <&usb_mp_clk>;
            clock-names = "otg";
            resets = <&rst USB0_RESET>;
            reset-names = "dwc2";
            phys = <&usbphy0>;
            phy-names = "usb2-phy";
            status = "disabled";
        };

        usb1: usb@ffb40000 {
            compatible = "snps,dwc2";
            reg = <0xffb40000 0xffff>;
            interrupts = <0 128 4>;
            clocks = <&usb_mp_clk>;
            clock-names = "otg";
            resets = <&rst USB1_RESET>;
            reset-names = "dwc2";
            phys = <&usbphy0>;
            phy-names = "usb2-phy";
            status = "disabled";
        };

        watchdog0: watchdog@ffd02000 {
            compatible = "snps,dw-wdt";
            reg = <0xffd02000 0x1000>;
            interrupts = <0 171 4>;
            clocks = <&osc1>;
            resets = <&rst L4WD0_RESET>;
            status = "disabled";
        };

        watchdog1: watchdog@ffd03000 {
            compatible = "snps,dw-wdt";
            reg = <0xffd03000 0x1000>;
            interrupts = <0 172 4>;
            clocks = <&osc1>;
            resets = <&rst L4WD1_RESET>;
            status = "disabled";
        };
    };
};
```

```
[    0.000000] Booting Linux on physical CPU 0x0
[    0.000000] Linux version 5.7.0-rc5-00055-g1ae7efb38854 (redsuser@reds-eda) (gcc version 4.7.3 20130328 (prerelease) (crosstool-NG linaro-1.13.1-4.7-2013.04-20130415 - Linaro GCC 2013.04), GNU ld (crosstool-NG linaro-1.13.1-4.7-2013.04-20130415 - Linaro GCC 2013.04) 2.23.1) #1 SMP Fri May 15 14:11:07 CEST 2020
[    0.000000] CPU: ARMv7 Processor [413fc090] revision 0 (ARMv7), cr=10c5387d
[    0.000000] CPU: PIPT / VIPT nonaliasing data cache, VIPT aliasing instruction cache
[    0.000000] OF: fdt: Machine model: Terasic DE-0(Atlas)
[    0.000000] Memory policy: Data cache writealloc
[    0.000000] On node 0 totalpages: 262144
[    0.000000]   Normal zone: 1536 pages used for memmap
[    0.000000]   Normal zone: 0 pages reserved
[    0.000000]   Normal zone: 196608 pages, LIFO batch:63
[    0.000000]   HighMem zone: 65536 pages, LIFO batch:15
[    0.000000] percpu: Embedded 18 pages/cpu s44928 r8192 d20608 u73728
[    0.000000] pcpu-alloc: s44928 r8192 d20608 u73728 alloc=18*4096
[    0.000000] pcpu-alloc: [0] 0 [0] 1
[    0.000000] Built 1 zonelists, mobility grouping on.  Total pages: 260608
[    0.000000] Kernel command line: console=ttyS0,115200 root=/dev/mmcblk0p2 rw rootwait
[    0.000000] Dentry cache hash table entries: 131072 (order: 7, 524288 bytes, linear)
[    0.000000] Inode-cache hash table entries: 65536 (order: 6, 262144 bytes, linear)
[    0.000000] mem auto-init: stack:off, heap alloc:off, heap free:off
[    0.000000] Memory: 1027296K/1048576K available (8192K kernel code, 638K rwdata, 1768K rodata, 1024K init, 140K bss, 21280K reserved, 0K cma-reserved, 262144K highmem)
[    0.000000] SLUB: HWalign=64, Order=0-3, MinObjects=0, CPUs=2, Nodes=1
[    0.000000] ftrace: allocating 27984 entries in 55 pages
[    0.000000] ftrace: allocated 55 pages with 5 groups
[    0.000000] rcu: Hierarchical RCU implementation.
[    0.000000] rcu:     RCU event tracing is enabled.
[    0.000000] rcu: RCU calculated value of scheduler-enlistment delay is 10 jiffies.
[    0.000000] NR_IRQS: 16, nr_irqs: 16, preallocated irqs: 16
[    0.000000] L2C: DT/platform modifies aux control register: 0x02060000 -> 0x02460000
[    0.000000] L2C-310 erratum 769419 enabled
[    0.000000] L2C-310 enabling early BRESP for Cortex-A9
[    0.000000] L2C-310 full line of zeros enabled for Cortex-A9
[    0.000000] L2C-310 ID prefetch enabled, offset 8 lines
[    0.000000] L2C-310 dynamic clock gating enabled, standby mode enabled
[    0.000000] L2C-310 cache controller enabled, 8 ways, 512 kB
[    0.000000] L2C-310: CACHE_ID 0x410030c9, AUX_CTRL 0x76460001
[    0.000000] random: get_random_bytes called from start_kernel+0x428/0x630 with crng_init=0
[    0.000000] clocksource: timer1: mask: 0xffffffff max_cycles: 0xffffffff, max_idle_ns: 19112604467 ns
[    0.000006] sched_clock: 32 bits at 100MHz, resolution 10ns, wraps every 21474836475ns
[    0.000018] Switching to timer-based delay loop, resolution 10ns
[    0.000198] Console: colour dummy device 80x30
[    0.000236] Calibrating delay loop (skipped), value calculated using timer frequency.. 200.00 BogoMIPS (lpj=1000000)
[    0.000251] pid_max: default: 32768 minimum: 301
[    0.000387] Mount-cache hash table entries: 2048 (order: 1, 8192 bytes, linear)
[    0.000402] Mountpoint-cache hash table entries: 2048 (order: 1, 8192 bytes, linear)
[    0.001099] CPU: Testing write buffer coherency: ok
[    0.001133] CPU0: Spectre v2: using BPIALL workaround
[    0.001325] CPU0: thread -1, cpu 0, socket 0, mpidr 80000000
[    0.001960] Setting up static identity map for 0x100000 - 0x100060
[    0.002101] rcu: Hierarchical SRCU implementation.
[    0.002434] smp: Bringing up secondary CPUs ...
[    0.003218] CPU1: thread -1, cpu 1, socket 0, mpidr 80000001
[    0.003227] CPU1: Spectre v2: using BPIALL workaround
[    0.003361] smp: Brought up 1 node, 2 CPUs
[    0.003372] SMP: Total of 2 processors activated (400.00 BogoMIPS).
[    0.003380] CPU: All CPU(s) started in SVC mode.
[    0.003934] devtmpfs: initialized
[    0.008193] VFP support v0.3: implementor 41 architecture 3 part 30 variant 9 rev 4
[    0.008432] clocksource: jiffies: mask: 0xffffffff max_cycles: 0xffffffff, max_idle_ns: 19112604462750000 ns
[    0.008454] futex hash table entries: 512 (order: 3, 32768 bytes, linear)
[    0.009339] NET: Registered protocol family 16
[    0.010249] DMA: preallocated 256 KiB pool for atomic coherent allocations
```

```
[    0.011211] hw-breakpoint: found 5 (+1 reserved) breakpoint and 1 watchpoint registers.
[    0.011221] hw-breakpoint: maximum watchpoint size is 4 bytes.
[    0.026365] vgaarb: loaded
[    0.026644] SCSI subsystem initialized
[    0.026847] usbcore: registered new interface driver usbfs
[    0.026897] usbcore: registered new interface driver hub
[    0.026958] usbcore: registered new device driver usb
[    0.027126] usb_phy_generic soc:usbphy: supply vcc not found, using dummy regulator
[    0.027448] pps_core: LinuxPPS API ver. 1 registered
[    0.027457] pps_core: Software ver. 5.3.6 - Copyright 2005-2007 Rodolfo Giometti <giometti@linux.it>
[    0.027485] PTP clock support registered
[    0.027654] FPGA manager framework
[    0.028482] clocksource: Switched to clocksource timer1
[    0.621904] NET: Registered protocol family 2
[    0.622570] tcp_listen_portaddr_hash hash table entries: 512 (order: 0, 6144 bytes, linear)
[    0.622601] TCP established hash table entries: 8192 (order: 3, 32768 bytes, linear)
[    0.622688] TCP bind hash table entries: 8192 (order: 4, 65536 bytes, linear)
[    0.622830] TCP: Hash tables configured (established 8192 bind 8192)
[    0.622943] UDP hash table entries: 512 (order: 2, 16384 bytes, linear)
[    0.622986] UDP-Lite hash table entries: 512 (order: 2, 16384 bytes, linear)
[    0.623167] NET: Registered protocol family 1
[    0.623678] RPC: Registered named UNIX socket transport module.
[    0.623690] RPC: Registered udp transport module.
[    0.623696] RPC: Registered tcp transport module.
[    0.623703] RPC: Registered tcp NFSv4.1 backchannel transport module.
[    0.623718] PCI: CLS 0 bytes, default 64
[    0.624352] hw perfevents: enabled with armv7_cortex_a9 PMU driver, 7 counters available
[    0.625681] workingset: timestamp_bits=30 max_order=18 bucket_order=0
[    0.633028] NFS: Registering the id_resolver key type
[    0.633060] Key type id_resolver registered
[    0.633068] Key type id_legacy registered
[    0.633085] Installing knfsd (copyright (C) 1996 okir@monad.swb.de).
[    0.633955] ntfs: driver 2.1.32 [Flags: R/W].
[    0.634178] jffs2: version 2.2. (NAND) \xfffffffc2\xffffffa9 2001-2006 Red Hat, Inc.
[    0.634763] bounce: pool size: 64 pages
[    0.634781] io scheduler mq-deadline registered
[    0.634790] io scheduler kyber registered
[    0.637982] dma-pl330 ffe01000.pdma: Loaded driver for PL330 DMAC-341330
[    0.637999] dma-pl330 ffe01000.pdma:     DBUFF-512x8bytes Num_Chans-8 Num_Peri-32 Num_Events-8
[    0.641558] Serial: 8250/16550 driver, 2 ports, IRQ sharing disabled
[    0.642611] printk: console [ttyS0] disabled
[    0.642659] ffc02000.serial0: ttyS0 at MMIO 0xffc02000 (irq = 36, base_baud = 6250000) is a 16550A
[    1.240748] printk: console [ttyS0] enabled
[    1.245583] ffc03000.serial1: ttyS1 at MMIO 0xffc03000 (irq = 37, base_baud = 6250000) is a 16550A
[    1.256073] brd: module loaded
[    1.267223] loop: module loaded
[    1.271679] libphy: Fixed MDIO Bus: probed
[    1.276429] CAN device driver interface
[    1.280574] socfpga-dwmac ff702000.ethernet: IRQ eth_wake_irq not found
[    1.287166] socfpga-dwmac ff702000.ethernet: IRQ eth_lpi not found
[    1.293467] socfpga-dwmac ff702000.ethernet: PTP uses main clock
[    1.299687] socfpga-dwmac ff702000.ethernet: Version ID not available
[    1.306109] socfpga-dwmac ff702000.ethernet:     DWMAC1000
[    1.311348] socfpga-dwmac ff702000.ethernet: DMA HW capability register supported
[    1.318817] socfpga-dwmac ff702000.ethernet: RX Checksum Offload Engine supported
[    1.326268] socfpga-dwmac ff702000.ethernet: COE Type 2
[    1.331486] socfpga-dwmac ff702000.ethernet: TX Checksum insertion supported
[    1.338517] socfpga-dwmac ff702000.ethernet: Enhanced/Alternate descriptors
[    1.345449] socfpga-dwmac ff702000.ethernet: Extended descriptors not supported
[    1.352738] socfpga-dwmac ff702000.ethernet: Ring mode enabled
[    1.358567] socfpga-dwmac ff702000.ethernet: device MAC address 26:6a:60:7e:22:a2
[    1.374237] libphy: stmmac: probed
```

```
[    1.377643] Micrel KSZ9021 Gigabit PHY stmmac-0:01: attached PHY driver [Micrel KSZ9021 Gigabit PHY] (mii_bus:phy_addr=stmmac-0:01, irq=POLL)
[    1.391517] dwc2 ffb40000.usb: supply vusb_d not found, using dummy regulator
[    1.398745] dwc2 ffb40000.usb: supply vusb_a not found, using dummy regulator
[    1.406106] dwc2 ffb40000.usb: EPs: 16, dedicated fifos, 8064 entries in SPRAM
[    1.413806] dwc2 ffb40000.usb: DWC OTG Controller
[    1.418545] dwc2 ffb40000.usb: new USB bus registered, assigned bus number 1
[    1.425596] dwc2 ffb40000.usb: irq 38, io mem 0xffb40000
[    1.431711] hub 1-0:1.0: USB hub found
[    1.435491] hub 1-0:1.0: 1 port detected
[    1.440247] usbcore: registered new interface driver usb-storage
[    1.446468] i2c /dev entries driver
[    1.450802] Synopsys Designware Multimedia Card Interface Driver
[    1.457229] dw_mmc ff704000.dwmmc0: IDMAC supports 32-bit address mode.
[    1.463884] dw_mmc ff704000.dwmmc0: Using internal DMA controller.
[    1.470072] dw_mmc ff704000.dwmmc0: Version ID is 240a
[    1.475237] dw_mmc ff704000.dwmmc0: DW MMC controller at irq 31,32 bit host data width,1024 deep fifo
[    1.484641] mmc_host mmc0: card is polling.
[    1.501497] mmc_host mmc0: Bus speed (slot 0) = 12500000Hz (slot req 400000Hz, actual 390625HZ div = 16)
[    1.523910] ledtrig-cpu: registered to indicate activity on CPUs
[    1.530088] usbcore: registered new interface driver usbhid
[    1.535649] usbhid: USB HID core driver
[    1.539792] fpga_manager fpga0: Altera SOCFPGA FPGA Manager registered
[    1.546839] altera_hps2fpga_bridge ff200000.fpga_bridge: fpga bridge [lwhps2fpga] registered
[    1.555545] altera_hps2fpga_bridge ff500000.fpga_bridge: fpga bridge [hps2fpga] registered
[    1.564250] oprofile: using arm/armv7-ca9
[    1.569063] NET: Registered protocol family 10
[    1.574440] Segment Routing with IPv6
[    1.578203] sit: IPv6, IPv4 and MPLS over IPv4 tunneling driver
[    1.584750] NET: Registered protocol family 17
[    1.589236] NET: Registered protocol family 15
[    1.593662] can: controller area network core (rev 20170425 abi 9)
[    1.599914] NET: Registered protocol family 29
[    1.604345] can: raw protocol (rev 20170425)
[    1.608617] can: broadcast manager protocol (rev 20170425 t)
[    1.614258] can: netlink gateway (rev 20190810) max_hops=1
[    1.619917] 8021q: 802.1Q VLAN Support v1.8
[    1.624127] Key type dns_resolver registered
[    1.628496] ThumbEE CPU extension supported.
[    1.632756] Registering SWP/SWPB emulation handler
[    1.642237] dw-apb-uart ffc02000.serial0: forbid DMA for kernel console
[    1.649143] Waiting for root device /dev/mmcblk0p2...
[    1.687145] mmc_host mmc0: Bus speed (slot 0) = 12500000Hz (slot req 50000000Hz, actual 12500000HZ div = 0)
[    1.696959] mmc0: new high speed SDHC card at address 59b4
[    1.703047] mmcblk0: mmc0:59b4 USDU1 14.9 GiB
[    1.710130]  mmcblk0: p1 p2 p3
[    1.739412] EXT4-fs (mmcblk0p2): mounting ext3 file system using the ext4 subsystem
[    1.828820] random: fast init done
[    1.869756] EXT4-fs (mmcblk0p2): recovery complete
[    1.883042] EXT4-fs (mmcblk0p2): mounted filesystem with ordered data mode. Opts: (null)
[    1.891174] VFS: Mounted root (ext3 filesystem) on device 179:2.
[    1.922138] devtmpfs: mounted
[    1.927495] Freeing unused kernel memory: 1024K
[    1.932327] Run /sbin/init as init process
[    1.936406]   with arguments:
[    1.936410]     /sbin/init
[    1.936413]   with environment:
[    1.936416]     HOME=/
[    1.936419]     TERM=linux
[    1.968526] usb 1-1: new high-speed USB device number 2 using dwc2
[    2.219554] hub 1-1:1.0: USB hub found
[    2.223366] hub 1-1:1.0: 2 ports detected
[    2.797711] EXT4-fs (mmcblk0p2): re-mounted. Opts: (null)
```

```
[    3.170651] socfpga-dwmac ff702000.ethernet eth0: PHY [stmmac-0:01] driver [Micrel KSZ9021 Gigabit PHY] (irq=POLL)
[    3.181894] socfpga-dwmac ff702000.ethernet eth0: No Safety Features support found
[    3.189706] socfpga-dwmac ff702000.ethernet eth0: registered PTP clock
[    3.196219] socfpga-dwmac ff702000.ethernet eth0: configuring for phy/rgmii link mode
[    3.760330] random: crng init done

```