```
/***********************************
2
    * HEIG-VD
3
    * Haute Ecole d'Ingenerie et de Gestion du Canton de Vaud
4
    * School of Business and Engineering in Canton de Vaud
5
    * REDS Institute
6
7
    * Reconfigurable Embedded Digital Systems
8
    **************************
9
    * File
                    : address_map_arm.h
: Sébastien Masle
10
    * Author
11
12
    * Date
                      : 16.02.2018
13
14
    * Context
                : SOCF class
15
16
    **************************
17
    * Brief: provides address values that exist in the system
18
19
    * Modifications :
20
    * Ver Date Engineer Comments

* 0.0 16.02.2018 SMS Initial version.
21
22
23
   *****************************
24
25
                                    "DE1-SoC"
26 #define BOARD
27
  /* Memory */
#define DDR_BASE
28
29
                                    0x00000000
30 #define DDR END
                                    0x3FFFFFFF
31 #define A9 ONCHIP BASE
                                   0xFFFF0000
32 #define A9 ONCHIP END
                                   0xffffffff
33 #define SDRAM BASE
                                   0xC0000000
34 #define SDRAM END
                                   0xC3FFFFFF
35 #define FPGA ONCHIP BASE
                                   0xC8000000
36 #define FPGA ONCHIP END
                                   0xC803FFFF
37 #define FPGA CHAR BASE
                                   0xC9000000
38 #define FPGA CHAR END
                                   0xC9001FFF
39
```