

```
1 // SPDX-License-Identifier: GPL-2.0+
2 /*
3  * Copyright (C) 2012 Altera Corporation <www.altera.com>
4  */
5
6 /dts-v1/;
7 /* First 4KB has trampoline code for secondary cores. */
8 /memreserve/ 0x00000000 0x0001000;
9 #include "socfpga.dtsi"
10
11 / {
12     soc {
13         clkmgr@ffd04000 {
14             clocks {
15                 osc1 {
16                     clock-frequency = <25000000>;
17                 };
18             };
19         };
20
21         mmc0: dwmmc0@ff704000 {
22             broken-cd;
23             bus-width = <4>;
24             cap-mmc-highspeed;
25             cap-sd-highspeed;
26         };
27
28         sysmgr@ffd08000 {
29             cpul-start-addr = <0xffd080c4>;
30         };
31     };
32 };
33
34 &watchdog0 {
35     status = "okay";
36 };
37
```