```
1  ------------------------------------------------------------------------------
   -
2  -- HEIG-VD
3  -- Haute Ecole d'Ingenerie et de Gestion du Canton de Vaud
4  -- School of Business and Engineering in Canton de Vaud
5  ------------------------------------------------------------------------------
   -
6  -- REDS Institute
7  -- Reconfigurable Embedded Digital Systems
8  ------------------------------------------------------------------------------
   -
9  --
10 -- File                 : DE1_SoC_top.vhd
11 -- Author               : Sébastien Masle
12 -- Date                 : 17.01.2018
13 --
14 -- Context              : HPA
15 --
16 ------------------------------------------------------------------------------
   -
17 -- Description : top design for DE1-SoC board
18 --
19 ------------------------------------------------------------------------------
   -
20 -- Dependencies :
21 --
22 ------------------------------------------------------------------------------
   -
23 -- Modifications :
24 -- Ver    Date        Engineer      Comments
25 -- 0.0    17.01.2018  SMS           Initial version.
26 --
27 ------------------------------------------------------------------------------
   -
28 library ieee;
29 use ieee.std_logic_1164.all;
30
31 entity DE1_SoC_top is
32     port ( -- clock pins
33            CLOCK_50_i  : in  std_logic;
34            CLOCK2_50_i : in  std_logic;
35            CLOCK3_50_i : in  std_logic;
36            CLOCK4_50_i : in  std_logic;
37
38            -- ADC
39            ADC_CS_N_o : out std_logic;
40            ADC_DIN_o  : out std_logic;
41            ADC_DOUT_i : in std_logic;
42            ADC_SCLK_o : out std_logic;
43
44            -- Audio
45            AUD_ADCLRCK_io : inout std_logic;
46            AUD_ADCDAT_i   : in std_logic;
47            AUD_DACLRCK_io : inout std_logic;
48            AUD_DACDAT_o   : out std_logic;
49            AUD_XCK_o      : out std_logic;
50            AUD_BCLK_io    : inout std_logic;
51
52            -- SDRAM
53            DRAM_ADDR_o  : out std_logic_vector(12 downto 0);
54            DRAM_BA_o    : out std_logic_vector(1 downto 0);
55            DRAM_CAS_N_o : out std_logic;
56            DRAM_CKE_o   : out std_logic;
57            DRAM_CLK_o   : out std_logic;
58            DRAM_CS_N_o  : out std_logic;
59            DRAM_DQ_io   : inout std_logic_vector(15 downto 0);
60            DRAM_LDQM_o  : out std_logic;
61            DRAM_RAS_N_o : out std_logic;
62            DRAM_UDQM_o  : out std_logic;
```

```
63              DRAM_WE_N_o   : out std_logic;
64
65              --I2C Bus for Configuration of the Audio and Video-In Chips
66              FPGA_I2C_SCLK_o  : out std_logic;
67              FPGA_I2C_SDAT_io : inout std_logic;
68
69              -- 40-pin headers
70              GPIO_0_io     : inout std_logic_vector(35 downto 0);
71              GPIO_1_io     : inout std_logic_vector(35 downto 0);
72
73              -- Seven Segment Displays
74              HEX0_o        : out std_logic_vector(6 downto 0);
75              HEX1_o        : out std_logic_vector(6 downto 0);
76              HEX2_o        : out std_logic_vector(6 downto 0);
77              HEX3_o        : out std_logic_vector(6 downto 0);
78              HEX4_o        : out std_logic_vector(6 downto 0);
79              HEX5_o        : out std_logic_vector(6 downto 0);
80
81              -- IR
82              IRDA_RXD_i    : in std_logic;
83              IRDA_TXD_o    : out std_logic;
84
85              -- Pushbuttons
86              KEY_i         : in std_logic_vector(3 downto 0);
87
88              -- LEDs
89              LEDR_o        : out std_logic_vector(9 downto 0);
90
91              -- PS2 Ports
92              PS2_CLK_io    : inout std_logic;
93              PS2_DAT_io    : inout std_logic;
94              PS2_CLK2_io   : inout std_logic;
95              PS2_DAT2_io   : inout std_logic;
96
97              -- Slider Switches
98              SW_i          : in std_logic_vector(9 downto 0);
99
100             -- Video-In
101             TD_CLK27_i    : in std_logic;
102             TD_DATA_i     : in std_logic_vector(7 downto 0);
103             TD_HS_i       : in std_logic;
104             TD_RESET_N_o  : out std_logic;
105             TD_VS_i       : in std_logic;
106
107             -- VGA
108             VGA_R_o        : out std_logic_vector(7 downto 0);
109             VGA_G_o        : out std_logic_vector(7 downto 0);
110             VGA_B_o        : out std_logic_vector(7 downto 0);
111             VGA_CLK_o      : out std_logic;
112             VGA_SYNC_N_o   : out std_logic;
113             VGA_BLANK_N_o  : out std_logic;
114             VGA_HS_o       : out std_logic;
115             VGA_VS_o       : out std_logic;
116
117             -- DDR3 SDRAM
118             HPS_DDR3_ADDR_o      : out std_logic_vector(14 downto 0);
119             HPS_DDR3_BA_o        : out std_logic_vector(2 downto 0);
120             HPS_DDR3_CAS_N_o     : out std_logic;
121             HPS_DDR3_CKE_o       : out std_logic;
122             HPS_DDR3_CK_N_o      : out std_logic;
123             HPS_DDR3_CK_P_o      : out std_logic;
124             HPS_DDR3_CS_N_o      : out std_logic;
125             HPS_DDR3_DM_o        : out std_logic_vector(3 downto 0);
126             HPS_DDR3_DQ_io       : inout std_logic_vector(31 downto 0);
127             HPS_DDR3_DQS_N_io    : inout std_logic_vector(3 downto 0);
128             HPS_DDR3_DQS_P_io    : inout std_logic_vector(3 downto 0);
129             HPS_DDR3_ODT_o       : out std_logic;
130             HPS_DDR3_RAS_N_o     : out std_logic;
131             HPS_DDR3_RESET_N_o   : out std_logic;
```

```
132             HPS_DDR3_RZQ_i       : in std_logic;
133             HPS_DDR3_WE_N_o      : out std_logic;
134
135             -- Ethernet
136             --HPS_ENET_GTX_CLK_o   : out std_logic;
137             --HPS_ENET_INT_N_io    : inout std_logic;
138             --HPS_ENET_MDC_o       : out std_logic;
139             --HPS_ENET_MDIO_io     : inout std_logic;
140             --HPS_ENET_RX_CLK_i    : in std_logic;
141             --HPS_ENET_RX_DATA_i   : in std_logic_vector(3 downto 0);
142             --HPS_ENET_RX_DV_i     : in std_logic;
143             --HPS_ENET_TX_DATA_o   : out std_logic_vector(3 downto 0);
144             --HPS_ENET_TX_EN_o     : out std_logic;
145
146             -- Flash
147             --HPS_FLASH_DATA_io    : inout std_logic_vector(3 downto 0);
148             --HPS_FLASH_DCLK_o     : out std_logic;
149             --HPS_FLASH_NCSO_o     : out std_logic;
150
151             -- Accelerometer
152             --HPS_GSENSOR_INT_io   : inout std_logic;
153
154             -- General Purpose I/O
155             --HPS_GPIO_io          : inout std_logic_vector(1 downto 0);
156
157             -- I2C
158             --HPS_I2C_CONTROL_io   : inout std_logic;
159             --HPS_I2C1_SCLK_io     : inout std_logic;
160             --HPS_I2C1_SDAT_io     : inout std_logic;
161             --HPS_I2C2_SCLK_io     : inout std_logic;
162             --HPS_I2C2_SDAT_io     : inout std_logic;
163
164             -- Pushbutton
165             HPS_KEY_io           : inout std_logic;
166
167             -- LED
168             HPS_LED_io           : inout std_logic;
169
170             -- SD Card
171             --HPS_SD_CLK_o         : out std_logic;
172             --HPS_SD_CMD_io        : inout std_logic;
173             --HPS_SD_DATA_io       : inout std_logic_vector(3 downto 0);
174
175             -- SPI
176             --HPS_SPIM_CLK_o       : out std_logic;
177             --HPS_SPIM_MISO_i      : in std_logic;
178             --HPS_SPIM_MOSI_o      : out std_logic;
179             --HPS_SPIM_SS_io       : inout std_logic;
180
181             -- UART
182             --HPS_UART_RX_i        : in std_logic;
183             --HPS_UART_TX_o        : out std_logic;
184
185             -- USB
186             --HPS_CONV_USB_N_io    : inout std_logic;
187             --HPS_USB_CLKOUT_i     : in std_logic;
188             --HPS_USB_DATA_io      : inout std_logic_vector(7 downto 0);
189             --HPS_USB_DIR_i        : in std_logic;
190             --HPS_USB_NXT_i        : in std_logic;
191             --HPS_USB_STP_o        : out std_logic;
192
193             -- LTC connector
194             --HPS_LTC_GPIO_io      : inout std_logic;
195
196             -- FAN
197             FAN_CTRL_o           : out std_logic
198             );
199   end DE1_SoC_top;
200
```

```
architecture top of DE1_SoC_top is

    component qsys_system is
        port (
            -----------------------------------
            -- FPGA Side
            -----------------------------------

            -- Global signals
            clk_clk                         : in    std_logic                       :=
            'X';             -- clk

            -----------------------------------
            -- HPS Side
            -----------------------------------
            -- DDR3 SDRAM
            memory_mem_a                    : out   std_logic_vector(14 downto
            0);                     -- mem_a
            memory_mem_ba                   : out   std_logic_vector(2 downto
            0);                      -- mem_ba
            memory_mem_ck                   : out
            std_logic;                                      -- mem_ck
            memory_mem_ck_n                 : out
            std_logic;                                      -- mem_ck_n
            memory_mem_cke                  : out
            std_logic;                                      -- mem_cke
            memory_mem_cs_n                 : out
            std_logic;                                      -- mem_cs_n
            memory_mem_ras_n                : out
            std_logic;                                      -- mem_ras_n
            memory_mem_cas_n                : out
            std_logic;                                      -- mem_cas_n
            memory_mem_we_n                 : out
            std_logic;                                      -- mem_we_n
            memory_mem_reset_n              : out
            std_logic;                                      -- mem_reset_n
            memory_mem_dq                   : inout std_logic_vector(31 downto 0) :=
            (others => 'X'); -- mem_dq
            memory_mem_dqs                  : inout std_logic_vector(3 downto 0)  :=
            (others => 'X'); -- mem_dqs
            memory_mem_dqs_n                : inout std_logic_vector(3 downto 0)  :=
            (others => 'X'); -- mem_dqs_n
            memory_mem_odt                  : out
            std_logic;                                      -- mem_odt
            memory_mem_dm                   : out   std_logic_vector(3 downto
            0);                      -- mem_dm
            memory_oct_rzqin                : in    std_logic                       :=
            'X';             -- oct_rzqin

                conduit_export_switch_i             : in    std_logic_vector(31 downto
                0) := (others => 'X'); -- switch_i
                conduit_export_key_i                : in    std_logic_vector(31 downto
                0) := (others => 'X'); -- key_i

                conduit_export_leds_o               : out   std_logic_vector(31 downto
                0);                     -- leds_o

                conduit_export_hex0_o               : out   std_logic_vector(31 downto
                0);                     -- hex0_o
                conduit_export_hex1_o               : out   std_logic_vector(31 downto
                0);                     -- hex1_o
                conduit_export_hex2_o               : out   std_logic_vector(31 downto
                0);                     -- hex2_o
                conduit_export_hex3_o               : out   std_logic_vector(31 downto
                0);                     -- hex3_o
                conduit_export_hex4_o               : out   std_logic_vector(31 downto
                0);                     -- hex4_o
                conduit_export_hex5_o               : out   std_logic_vector(31 downto
                0);                     -- hex5_o
```

```
244
245             -- Pushbutton
246             hps_io_hps_io_gpio_inst_GPIO54  : inout std_logic                    :=
                'X';             -- hps_io_gpio_inst_GPIO54
247
248             -- LED
249             hps_io_hps_io_gpio_inst_GPIO53  : inout std_logic                    :=
                'X'              -- hps_io_gpio_inst_GPIO53
250         );
251     end component qsys_system;
252
253 begin
254
255 ------------------------------------------------------------
256 --  HPS mapping
257 ------------------------------------------------------------
258
259     System : component qsys_system
260     port map (
261         ------------------------------------
262         -- FPGA Side
263         ------------------------------------
264
265             -- Global signals
266             clk_clk             => CLOCK_50_i,
267
268             ------------------------------------
269             -- HPS Side
270             ------------------------------------
271             -- DDR3 SDRAM
272             memory_mem_a        => HPS_DDR3_ADDR_o,
273             memory_mem_ba       => HPS_DDR3_BA_o,
274             memory_mem_ck       => HPS_DDR3_CK_P_o,
275             memory_mem_ck_n     => HPS_DDR3_CK_N_o,
276             memory_mem_cke      => HPS_DDR3_CKE_o,
277             memory_mem_cs_n     => HPS_DDR3_CS_N_o,
278             memory_mem_ras_n    => HPS_DDR3_RAS_N_o,
279             memory_mem_cas_n    => HPS_DDR3_CAS_N_o,
280             memory_mem_we_n     => HPS_DDR3_WE_N_o,
281             memory_mem_reset_n  => HPS_DDR3_RESET_N_o,
282             memory_mem_dq       => HPS_DDR3_DQ_io,
283             memory_mem_dqs      => HPS_DDR3_DQS_P_io,
284             memory_mem_dqs_n    => HPS_DDR3_DQS_N_io,
285             memory_mem_odt      => HPS_DDR3_ODT_o,
286             memory_mem_dm       => HPS_DDR3_DM_o,
287             memory_oct_rzqin    => HPS_DDR3_RZQ_i,
288
289             conduit_export_switch_i (9 downto 0)               => SW_i ,     -- switch_i
290             conduit_export_switch_i (31 downto 10)                => (others => '0'),
291             conduit_export_key_i (3 downto 0)                     => KEY_i,     --
                key_i
292             conduit_export_key_i (31 downto 4)                    => (others => '0'),
293
294             conduit_export_leds_o (9 downto 0)                    => LEDR_o,    --
                leds_o
295
296             conduit_export_hex0_o (6 downto 0)                    => HEX0_o,    --
                hex0_o
297             conduit_export_hex1_o (6 downto 0)                    => HEX1_o,    --
                hex1_o
298             conduit_export_hex2_o (6 downto 0)                    => HEX2_o,    --
                hex2_o
299             conduit_export_hex3_o (6 downto 0)                    => HEX3_o,    --
                hex3_o
300             conduit_export_hex4_o (6 downto 0)                    => HEX4_o,    --
                hex4_o
301             conduit_export_hex5_o (6 downto 0)                 => HEX5_o,    -- hex5_o
302
303
```

```
304                 -- Pushbutton
305                 hps_io_hps_io_gpio_inst_GPIO54  => HPS_KEY_io,
306 
307                 -- LED
308                 hps_io_hps_io_gpio_inst_GPIO53  => HPS_LED_io
309         );
310 
311     end top;
```