General-Purpose I/O Interface 22

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The hard processor system (HPS) provides three general-purpose I/O (GPIO) interface modules. The GPIO modules are instances of the Synopsys® DesignWare® APB General Purpose Programming I/O (DW_apb_gpio) peripheral.† (65)

Features of the GPIO Interface

The GPIO interface offers the following features:

- Supports digital debounce
- Configurable interrupt mode
- Supports up to 67 I/O pins and 14 input-only pins

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†Paragraphs marked with the dagger (†) symbol are Synopsys Proprietary. Used with permission.

GPIO Interface Block Diagram and System Integration

The figure below shows a block diagram of the GPIO interface. The following table shows a pin table of the GPIO interface:

Figure 22-1: Cyclone V SoC GPIO

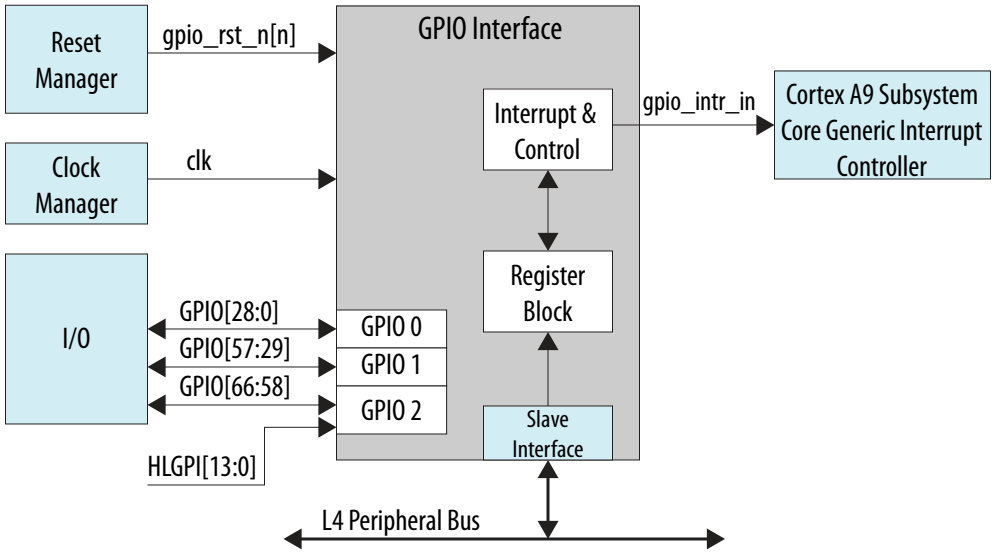


Table 22-1: GPIO Interface pin table

Pin Name	Mapped to GPIO Signal Name	Comments
GPIO [28:0]	GPIO 0 [28:0]	Input / Output
GPIO [57:29]	GPIO 1 [28:0]	Input / Output
GPIO [66:58]	GPIO 2 [8:0]	Input / Output
HLGPI [13:0]	GPIO 2 [26:13]	Input only

Table 22-2: GPIO Interface pin table

Pin Name	Mapped to GPIO Signal Name	Comments
HPS_DEDICATED_Q1 [12:1]	GPIO 0 [11:0]	Input / Output
HPS_DEDICATED_Q2 [12:1]	GPIO 0 [23:12]	Input / Output
HPS_DEDICATED_Q3 [12:1]	GPIO 1 [11:0]	Input / Output
HPS_DEDICATED_Q4 [12:1]	GPIO 1 [23:12]	Input / Output

Related Information

http://www.altera.com/literature/hb/cyclone-v/cv_52005.pdf
For more information on I/O banks locations on device, refer to *Cyclone V I/O Features*.

Functional Description of the GPIO Interface

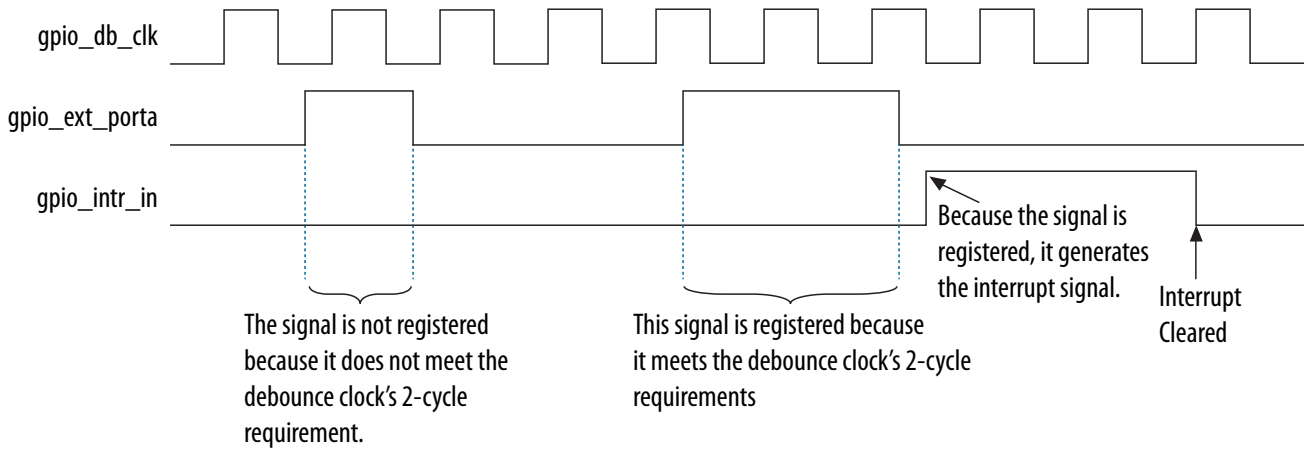
Debounce Operation

The GPIO modules provided in the HPS include optional debounce capabilities. The external signal can be debounced to remove any spurious glitches that are less than one period of the external debouncing clock, `gpio_db_clk`. †

When input signals are debounced using the `gpio_db_clk` debounce clock, the signals must be active for a minimum of two cycles of the debounce clock to guarantee that they are registered. Any input pulse widths less than a debounce clock period are filtered out. If the input signal pulse width is between one and two debounce clock widths, it may or may not be filtered out, depending on its phase relationship to the debounce clock. If the input pulse spans two rising edges of the debounce clock, it is registered. If it spans only one rising edge, it is not registered. †

The figure below shows a timing diagram of the debounce circuitry for both cases: a bounced input signal, and later, a propagated input signal.

Figure 22-2: Debounce Timing With Asychronous Reset Flip-Flops



Note: Enabling the debounce circuitry increases interrupt latency by two clock cycles of the debounce clock.

Pin Directions

The pins `GPIO0` through `GPIO66` can be configured to be either input or output signals. The pins `HLGPI0` through `HLGPI13` share pins with the HPS DDR controller and are input-only signals.

Taking the GPIO Interface Out of Reset

When a cold or warm reset is issued in the HPS, the reset manager resets this module and holds it in reset until software releases it.

After the Cortex-A9 MPCore CPU boots, it can deassert the reset signal by clearing the appropriate bits in the reset manager's corresponding reset register. For details about reset registers, refer to "Module Reset Signals".

GPIO Interface Programming Model

Debounce capability for each of the input signals can be enabled or disabled under software control by setting the corresponding bits in the `gpio_debounce` register, accordingly. The debounce clock must be stable and operational before the debounce capability is enabled.

Under software control, the direction of the external I/O pad is controlled by a write to the `gpio_swportx_ddr` register. When configured as input mode, reading `gpio_ext_porta` would read the values on the signal of the external I/O pad. When configured as output mode, the data written to the `gpio_swporta_dr` register drives the output buffer of the I/O pad. The same pins are shared for both input and output modes, so they cannot be configured as input and output modes at the same time. †

General-Purpose I/O Interface Address Map and Register Definitions

The address map and register definitions for the GPIO consist of the following regions:

- GPIO Module 0
- GPIO Module 1
- GPIO Module 2

Related Information

- **Introduction to the Hard Processor System** on page 1-1
  For more information, refer to *Introduction to the Hard Processor System* chapter.
- **http://www.altera.com/literature/hb/cyclone-v/hps.html**

GPIO Module Address Map

Registers in the GPIO module

Module Instance	Base Address
gpio0	0xFF708000
gpio1	0xFF709000
gpio2	0xFF70A000

GPIO Module

Register	Offset	Width	Access	Reset Value	Description
gpio_swporta_dr on page 22-5	0x0	32	RW	0x0	Port A Data Register
gpio_swporta_ddr on page 22-6	0x4	32	RW	0x0	Port A Data Direction Register

Register	Offset	Width	Access	Reset Value	Description
gpio_inten on page 22-7	0x30	32	RW	0x0	Interrupt Enable Register
gpio_intmask on page 22-8	0x34	32	RW	0x0	Interrupt Mask Register
gpio_inttype_level on page 22-9	0x38	32	RW	0x0	Interrupt Level Register
gpio_int_polarity on page 22-10	0x3C	32	RW	0x0	Interrupt Polarity Register
gpio_intstatus on page 22-11	0x40	32	RO	0x0	Interrupt Status Register
gpio_raw_intstatus on page 22-12	0x44	32	RO	0x0	Raw Interrupt Status Register
gpio_debounce on page 22-13	0x48	32	RW	0x0	Debounce Enable Register
gpio_porta_eoi on page 22-14	0x4C	32	WO	0x0	Clear Interrupt Register
gpio_ext_porta on page 22-15	0x50	32	RO	0x0	External Port A Register
gpio_ls_sync on page 22-16	0x60	32	RW	0x0	Synchronization Level Register
gpio_id_code on page 22-17	0x64	32	RO	0x0	ID Code Register
gpio_ver_id_code on page 22-17	0x6C	32	RO	0x3230382A	GPIO Version Register
gpio_config_reg2 on page 22-18	0x70	32	RO	0x39CFC	Configuration Register 2
gpio_config_reg1 on page 22-20	0x74	32	RO	0x1FF0F2	Configuration Register 1

gpio_swporta_dr

This GPIO Data register is used to input or output data Check the GPIO chapter in the handbook for details on how GPIO2 is implemented.

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF708000
gpio1	0xFF709000	0xFF709000
gpio2	0xFF70A000	0xFF70A000

Offset: 0x0

Access: RW

Important: To prevent indeterminate system behavior, reserved areas of memory must not be accessed by software or hardware. Any area of the memory map that is not explicitly defined as a register space or accessible memory is considered reserved.

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			gpio_swporta_dr RW 0x0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
gpio_swporta_dr RW 0x0															

gpio_swporta_dr Fields

Bit	Name	Description	Access	Reset
28:0	gpio_swporta_dr	Values written to this register are output on the I/O signals of the GPIO Data Register, if the corresponding data direction bits for GPIO Data Direction Field are set to Output mode. The value read back is equal to the last value written to this register. Note that only bits[26:0] are implemented for gpio2.	RW	0x0

gpio_swporta_ddr

This register establishes the direction of each corresponding GPIO Data Field Bit. Check the GPIO chapter in the handbook for details on how GPIO2 is implemented.

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF708004
gpio1	0xFF709000	0xFF709004
gpio2	0xFF70A000	0xFF70A004

Offset: 0x4

Access: RW

Important: To prevent indeterminate system behavior, reserved areas of memory must not be accessed by software or hardware. Any area of the memory map that is not explicitly defined as a register space or accessible memory is considered reserved.

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			gpio_swporta_ddr RW 0x0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
gpio_swporta_ddr RW 0x0															

gpio_swporta_ddr Fields

Bit	Name	Description	Access	Reset
28:0	gpio_swporta_ddr	Values written to this register independently control the direction of the corresponding data bit in the Port A Data Register. Note that only bits[26:0] are implemented for gpio2. **Value** — **Description** 0x0 — Input Direction 0x1 — Output Direction	RW	0x0

gpio_inten

The Interrupt enable register allows interrupts for each bit of the Port A data register.

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF708030
gpio1	0xFF709000	0xFF709030
gpio2	0xFF70A000	0xFF70A030

Offset: 0x30

Access: RW

Important: To prevent indeterminate system behavior, reserved areas of memory must not be accessed by software or hardware. Any area of the memory map that is not explicitly defined as a register space or accessible memory is considered reserved.

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			gpio_inten RW 0x0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
gpio_inten RW 0x0															

gpio_inten Fields

Bit	Name	Description	Access	Reset
28:0	gpio_inten	Allows each bit of Port A Data Register to be configured for interrupt capability. Interrupts are disabled on the corresponding bits of Port A Data Register if the corresponding data direction register is set to Output. Note that only bits[26:0] are implemented for gpio2. **Value** **Description** 0x0 Disable Interrupt on Port A 0x1 Enable Interrupt on Port A	RW	0x0

gpio_intmask

Controls which pins cause interrupts on Port A Data Register inputs.

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF708034
gpio1	0xFF709000	0xFF709034
gpio2	0xFF70A000	0xFF70A034

Offset: 0x34

Access: RW

Important: To prevent indeterminate system behavior, reserved areas of memory must not be accessed by software or hardware. Any area of the memory map that is not explicitly defined as a register space or accessible memory is considered reserved.

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			gpio_intmask RW 0x0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
gpio_intmask RW 0x0															

gpio_intmask Fields

Bit	Name	Description	Access	Reset
28:0	gpio_intmask	Controls whether an interrupt on Port A Data Register can generate an interrupt to the interrupt controller by not masking it. The unmasked status can be read as well as the resultant status after masking. Note that only bits[26:0] are implemented for gpio2. **Value** — **Description** 0x0 — Interrupt bits are unmasked 0x1 — Mask Interrupt	RW	0x0

gpio_inttype_level

The interrupt level register defines the type of interrupt (edge or level).

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF708038
gpio1	0xFF709000	0xFF709038
gpio2	0xFF70A000	0xFF70A038

Offset: 0x38

Access: RW

Important: To prevent indeterminate system behavior, reserved areas of memory must not be accessed by software or hardware. Any area of the memory map that is not explicitly defined as a register space or accessible memory is considered reserved.

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			gpio_inttype_level RW 0x0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
gpio_inttype_level RW 0x0															

gpio_inttype_level Fields

Bit	Name	Description	Access	Reset
28:0	gpio_inttype_level	This field controls the type of interrupt that can occur on the Port A Data Register. Note that only bits[26:0] are implemented for gpio2. **Value** — **Description** 0x0 — Level-sensitive 0x1 — Edge-sensitive	RW	0x0

gpio_int_polarity

Controls the Polarity of Interrupts that can occur on inputs of Port A Data Register

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF70803C
gpio1	0xFF709000	0xFF70903C
gpio2	0xFF70A000	0xFF70A03C

Offset: 0x3C

Access: RW

Important: To prevent indeterminate system behavior, reserved areas of memory must not be accessed by software or hardware. Any area of the memory map that is not explicitly defined as a register space or accessible memory is considered reserved.

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			gpio_int_polarity RW 0x0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
gpio_int_polarity RW 0x0															

gpio_int_polarity Fields

Bit	Name	Description	Access	Reset
28:0	gpio_int_polarity	Controls the polarity of edge or level sensitivity that can occur on input of Port A Data Register. Note that only bits[26:0] are implemented for gpio2. **Value** — **Description** 0x0 — Active low 0x1 — Active high	RW	0x0

gpio_intstatus

The Interrupt status is reported for all Port A Data Register Bits.

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF708040
gpio1	0xFF709000	0xFF709040
gpio2	0xFF70A000	0xFF70A040

Offset: 0x40

Access: RO

Important: To prevent indeterminate system behavior, reserved areas of memory must not be accessed by software or hardware. Any area of the memory map that is not explicitly defined as a register space or accessible memory is considered reserved.

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			gpio_intstatus RO 0x0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
gpio_intstatus RO 0x0															

gpio_intstatus Fields

Bit	Name	Description	Access	Reset
28:0	gpio_intstatus	Interrupt status of Port A Data Register. Note that only bits[26:0] are implemented for gpio2. **Value** **Description** 0x0 Inactive 0x1 Active	RO	0x0

gpio_raw_intstatus

This is the Raw Interrupt Status Register for Port A Data Register. It is used with the Interrupt Mask Register to allow interrupts from the Port A Data Register.

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF708044
gpio1	0xFF709000	0xFF709044
gpio2	0xFF70A000	0xFF70A044

Offset: 0x44

Access: RO

Important: To prevent indeterminate system behavior, reserved areas of memory must not be accessed by software or hardware. Any area of the memory map that is not explicitly defined as a register space or accessible memory is considered reserved.

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			gpio_raw_intstatus RO 0x0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
gpio_raw_intstatus RO 0x0															

gpio_raw_intstatus Fields

Bit	Name	Description	Access	Reset
28:0	gpio_raw_intstatus	Raw interrupt of status of Port A Data Register (premasking bits). Note that only bits[26:0] are implemented for gpio2. Value: Description 0x0: Inactive 0x1: Active	RO	0x0

gpio_debounce

Debounces each IO Pin

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF708048
gpio1	0xFF709000	0xFF709048
gpio2	0xFF70A000	0xFF70A048

Offset: 0x48

Access: RW

Important: To prevent indeterminate system behavior, reserved areas of memory must not be accessed by software or hardware. Any area of the memory map that is not explicitly defined as a register space or accessible memory is considered reserved.

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			gpio_debounce RW 0x0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
gpio_debounce RW 0x0															

gpio_debounce Fields

Bit	Name	Description	Access	Reset
28:0	gpio_debounce	Controls whether an external signal that is the source of an interrupt needs to be debounced to remove any spurious glitches. A signal must be valid for two periods of an external clock (gpio_db_clk) before it is internally processed. Note that only bits[26:0] are implemented for gpio2. **Value** — **Description** 0x0 — No debounce 0x1 — Enable debounce	RW	0x0

gpio_porta_eoi

Port A Data Register interrupt handling.

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF70804C
gpio1	0xFF709000	0xFF70904C
gpio2	0xFF70A000	0xFF70A04C

Offset: 0x4C

Access: WO

Important: To prevent indeterminate system behavior, reserved areas of memory must not be accessed by software or hardware. Any area of the memory map that is not explicitly defined as a register space or accessible memory is considered reserved.

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			gpio_porta_eoi WO 0x0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
gpio_porta_eoi WO 0x0															

gpio_porta_eoi Fields

Bit	Name	Description	Access	Reset
28:0	gpio_porta_eoi	Controls the clearing of edge type interrupts from the Port A Data Register. Note that only bits[26:0] are implemented for gpio2. Value: Description 0x0: No interrupt clear 0x1: Clear interrupt	WO	0x0

gpio_ext_porta

The external port register is used to input data to the metastability flops.

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF708050
gpio1	0xFF709000	0xFF709050
gpio2	0xFF70A000	0xFF70A050

Offset: 0x50

Access: RO

Important: To prevent indeterminate system behavior, reserved areas of memory must not be accessed by software or hardware. Any area of the memory map that is not explicitly defined as a register space or accessible memory is considered reserved.

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved			gpio_ext_porta RO 0x0												
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
gpio_ext_porta RO 0x0															

gpio_ext_porta Fields

Bit	Name	Description	Access	Reset
28:0	gpio_ext_porta	When Port A Data Register is configured as Input, then reading this location reads the values on the signals. When the data direction of Port A Data Register is set as Output, reading this location reads Port A Data Register. Note that only bits[26:0] are implemented for gpio2.	RO	0x0

gpio_ls_sync

The Synchronization level register is used to synchronize input with l4_mp_clk

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF708060
gpio1	0xFF709000	0xFF709060
gpio2	0xFF70A000	0xFF70A060

Offset: 0x60

Access: RW

Important: To prevent indeterminate system behavior, reserved areas of memory must not be accessed by software or hardware. Any area of the memory map that is not explicitly defined as a register space or accessible memory is considered reserved.

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved															gpio_ls_sync RW 0x0

gpio_ls_sync Fields

Bit	Name	Description	Access	Reset
0	gpio_ls_sync	The level-sensitive interrupts is synchronized to l4_mp_clk. **Value** **Description** 0x0 No synchronization to l4_mp_clk 0x1 Synchronize to l4_mp_clk	RW	0x0

gpio_id_code

GPIO ID code.

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF708064
gpio1	0xFF709000	0xFF709064
gpio2	0xFF70A000	0xFF70A064

Offset: 0x64

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
gpio_id_code RO 0x0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
gpio_id_code RO 0x0															

gpio_id_code Fields

Bit	Name	Description	Access	Reset
31:0	gpio_id_code	Chip identification	RO	0x0

gpio_ver_id_code

GPIO Component Version

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF70806C
gpio1	0xFF709000	0xFF70906C
gpio2	0xFF70A000	0xFF70A06C

Offset: 0x6C

Access: RO

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
gpio_ver_id_code RO 0x3230382A															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
gpio_ver_id_code RO 0x3230382A															

gpio_ver_id_code Fields

Bit	Name	Description	Access	Reset
31:0	gpio_ver_id_code	ASCII value for each number in the version, followed by *. For example. 32_30_31_2A represents the version 2.01	RO	0x3230382A

gpio_config_reg2

Specifies the bit width of port A.

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF708070
gpio1	0xFF709000	0xFF709070
gpio2	0xFF70A000	0xFF70A070

Offset: 0x70

Access: RO

Important: To prevent indeterminate system behavior, reserved areas of memory must not be accessed by software or hardware. Any area of the memory map that is not explicitly defined as a register space or accessible memory is considered reserved.

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												encoded_id_pwidth_d RO 0x7			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
encoded_id_pwidth_d RO 0x7	encoded_id_pwidth_c RO 0x7					encoded_id_pwidth_b RO 0x7						encoded_id_pwidth_a RO 0x1C			

gpio_config_reg2 Fields

Bit	Name	Description	Access	Reset
19:15	encoded_id_pwidth_d	Specifies the width of GPIO Port D. Ignored because there is no Port D in the GPIO. **Value** **Description** 0x7 Width (less 1) of 8 bits 0x1c Width (less 1) of 29 bits	RO	0x7
14:10	encoded_id_pwidth_c	Specifies the width of GPIO Port C. Ignored because there is no Port C in the GPIO. **Value** **Description** 0x7 Width (less 1) of 8 bits 0x1c Width (less 1) of 29 bits	RO	0x7
9:5	encoded_id_pwidth_b	Specifies the width of GPIO Port B. Ignored because there is no Port B in the GPIO. **Value** **Description** 0x7 Width (less 1) of 8 bits 0x1c Width (less 1) of 29 bits	RO	0x7
4:0	encoded_id_pwidth_a	Specifies the width of GPIO Port A. The value 28 represents the 29-bit width less one. **Value** **Description** 0x7 Width (less 1) of 8 bits 0x1c Width (less 1) of 29 bits	RO	0x1C

gpio_config_reg1

Reports settings of various GPIO configuration parameters

Module Instance	Base Address	Register Address
gpio0	0xFF708000	0xFF708074
gpio1	0xFF709000	0xFF709074
gpio2	0xFF70A000	0xFF70A074

Offset: 0x74

Access: RO

Important: To prevent indeterminate system behavior, reserved areas of memory must not be accessed by software or hardware. Any area of the memory map that is not explicitly defined as a register space or accessible memory is considered reserved.

Bit Fields															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved											encoded_id_width RO 0x1F				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
gpio_id RO 0x1	add_encoded_params RO 0x1	debounce RO 0x1	porta_intr RO 0x1	Reserved			hw_porta RO 0x0	portd_single_ctl RO 0x1	portc_single_ctl RO 0x1	portb_single_ctl RO 0x1	porta_single_ctl RO 0x1	num_ports RO 0x0		apb_data_width RO 0x2	

gpio_config_reg1 Fields

Bit	Name	Description	Access	Reset
20:16	encoded_id_width	This value is fixed at 32 bits. **Value** **Description** 0x1f Width of ID Field	RO	0x1F
15	gpio_id	Provides an ID code value **Value** **Description** 0x1 GPIO ID Code	RO	0x1

Bit	Name	Description	Access	Reset
14	add_encoded_params	Fixed to allow the indentification of the Designware IP component. **Value** **Description** 0x1 Enable IP indentification	RO	0x1
13	debounce	The value of this field is fixed to allow debouncing of the Port A signals. **Value** **Description** 0x1 Debounce is Enabled	RO	0x1
12	porta_intr	The value of this field is fixed to allow interrupts on Port A. **Value** **Description** 0x1 Port A Interrupts Enabled	RO	0x1
8	hw_porta	The value is fixed to enable Port A configuration to be controlled by software only. **Value** **Description** 0x0 Software Configuration Control Enabled	RO	0x0
7	portd_single_ctl	Indicates the mode of operation of Port D to be software controlled only. Ignored because there is no Port D in the GPIO. **Value** **Description** 0x1 Software Enabled Individual Port Control	RO	0x1
6	portc_single_ctl	Indicates the mode of operation of Port C to be software controlled only. Ignored because there is no Port C in the GPIO. **Value** **Description** 0x1 Software Enabled Individual Port Control	RO	0x1

Bit	Name	Description	Access	Reset
5	portb_single_ctl	Indicates the mode of operation of Port B to be software controlled only. Ignored because there is no Port B in the GPIO. **Value** **Description** 0x1 Software Enabled Individual Port Control	RO	0x1
4	porta_single_ctl	Indicates the mode of operation of Port A to be software controlled only. **Value** **Description** 0x1 Software Enabled Individual Port Control	RO	0x1
3:2	num_ports	The value of this register is fixed at one port (Port A). **Value** **Description** 0x0 Number of GPIO Ports = 1	RO	0x0
1:0	apb_data_width	Fixed to support an ABP data bus width of 32-bits. **Value** **Description** 0x2 APB Data Width = 32-bits	RO	0x2

Document Revision History

Table 22-3: Document Revision History

Date	Version	Changes
October 2016	2016.10.28	Maintenance release.
May 2016	2016.05.27	Maintenance release.
May 2016	2016.05.03	Maintenance release.
November 2015	2015.11.02	Maintenance release.
May 2015	2015.05.04	Maintenance release.
December 2014	2014.12.15	• Maintenance release. • Added *Taking the GPIO Out of Reset* section.
June 2014	2014.06.30	Added Address Map and Register Descriptions

Date	Version	Changes
February 2014	2014.02.28	Updated content in sections: • Features of the GPIO Interface • GPIO Interface Block Diagram and System Integration • Debounce Operation
December 2013	2013.12.30	Minor formatting updates Updated GPIO interface block diagram and GPIO interface pin table
November 2012	1.2	Minor updates.
May 2012	1.1	Added programming model section.
January 2012	1.0	Initial release.