Isaias Osorio

CPE301 – SPRING 2016

Design Assignment X

**DO NOT REMOVE THIS PAGE DURING SUBMISSION:**

The student understands that all required components should be submitted in complete for grading of this assignment.

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| --- | --- | --- | --- |
| **NO** | **SUBMISSION ITEM** | **COMPLETED (Y/N)** | **MARKS**  **(/MAX)** |
| 0. | COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS |  |  |
| 1. | INITIAL CODE OF TASK 1/A |  |  |
| 2. | INCREMENTAL / DIFFERENTIAL CODE OF TASK 2/B |  |  |
| 3. | INCREMENTAL / DIFFERENTIAL CODE OF TASK 3/C |  |  |
| 4. | INCREMENTAL / DIFFERENTIAL CODE OF TASK 4/D |  |  |
| 5. | INCREMENTAL / DIFFERENTIAL CODE OF TASK 5/E |  |  |
| 6. | SCHEMATICS |  |  |
| 7. | SCREENSHOTS OF EACH TASK OUTPUT |  |  |
| 8. | SCREENSHOT OF EACH DEMO |  |  |
| 9. | VIDEO LINKS OF EACH DEMO |  |  |
| 10. | GOOGLECODE LINK OF THE DA |  |  |
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| 0. | COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS |  |  |

1. Atmel Studio

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| 1. | INITIAL CODE OF TASK 1/A |  |  |

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; DesignAssignment0.asm

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; Created: 2/16/2016 8:54:39 PM

; Author : Isaias Osorio

;

; Replace with your application code

start:

ldi r16, 33 ;Load registers with numbers

ldi r17, 36

ldi r18, 39

ldi r19, 42

ldi r20, 45

sbi DDRB, 2 ; Port B set as output using pin 2

out PORTB, r0 ; Set all outputs to 0

add r20, r16 ;For some reason loading immediates only starting at register 16

add r20, r17 ;Add the integers

add r20, r18

add r20, r19

brcc End ; Carry flag

ldi r17, 4

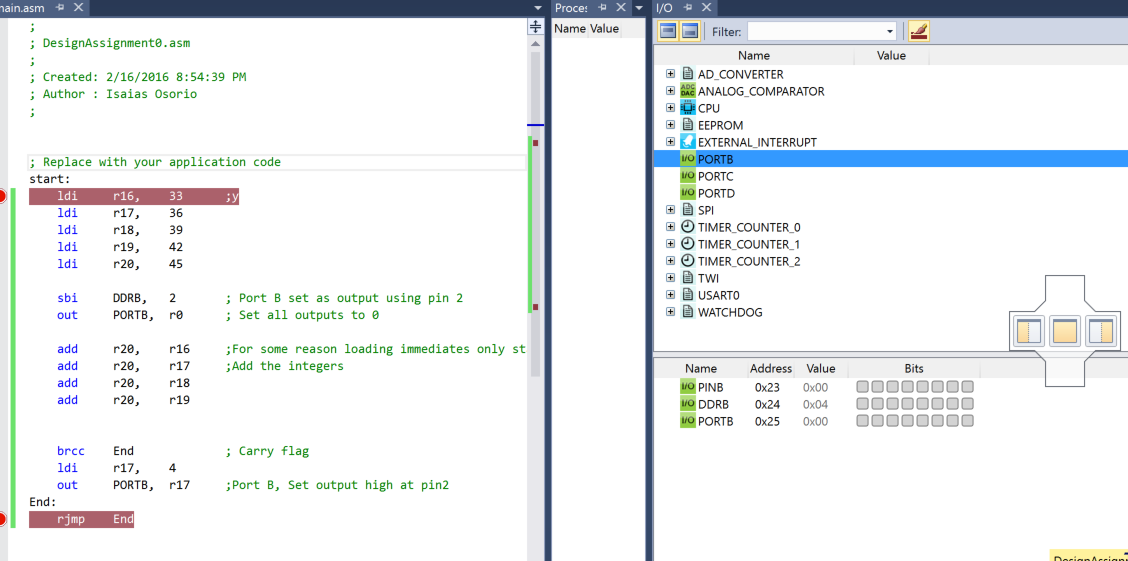
out PORTB, r17 ;Port B, Set output high at pin2

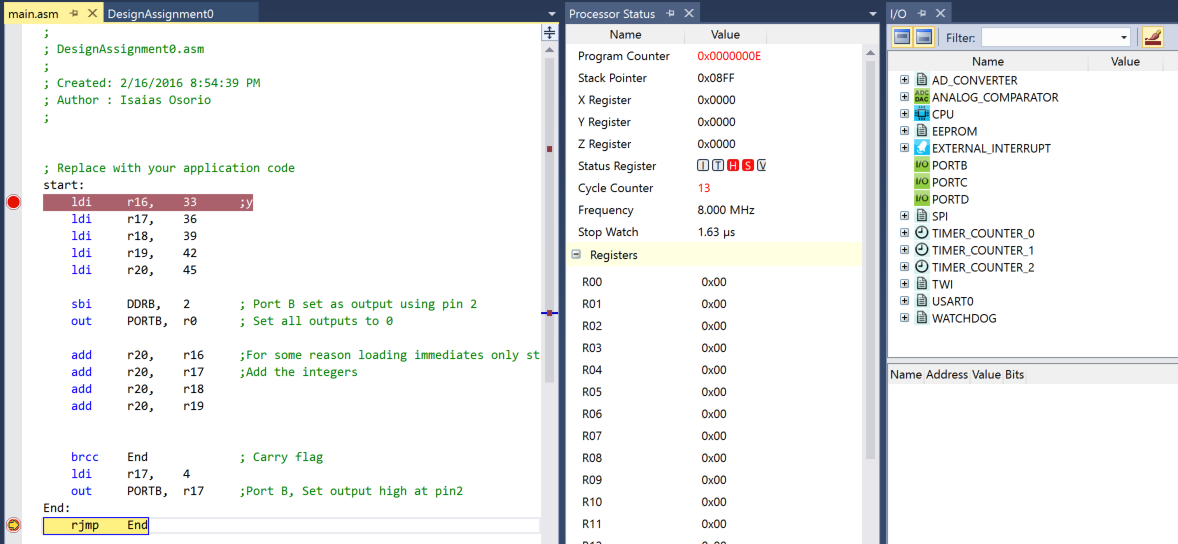
End:

rjmp End

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| --- | --- | --- | --- |
| 2. | TASK B |  |  |

Initial



End

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| 6. | SCHEMATICS |  |  |

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| 9. | VIDEO LINKS OF EACH DEMO |  |  |
| n/a | | | |
| 10. | GOOGLECODE LINK OF THE DA |  |  |
| https://github.com/isaiasmoioso/CPE-301.git | | | |

**Student Academic Misconduct Policy**

<http://studentconduct.unlv.edu/misconduct/policy.html>

“This assignment submission is my own, original work”.

NAME OF THE STUDENT